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32-bit Arm® Cortex®-R5F TRAVEO™ T1G Microcontroller

S6J3360/70 is a series of Automotive Cluster applications in general meter control to connect to the driver as speed meter, tachometer, temperature meter, and fuel meter. This embedded device enables next-generation functions such as Controller Area Network with Flexible Data rate (CAN FD) and Secure Hardware Extension (SHE). MCUs for this application require an operating temperature range of T_A -40 °C to 105 °C and Automotive Electronics Council (AEC) qualification.

Features

Key Features

- 32-bit Arm® Cortex®-R5F CPU core at up to 132 MHz
- 80-MHz internal flash memory access speed
- Flash memory size (max)
 - TC-Flash: 2,112 KB/ Work-Flash: 112 KB
- RAM size (max)
 - TC-RAM: 128 KB/ System -RAM: 128 KB (this includes 16 KB + 8 KB back-up area)
- 5 V or 3.3 V power supply voltage
- Packages
 - LQFP packages (144-pin)
 - TEQFP packages (176-pin/144-pin)
- ASIL-B support for ISO 26262 specification
- CMOS 40-nm technology
- JTAG debug interface
- Operating temperature: -40 to 105 °C

Peripheral Functions

- System
 - External interrupt
 - I/O timer (Free-run timer/ Input capture/ Output compare)
 - 12-bit A/D converter
 - Base timer
 - Reload timer
 - DMA controller
- Applications
 - Stepper motor controller
 - LCD controller
 - Real time clock
 - LCD bus interface
 - Indicator PWM
- Sound function
 - Sound waveform generator
 - Sound mixer
 - PCM-PWM
 - I2S
 - Sound generator
- External device and memory interface
 - CAN FD controller
 - Multi-function serial interface (UART, CSIO, LIN and I²C)
 - DDR-HSSPI
 - External bus interface
- Security and safety
 - Secure Hardware Extension (SHE)
 - Safety features such as MPU, TPU, ECC, and others
 - Watchdog timer
 - Low-voltage detector
 - Clock supervisor

Figure 1: Functional Diagram

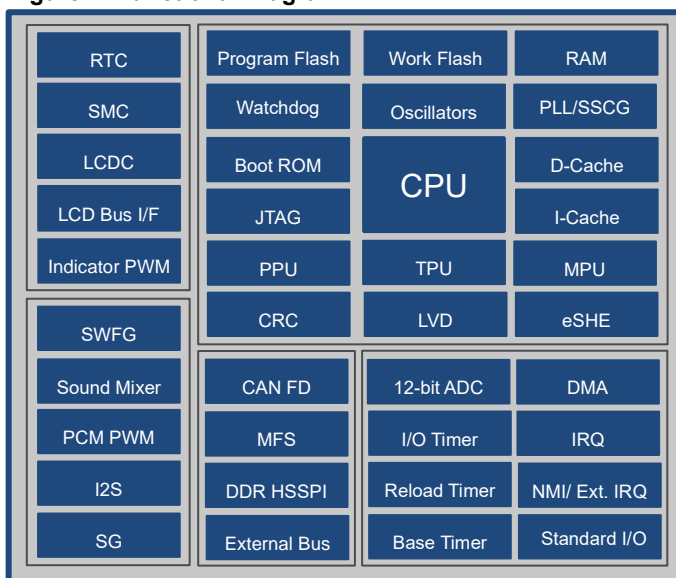


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1. Features

1.1 Function List

The following table shows the functions that are implemented in the S6J3360/S6J3370 series.

| Function | S6J33xxJxx 176-Pin | S6J33xxHxx 144-Pin | Remarks |
|-------------------------------------|--|-----------------------|------------------------------|
| CPU core | Arm® Cortex®-R5F | | |
| FPU | Available | | |
| PPU | Available | | |
| MPU | Available | | |
| TPU | Available | | |
| Endian | Little endian | | |
| Core clock frequency | 132 MHz | | See section 7.4.3 |
| HPM bus frequency | Option | | See section 7.4.3 |
| LLPM bus frequency | Option | | See section 7.4.3 |
| Resource clock frequency | Option | | See section 7.4.3 |
| Embedded CR oscillation | Slow clock: 100 kHz Fast clock: 4 MHz (Center frequency) | | |
| PLL | PLL0, Expand PLL0,1,2 | | |
| SSCG PLL | SSCG0 | | |
| Clock supervisor | Available | | |
| DMA | 16 ch | | |
| Boot-ROM | 16 KB | | |
| JTAG | Available | | |
| Data cache | 16 KB | | |
| Instruction cache | 16 KB | | |
| Program Flash | Option | | See section 1.2.1 |
| Work Flash | 112 KB | | See section 1.2.1 |
| TC-RAM | 128 KB | | See section 1.2.1 |
| System-RAM | 128 KB (include backup area) | | See section 1.2.1 |
| Backup area in System-RAM | 16+8 KB | | See section 1.2.1 |
| Security (SHE) | Available | | |
| Low latency interrupt | Available | | |
| Power domain | 3 domains | | PD1/PD2/PD4 (PD4_1,PD4_2) |
| Power supply | 5.0 V ± 0.5 V or 3.3 V ± 0.3 V | | |
| Embedded LDO power supply for 5.0 V | Available | | |

| Function | S6J33xxJxx 176-Pin | S6J33xxHxx 144-Pin | Remarks |
|--|--|---|-------------------------------------|
| Low-voltage detection of external power supply | Available | | |
| Low-voltage detection of internal LDO output | Available | | |
| Hardware watchdog timer | Available | | |
| Software watchdog timer | Available | | |
| Package | TEQPF-176 (0.5 mm) | LQFP-144 (0.4 mm)/ LQFP-144 (0.5 mm)/ TEQFP-144 (0.4 mm)/ TEQFP-144 (0.5 mm) | See section 1.2.1 (): pin pitch |
| General-purpose I/O | 126 ports (124 ports) | 94 ports (92 ports) | (): When used sub clock |
| QPRC | 2 ch | | |
| 32-bit reload timer | 6 ch (Input: 6 pin/ Output: 6 pin) | | |
| Real-time clock | Available | | Automatic calibration |
| Sound waveform generator | 1 unit × 5 outputs | | |
| Sound mixer | 1 unit × 10 inputs | | |
| PCM-PWM | 1 unit (L and R) | | |
| Base timer | 16 units (32 ch) | | |
| Free-run timer | 8 ch (Input: 8 pin) | | |
| Input capture unit | 12 ch | | |
| Output compare unit | 12 ch (Output: 12 pin) | | |
| Stepping motor controller (SMC) | 6 gauges | | |
| 12-bit A/D converter | 48 ch | 40 ch | 1 unit |
| Partial wake up | Analog input 8 ch Trigger 1 ch | | |
| CRC | 4 ch | | |
| Programmable CRC | 1 ch | | |
| Source clock timer | 4 ch | | |
| NMI | Available | | |
| External interrupt | 24 ch | | |
| Internal interrupt | 256 vectors | | |

| Function | S6J33xxJxx 176-Pin | S6J33xxHxx 144-Pin | Remarks |
|---------------------------------|--|------------------------------------|--|
| I2S | 2 ch (ch0: Output only ch1: Input/ Output) | | One only supports an output as a function of the sound system. |
| DDR HSSPI | 1 ch | | |
| Segment LCD controller | 4 COM × 32 SEG | | |
| LCD bus interface | Data: 18 bit | | |
| Ext. bus interface | Address: 22 bit Data: 16 bit | Address: 15 bit Data: 16 bit | |
| CAN FD | 4 ch | | |
| CAN FD RAM (ECC supported) | 16 KB/ch It is equivalent to a 128-message buffer per channel of the CAN module | | |
| Multi-function serial interface | 12 ch | | |
| | I ² C | 10 ch (Fast mode support: 2 ch) | |
| Sound generator | 5 ch | | |
| Indicator PWM | 1 ch | | |
| Clock output | 1 ch | | |

Notes:

- The optional functions are described in section 1.2
- The specifications in the table that are related to electrical characteristics only show the typical values. They do not necessarily include the width of characteristics, errors, and so on. The details are described in section 7.2.

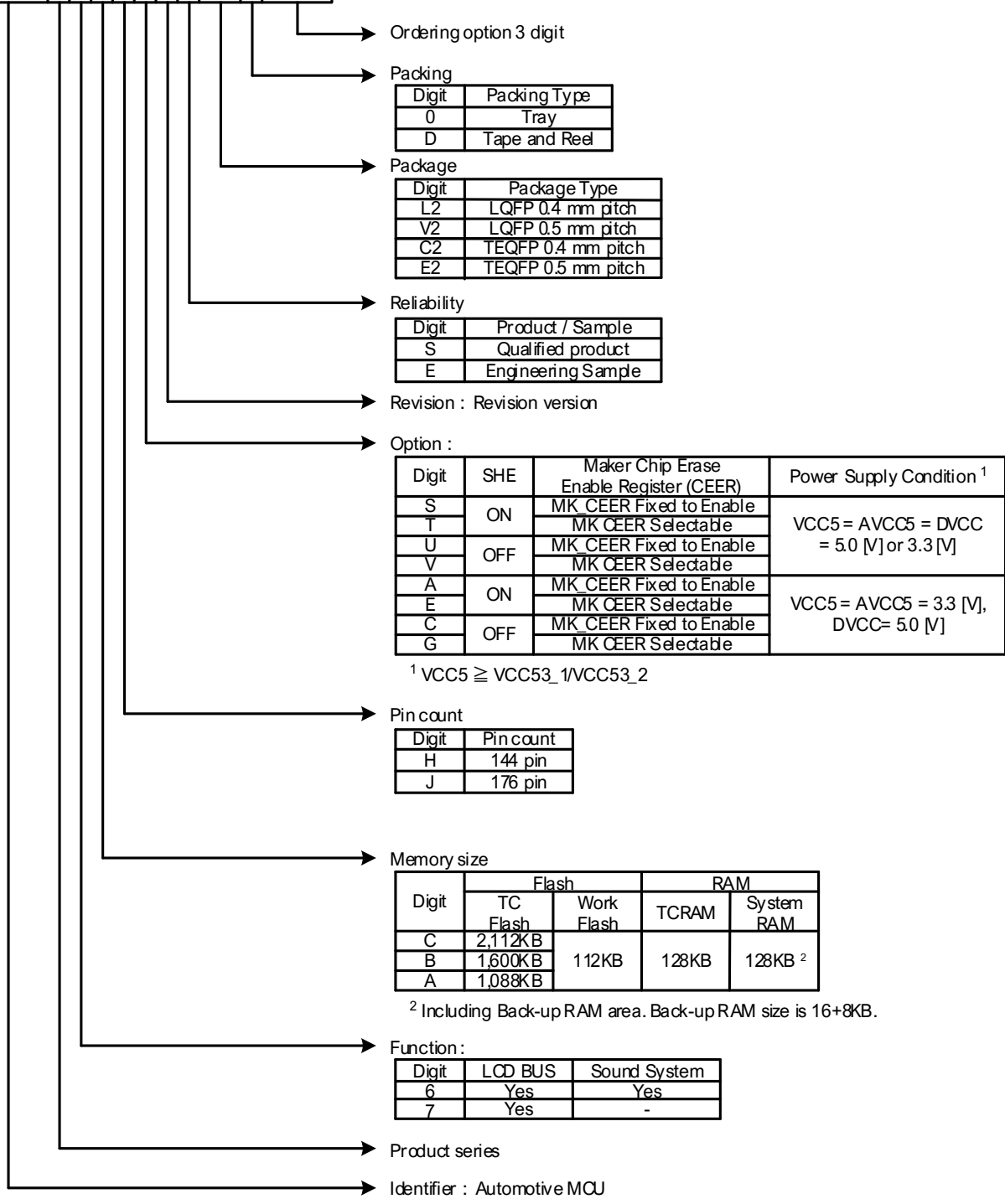
1.2 Optional Function

1.2.1 Basic Option

The following figure shows the optional functions and the part number relations of the series.

◆Basic Option

S 6 J 3 | 3 0 0 | H A A S | V 2 0 | x x x



Note:

- This table only shows the relation between the optional function and the part numbers; that is, all products are not necessarily available for orders. See the order number on the datasheet and confirm product availability.
- Relationship of package option and pin count option is as follows.

(S6J3370 series support LQFP package. S6J3360 series don't support LQFP package.)

| | | Pin count | | |
|---------|----|--------------------|--------|---|
| | | H | J | |
| | | 144pin | 176pin | |
| Package | L2 | LQFP 0.4 mm pitch | ○ | - |
| | V2 | LQFP 0.5 mm pitch | ○ | - |
| | C2 | TEQFP 0.4 mm pitch | ○ | - |
| | E2 | TEQFP 0.5 mm pitch | ○ | ○ |

○: Support, —: Not support.

1.2.2 ID

ID is specified for each memory size digit, option digit, and revision.

| Memory Size | Option | Revision | Chip ID | JTAG ID | SHE Module ID (SHE_MID) * |
|-------------|--------|------------|------------|------------|---------------------------|
| C | S | B | 0x10160101 | 0x002505CF | 0x000F_0300 |
| | T | | | 0x002515CF | |
| | U | | | 0x002525CF | |
| | V | | | 0x002535CF | |
| | A | | 0x10168101 | 0x002505CF | |
| | E | | | 0x002515CF | |
| | C | | | 0x002525CF | |
| | G | | | 0x002535CF | |
| B | S | | 0x10160101 | 0x002545CF | |
| | T | | | 0x002555CF | |
| | U | | | 0x002565CF | |
| | V | | | 0x002575CF | |
| | A | | 0x10168101 | 0x002545CF | |
| | E | | | 0x002555CF | |
| | C | | | 0x002565CF | |
| | G | | | 0x002575CF | |
| A | S | 0x10160101 | 0x002585CF | | |
| | T | | 0x002595CF | | |
| | U | | 0x0025A5CF | | |
| | V | | 0x0025B5CF | | |
| | A | 0x10168101 | 0x002585CF | | |
| | E | | 0x002595CF | | |
| | C | | 0x0025A5CF | | |
| | G | | 0x0025B5CF | | |

* See the "SHE Module ID Register" in the "Secure Hardware Extension (SHE)" chapter in the TRAVEO™ T1G Platform hardware manual for details.

2. Handling Precautions

Semiconductor devices inherently have a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, and so on). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

2.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, and so on) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing overvoltage and overcurrent conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of output pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling unused input pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Make sure that voltages applied to pins do not exceed the absolute maximum ratings. This must include attention to abnormal noise, surge levels, and so on.
2. Make sure that abnormal current flows do not occur during the power-on sequence.

Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, and so on. Customers are requested to observe applicable regulations and standards in the design of products.

Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Precautions Related to Usage of Devices

Cypress Semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, and so on).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, and so on) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

2.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason, it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and have established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Pb-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70 % relative humidity, and at temperatures between 5 °C and 30 °C.
When you open a dry package, the relative humidity must be 40 % to 70 %.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125 °C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40 % and 70 %. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 M Ω).
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

2.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity
Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity
When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil
Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, including cosmic radiation
Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame
CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

3. Handling Devices

Latch-Up Prevention

The latch-up phenomenon may occur on a CMOS IC in the following cases: the voltage applied to an input or output pin is higher than VCC5 or lower than VSS; or the voltage applied between a VCC5 pin and a VSS pin exceeds the rating. A latch-up causes a rapid increase in the power supply current, possibly resulting in thermal damage to an element. When using the device, take sufficient care not to exceed the maximum rating.

Also, be careful that analog power supplies (AVCC5, AVRH5) and analog inputs do not exceed the digital power supply (VCC5) at the analog system power-on and power-off times. The power-on sequence is as follows. Simultaneously, turn on the digital supply voltage (VCC5) and analog supply voltages (AVCC5, AVRH5), or turn on the digital supply voltage (VCC5) and then the analog supply voltages (AVCC5, AVRH5).

Handling Unused Pins

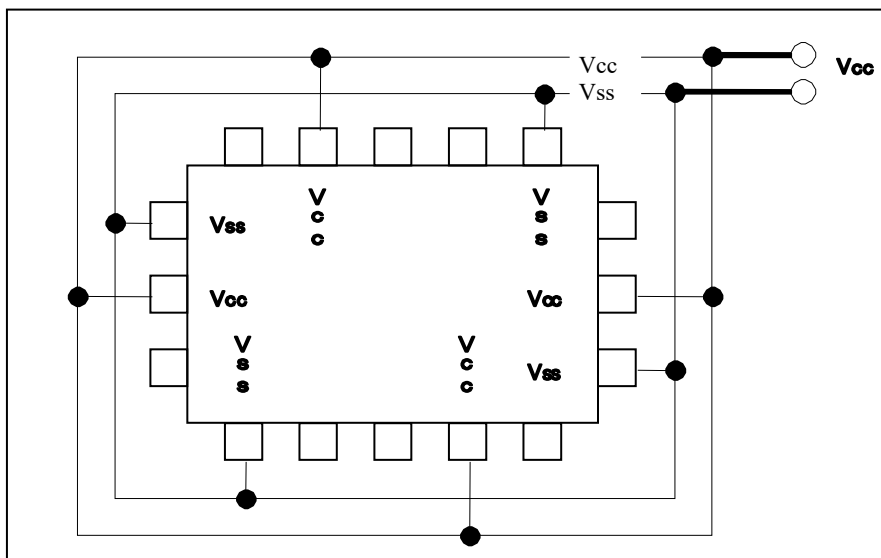
Leaving unused input pins open may cause permanent damage from a malfunction or latch-up. Take measures, such as pulling up or pulling down the voltage with resistors of 2 kΩ or higher, for unused pins.

If there are any unused input/output pins, set them to the output state and then open them, or set them to the input state and handle them in the same way as input pins.

Power Supply Pins

If the device has multiple VCC and VSS pins, the device is designed in such a way that the pins of the same potential are connected to each other inside the device to prevent malfunctions such as latch-up. However, to reduce unwanted emissions, prevent malfunctions of strobe signals caused by an increase of the ground level, and observe standards on total output current, be sure to connect all the VCC and VSS pins to the power source and ground externally. Also, handle all the VSS power supply pins as shown in the following diagram. If there are multiple VCC or VSS systems, the device does not operate normally even within the guaranteed operating range.

Figure 1-1 Pin Assignment



In addition, consider connecting with low impedance from the power supply source to the VCC and VSS of this device.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the VCC pin and the VSS pin.

Crystal Oscillation Circuit

Noise entering the X0 or X1 pin may cause a malfunction. Design the printed circuit board in such a way that the X0 and X1 pins, the crystal oscillator (or ceramic resonator), and a bypass capacitor to ground are located very close to the device.

Cypress recommends that the printed circuit board artwork have the X0 and X1 pins enclosed by ground.

Mode Pin (MODE)

Use mode pin (MODE) by directly connecting it to a VCC5 or VSS pin. To prevent noise from causing the device to accidentally enter test mode, reduce the pattern length between each mode pin and a VCC5 or VSS pin on the printed circuit board, and connect them with low impedance.

PLL Clock Operation

While a PLL clock is selected, if the oscillator breaks off or input stops, the PLL clock may continue operating with the free running frequency of the internal self-oscillator circuit. This operation is outside of the guaranteed range.

Power Supply Pin Processing of an A/D Converter

Even when no A/D converter is used, establish a connection such that $AVCC5 = AVRH5 = VCC5$, and $AVSS = VSS$.

Power-on Sequence of the Power Supply Analog Inputs of an A/D Converter

Be sure to turn on the digital power supply (VCC5) before the application of the power supplies (AVCC5, AVRH5) and analog inputs (ADC0_AN0 to ADC0_AN47) of an A/D converter. At the power-off time, turn off the power supplies and analog inputs of the A/D converter, and then turn off the digital power supply (VCC5). Perform these power-on and power-off operations without AVRH5 exceeding AVCC5. Even when using a pin shared with an analog input as an input port, do not allow the input voltage to exceed AVCC5. (Turning on or off the analog supply voltage and digital supply voltage simultaneously is not a problem.)

C-Pin Processing

This device has a built-in voltage step-down circuit. Be sure to connect a capacitor to the C pin (See the pin assignment) for internal stabilization of the device. For the standard values, see "Recommended operating conditions" in the latest datasheet.

Writing to a Register Containing a Status Flag

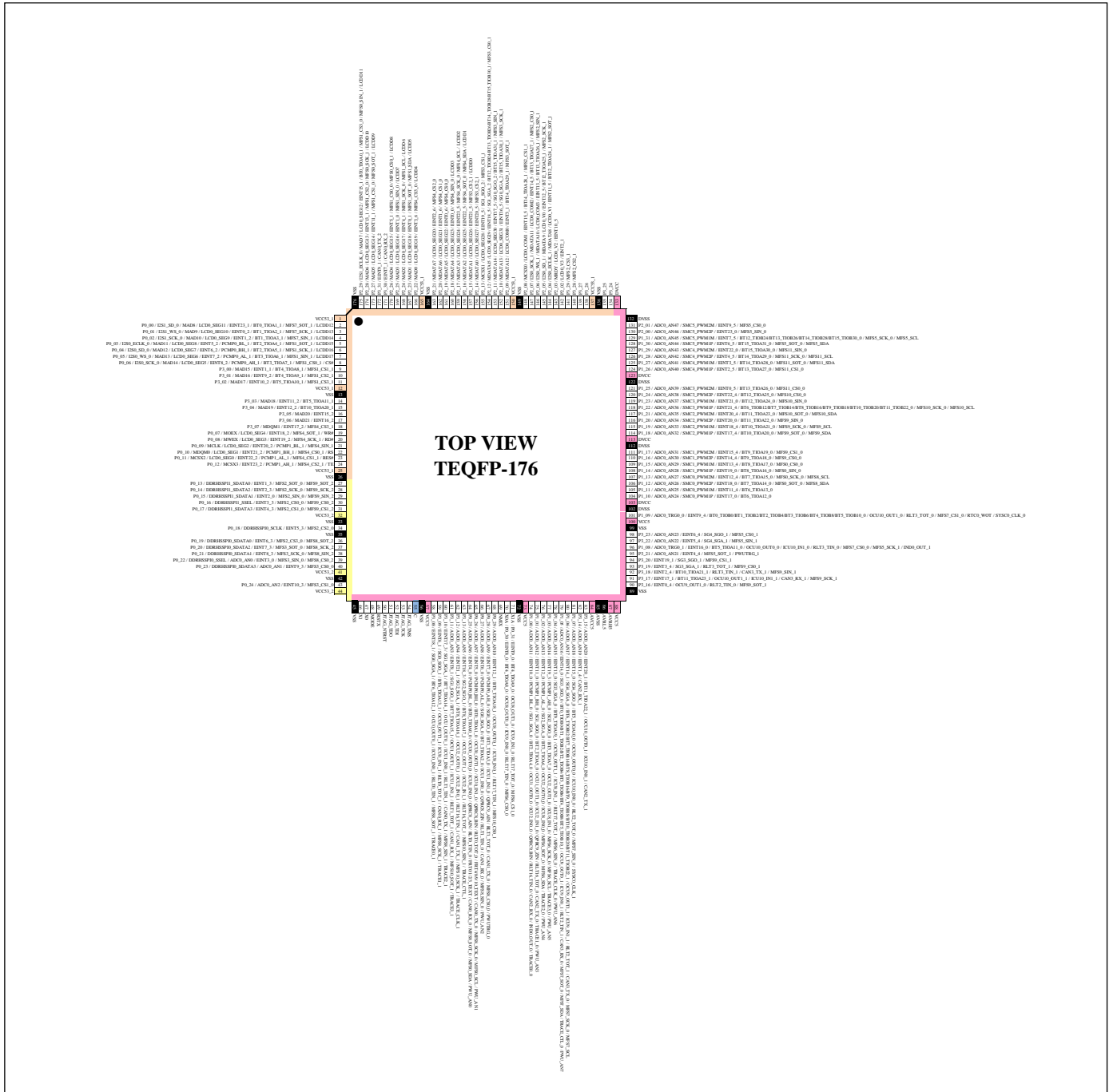
When you write to a register containing a status flag (such as an interrupt request flag) to control a function, take care not to accidentally clear the status flag. Therefore, before the write operation, configure the status bit such that the flag is not cleared, and then set the control bit to the desired value. Especially for control bits configured as a set of multiple bits, bit instructions cannot be used (bit instructions only have 1-bit access). In such cases, byte, half-word, or word access is used to write to the control bits and a status flag simultaneously. However, at this time, be careful not to accidentally clear bits other than the intended ones (the status flag bit in this case).

Note: Bit instructions take this point into consideration for registers that support bit-band units, so it does not need to be a concern. You need to take care when using bit instructions for registers that do not support bit-band units.

4. Pin Assignment

4.1 TEQFP 176 Pin Assignment

Figure 4-1: TEQFP-176



5. Pin Descriptions

5.1 Pin Descriptions

5.1.1 TEQFP176

Table 5-1-1: Pin Descriptions of TEQFP176

| TEQFP176 | | | |
|----------|-------------|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 1 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 2 | P0_00 | P | GPIO port |
| | I2S1_SD_0 | | I2S ch.1 serial data I/O pin_0 |
| | MAD8 | | External bus interface address output pin |
| | LCD0_SEG11 | | LCD controller segment output pin |
| | EINT23_1 | | External interrupt ch.23 input pin_1 |
| | BT0_TIOA1_1 | | Base timer0 ch.1 TIOA output pin_1 |
| | MFS7_SOT_1 | | Multi-function serial ch.7 serial data output pin_1 |
| | LCDD12 | | LCD bus interface data I/O pin |
| 3 | P0_01 | P | GPIO port |
| | I2S1_WS_0 | | I2S ch.1 word select pin_0 |
| | MAD9 | | External bus interface address output pin |
| | LCD0_SEG10 | | LCD controller segment output pin |
| | EINT0_2 | | External interrupt ch.0 input pin_2 |
| | BT1_TIOA2_1 | | Base timer1 ch.2 TIOA output pin_1 |
| | MFS7_SCK_1 | | Multi-function serial ch.7 clock I/O pin_1 |
| | LCDD13 | | LCD bus interface data I/O pin |
| 4 | P0_02 | P | GPIO port |
| | I2S1_SCK_0 | | I2S ch.1 serial clock pin_0 |
| | MAD10 | | External bus interface address output pin |
| | LCD0_SEG9 | | LCD controller segment output pin |
| | EINT1_2 | | External interrupt ch.1 input pin_2 |
| | BT1_TIOA3_1 | | Base timer1 ch.3 TIOA output pin_1 |
| | MFS7_SIN_1 | | Multi-function serial ch.7 serial data input pin_1 |
| | LCDD14 | | LCD bus interface data I/O pin |
| 5 | P0_03 | P | GPIO port |
| | I2S0_ECLK_0 | | I2S ch.0 external clock input pin_0 |
| | MAD11 | | External bus interface address output pin |
| | LCD0_SEG8 | | LCD controller segment output pin |
| | EINT5_2 | | External interrupt ch.5 input pin_2 |
| | PCMP0_BL_1 | | PCM_PWM ch.0 BL output pin_1 |
| | BT2_TIOA4_1 | | Base timer2 ch.4 TIOA output pin_1 |
| | MFS1_SOT_1 | | Multi-function serial ch.1 serial data output pin_1 |
| | LCDD15 | | LCD bus interface data I/O pin |

| TEQFP176 | | | |
|----------|--------------|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 6 | P0_04 | P | GPIO port |
| | I2S0_SD_0 | | I2S ch.0 serial data I/O pin_0 |
| | MAD12 | | External bus interface address output pin |
| | LCD0_SEG7 | | LCD controller segment output pin |
| | EINT6_2 | | External interrupt ch.6 input pin_2 |
| | PCMP0_BH_1 | | PCM_PWM ch.0 BH output pin_1 |
| | BT2_TIOA5_1 | | Base timer2 ch.5 TIOA output pin_1 |
| | MFS1_SCK_1 | | Multi-function serial ch.1 clock I/O pin_1 |
| | LCDD16 | | LCD bus interface data I/O pin |
| 7 | P0_05 | P | GPIO port |
| | I2S0_WS_0 | | I2S ch.0 word select pin_0 |
| | MAD13 | | External bus interface address output pin |
| | LCD0_SEG6 | | LCD controller segment output pin |
| | EINT7_2 | | External interrupt ch.7 input pin_2 |
| | PCMP0_AL_1 | | PCM_PWM ch.0 AL output pin_1 |
| | BT3_TIOA6_1 | | Base timer3 ch.6 TIOA output pin_1 |
| | MFS1_SIN_1 | | Multi-function serial ch.1 serial data input pin_1 |
| | LCDD17 | | LCD bus interface data I/O pin |
| 8 | P0_06 | P | GPIO port |
| | I2S0_SCK_0 | | I2S ch.0 serial clock pin_0 |
| | MAD14 | | External bus interface address output pin |
| | LCD0_SEG5 | | LCD controller segment output pin |
| | EINT8_2 | | External interrupt ch.8 input pin_2 |
| | PCMP0_AH_1 | | PCM_PWM ch.0 AH output pin_1 |
| | BT3_TIOA7_1 | | Base timer3 ch.7 TIOA output pin_1 |
| | MFS1_CS0_1 | | Multi-function serial ch.1 serial chip select 0 I/O pin_1 |
| | CS# | | LCD bus interface chip select output pin |
| 9 | P3_00 | A | GPIO port |
| | MAD15 | | External bus interface address output pin |
| | EINT1_1 | | External interrupt ch.1 input pin_1 |
| | BT4_TIOA8_1 | | Base timer4 ch.8 TIOA output pin_1 |
| | MFS1_CS1_1 | | Multi-function serial ch.1 serial chip select 1 output pin_1 |
| 10 | P3_01 | A | GPIO port |
| | MAD16 | | External bus interface address output pin |
| | EINT9_2 | | External interrupt ch.9 input pin_2 |
| | BT4_TIOA9_1 | | Base timer4 ch.9 TIOA output pin_1 |
| | MFS1_CS2_1 | | Multi-function serial ch.1 serial chip select 2 output pin_1 |
| 11 | P3_02 | A | GPIO port |
| | MAD17 | | External bus interface address output pin |
| | EINT10_2 | | External interrupt ch.10 input pin_2 |
| | BT5_TIOA10_1 | | Base timer5 ch.10 TIOA output pin_1 |
| | MFS1_CS3_1 | | Multi-function serial ch.1 serial chip select 3 output pin_1 |
| 12 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 13 | VSS | - | GND |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 14 | P3_03 | A | GPIO port |
| | MAD18 | | External bus interface address output pin |
| | EINT11_2 | | External interrupt ch.11 input pin_2 |
| | BT5_TIOA11_1 | | Base timer5 ch.11 TIOA output pin_1 |
| 15 | P3_04 | A | GPIO port |
| | MAD19 | | External bus interface address output pin |
| | EINT12_2 | | External interrupt ch.12 input pin_2 |
| | BT10_TIOA20_1 | | Base timer10 ch.20 TIOA output pin_1 |
| 16 | P3_05 | A | GPIO port |
| | MAD20 | | External bus interface address output pin |
| | EINT15_2 | | External interrupt ch.15 input pin_2 |
| 17 | P3_06 | A | GPIO port |
| | MAD21 | | External bus interface address output pin |
| | EINT16_2 | | External interrupt ch.16 input pin_2 |
| 18 | P3_07 | A | GPIO port |
| | MDQM1 | | External bus interface byte mask signal output pin |
| | EINT17_2 | | External interrupt ch.17 input pin_2 |
| | MFS4_CS3_1 | | Multi-function serial ch.4 serial chip select 3 output pin_1 |
| 19 | P0_07 | P | GPIO port |
| | MOEX | | External bus interface read enable signal output pin |
| | LCD0_SEG4 | | LCD controller segment output pin |
| | EINT18_2 | | External interrupt ch.18 input pin_2 |
| | MFS4_SOT_1 | | Multi-function serial ch.4 serial data output pin_1 |
| | WR# | | LCD bus interface write enable output pin |
| 20 | P0_08 | P | GPIO port |
| | MWEX | | External bus interface write enable signal output pin |
| | LCD0_SEG3 | | LCD controller segment output pin |
| | EINT19_2 | | External interrupt ch.19 input pin_2 |
| | MFS4_SCK_1 | | Multi-function serial ch.4 clock I/O pin_1 |
| | RD# | | LCD bus interface read enable output pin |
| 21 | P0_09 | P | GPIO port |
| | MCLK | | External bus interface clock output pin |
| | LCD0_SEG2 | | LCD controller segment output pin |
| | EINT20_2 | | External interrupt ch.20 input pin_2 |
| | PCMP1_BL_1 | | PCM_PWM ch.1 BL output pin_1 |
| | MFS4_SIN_1 | | Multi-function serial ch.4 serial data input pin_1 |
| 22 | P0_10 | P | GPIO port |
| | MDQM0 | | External bus interface byte mask signal output pin |
| | LCD0_SEG1 | | LCD controller segment output pin |
| | EINT21_2 | | External interrupt ch.21 input pin_2 |
| | PCMP1_BH_1 | | PCM_PWM ch.1 BH output pin_1 |
| | MFS4_CS0_1 | | Multi-function serial ch.4 serial chip select 0 I/O pin_1 |
| | RS | | LCD bus interface register select output pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 23 | P0_11 | P | GPIO port |
| | MCSX2 | | External bus interface chip select output pin |
| | LCD0_SEG0 | | LCD controller segment output pin |
| | EINT22_2 | | External interrupt ch.22 input pin_2 |
| | PCMP1_AL_1 | | PCM_PWM ch.1 AL output pin_1 |
| | MFS4_CS1_1 | | Multi-function serial ch.4 serial chip select 1 output pin_1 |
| | RES# | | LCD bus interface reset control output pin |
| 24 | P0_12 | A | GPIO port |
| | MCSX3 | | External bus interface chip select output pin |
| | EINT23_2 | | External interrupt ch.23 input pin_2 |
| | PCMP1_AH_1 | | PCM_PWM ch.1 AH output pin_1 |
| | MFS4_CS2_1 | | Multi-function serial ch.4 serial chip select 2 output pin_1 |
| | TE | | LCD bus interface tearing effect input pin |
| 25 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 26 | VSS | - | GND |
| 27 | P0_13 | M | GPIO port |
| | DDRHSSPI1_SDATA0 | | DDR HSSPI serial data I/O pin |
| | EINT1_3 | | External interrupt ch.1 input pin_3 |
| | MFS2_SOT_0 | | Multi-function serial ch.2 serial data output pin_0 |
| | MFS9_SOT_2 | | Multi-function serial ch.9 serial data output pin_2 |
| 28 | P0_14 | M | GPIO port |
| | DDRHSSPI1_SDATA2 | | DDR HSSPI serial data I/O pin |
| | EINT2_3 | | External interrupt ch.2 input pin_3 |
| | MFS2_SCK_0 | | Multi-function serial ch.2 clock I/O pin_0 |
| | MFS9_SCK_2 | | Multi-function serial ch.9 clock I/O pin_2 |
| 29 | P0_15 | M | GPIO port |
| | DDRHSSPI1_SDATA1 | | DDR HSSPI serial data I/O pin |
| | EINT2_0 | | External interrupt ch.2 input pin_0 |
| | MFS2_SIN_0 | | Multi-function serial ch.2 serial data input pin_0 |
| | MFS9_SIN_2 | | Multi-function serial ch.9 serial data input pin_2 |
| 30 | P0_16 | M | GPIO port |
| | DDRHSSPI1_SSEL | | DDR HSSPI select output pin |
| | EINT3_3 | | External interrupt ch.3 input pin_3 |
| | MFS2_CS0_0 | | Multi-function serial ch.2 serial chip select 0 I/O pin_0 |
| | MFS9_CS0_2 | | Multi-function serial ch.9 serial chip select 0 I/O pin_2 |
| 31 | P0_17 | M | GPIO port |
| | DDRHSSPI1_SDATA3 | | DDR HSSPI serial data I/O pin |
| | EINT4_3 | | External interrupt ch.4 input pin_3 |
| | MFS2_CS1_0 | | Multi-function serial ch.2 serial chip select 1 output pin_0 |
| | MFS9_CS1_2 | | Multi-function serial ch.9 serial chip select 1 output pin_2 |
| 32 | VCC53_2 | - | +3.3 V/+5.0 V selection power supply pin (2) |
| 33 | VSS | - | GND |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 34 | P0_18 | M | GPIO port |
| | DDRHSSPI0_SCLK | | DDR HSSPI serial clock output pin |
| | EINT5_3 | | External interrupt ch.5 input pin_3 |
| | MFS2_CS2_0 | | Multi-function serial ch.2 serial chip select 2 output pin_0 |
| 35 | VSS | - | GND |
| 36 | P0_19 | M | GPIO port |
| | DDRHSSPI0_SDATA0 | | DDR HSSPI serial data I/O pin |
| | EINT6_3 | | External interrupt ch.6 input pin_3 |
| | MFS2_CS3_0 | | Multi-function serial ch.2 serial chip select 3 output pin_0 |
| | MFS8_SOT_2 | | Multi-function serial ch.8 serial data output pin_2 |
| 37 | P0_20 | M | GPIO port |
| | DDRHSSPI0_SDATA2 | | DDR HSSPI serial data I/O pin |
| | EINT7_3 | | External interrupt ch.7 input pin_3 |
| | MFS3_SOT_0 | | Multi-function serial ch.3 serial data output pin_0 |
| | MFS8_SCK_2 | | Multi-function serial ch.8 clock I/O pin_2 |
| 38 | P0_21 | M | GPIO port |
| | DDRHSSPI0_SDATA1 | | DDR HSSPI serial data I/O pin |
| | EINT8_3 | | External interrupt ch.8 input pin_3 |
| | MFS3_SCK_0 | | Multi-function serial ch.3 clock I/O pin_0 |
| | MFS8_SIN_2 | | Multi-function serial ch.8 serial data input pin_2 |
| 39 | P0_22 | M | GPIO port |
| | DDRHSSPI0_SSEL | | DDR HSSPI select output pin |
| | ADC0_AN0 | | ADC ch.0 analog input pin |
| | EINT3_0 | | External interrupt ch.3 input pin_0 |
| | MFS3_SIN_0 | | Multi-function serial ch.3 serial data input pin_0 |
| | MFS8_CS0_2 | | Multi-function serial ch.8 serial chip select 0 I/O pin_2 |
| 40 | P0_23 | M | GPIO port |
| | DDRHSSPI0_SDATA3 | | DDR HSSPI serial data I/O pin |
| | ADC0_AN1 | | ADC ch.1 analog input pin |
| | EINT9_3 | | External interrupt ch.9 input pin_3 |
| | MFS3_CS0_0 | | Multi-function serial ch.3 serial chip select 0 I/O pin_0 |
| 41 | VCC53_2 | - | +3.3 V/ +5.0 V selection power supply pin (2) |
| 42 | VSS | - | GND |
| 43 | P0_24 | M | GPIO port |
| | ADC0_AN2 | | ADC ch.2 analog input pin |
| | EINT10_3 | | External interrupt ch.10 input pin_3 |
| | MFS3_CS1_0 | | Multi-function serial ch.3 serial chip select 1 output pin_0 |
| 44 | VCC53_2 | - | +3.3 V/+5.0 V selection power supply pin (2) |
| 45 | VSS | - | GND |
| 46 | X1 | K | Main clock oscillation output pin |
| 47 | X0 | K | Main clock oscillation input pin |
| 48 | MODE | G | Mode pin |
| 49 | RSTX | H | External reset input pin |
| 50 | JTAG_NTRST | D | JTAG test reset input pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 51 | JTAG_TDO | F | JTAG test data output pin |
| 52 | JTAG_TDI | E | JTAG test data input pin |
| 53 | JTAG_TCK | E | JTAG test clock input pin |
| 54 | JTAG_TMS | E | JTAG test mode state input pin |
| 55 | C | - | External capacity connection output pin |
| 56 | VSS | - | GND |
| 57 | VCC5 | - | +5.0 V power supply pin |
| 58 | P3_08 | A | GPIO port |
| | EINT18_1 | | External interrupt ch.18 input pin_1 |
| | SG0_SGA_1 | | Sound generator ch.0 SGA output pin_1 |
| | BT6_TIOA12_1 | | Base timer6 ch.12 TIOA output pin_1 |
| | OCU0_OUT0_1 | | Output compare0 ch.0 output pin_1 |
| | ICU0_IN0_1 | | Input capture0 ch.0 input pin_1 |
| | RLT0_TIN_1 | | Reload timer ch.0 event input pin_1 |
| | MFS8_SOT_1 | | Multi-function serial ch.8 serial data output pin_1 |
| | TRACE0_1 | | Trace data 0 output pin_1 |
| 59 | P3_09 | A | GPIO port |
| | EINT6_1 | | External interrupt ch.6 input pin_1 |
| | SG0_SGO_1 | | Sound generator ch.0 SGO output pin_1 |
| | BT6_TIOA13_1 | | Base timer6 ch.13 TIOA output pin_1 |
| | OCU0_OUT1_1 | | Output compare0 ch.1 output pin_1 |
| | ICU0_IN1_1 | | Input capture0 ch.1 input pin_1 |
| | RLT0_TOT_1 | | Reload timer ch.0 output pin_1 |
| | CAN0_RX_1 | | CAN ch.0 reception data input pin_1 |
| | MFS8_SCK_1 | | Multi-function serial ch.8 clock I/O pin_1 |
| | TRACE1_1 | | Trace data 1 output pin_1 |
| 60 | P3_10 | A | GPIO port |
| | EINT17_3 | | External interrupt ch.17 input pin_3 |
| | SG1_SGA_1 | | Sound generator ch.1 SGA output pin_1 |
| | BT7_TIOA14_1 | | Base timer7 ch.14 TIOA output pin_1 |
| | OCU1_OUT0_1 | | Output compare1 ch.0 output pin_1 |
| | ICU1_IN0_1 | | Input capture1 ch.0 input pin_1 |
| | RLT1_TIN_1 | | Reload timer ch.1 event input pin_1 |
| | CAN0_TX_1 | | CAN ch.0 transmission data output pin_1 |
| | MFS8_SIN_1 | | Multi-function serial ch.8 serial data input pin_1 |
| | TRACE2_1 | | Trace data 2 output pin_1 |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 61 | P3_11 | A | GPIO port |
| | ADC0_AN3 | | ADC ch.3 analog input pin |
| | EINT8_1 | | External interrupt ch.8 input pin_1 |
| | SG1_SGO_1 | | Sound generator ch.1 SGO output pin_1 |
| | BT7_TIOA15_1 | | Base timer7 ch.15 TIOA output pin_1 |
| | OCU1_OUT1_1 | | Output compare1 ch.1 output pin_1 |
| | ICU1_IN1_1 | | Input capture1 ch.1 input pin_1 |
| | RLT1_TOT_1 | | Reload timer ch.1 output pin_1 |
| | CAN1_RX_1 | | CAN ch.1 reception data input pin_1 |
| | MFS10_SOT_1 | | Multi-function serial ch.10 serial data output pin_1 |
| | TRACE3_1 | | Trace data 3 output pin_1 |
| 62 | P3_12 | A | GPIO port |
| | ADC0_AN4 | | ADC ch.4 analog input pin |
| | EINT21_1 | | External interrupt ch.21 input pin_1 |
| | SG2_SGA_1 | | Sound generator ch.2 SGA output pin_1 |
| | BT8_TIOA16_1 | | Base timer8 ch.16 TIOA output pin_1 |
| | OCU2_OUT0_1 | | Output compare2 ch.0 output pin_1 |
| | ICU2_IN0_1 | | Input capture2 ch.0 input pin_1 |
| | RLT16_TIN_1 | | Reload timer ch.16 event input pin_1 |
| | CAN1_TX_1 | | CAN ch.1 transmission data output pin_1 |
| | MFS10_SCK_1 | | Multi-function serial ch.10 clock I/O pin_1 |
| | TRACE_CLK_1 | | Trace clock output pin_1 |
| 63 | P3_13 | A | GPIO port |
| | ADC0_AN5 | | ADC ch.5 analog input pin |
| | EINT18_3 | | External interrupt ch.18 input pin_3 |
| | SG2_SGO_1 | | Sound generator ch.2 SGO output pin_1 |
| | BT8_TIOA17_1 | | Base timer8 ch.17 TIOA output pin_1 |
| | OCU2_OUT1_1 | | Output compare2 ch.1 output pin_1 |
| | ICU2_IN1_1 | | Input capture2 ch.1 input pin_0 |
| | RLT16_TOT_1 | | Reload timer ch.16 output pin_1 |
| | MFS10_SIN_1 | | Multi-function serial ch.10 serial data input pin_1 |
| | TRACE_CTL_1 | | Trace control output pin_1 |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 64 | P0_25 | A | GPIO port |
| | ADC0_AN6 | | ADC ch.6 analog input pin |
| | EINT4_0 | | External interrupt ch.4 input pin_0 |
| | PCMP0_BL_0 | | PCM_PWM ch.0 BL output pin_0 |
| | BT0_TIOA0_0 | | Base timer0 ch.0 TIOA output pin_0 |
| | OCU0_OUT0_0 | | Output compare0 ch.0 output pin_0 |
| | ICU0_IN0_0 | | Input capture0 ch.0 input pin_0 |
| | QPRC8_AIN | | Quadrature position and revolution counter ch.8 AIN input pin |
| | RLT0_TIN_0 | | Reload timer ch.0 event input pin_0 |
| | FRT0/1/2/3_TEXT | | Free-run timer ch.0/1/2/3 clock input pin |
| | CAN0_RX_0 | | CAN ch.0 reception data input pin_0 |
| | MFS8_SOT_0 | | Multi-function serial ch.8 serial data output pin_0 |
| | MFS0_SDA | | I ² C ch.0 serial data I/O pin |
| | PWU_AN0 | | Partial wakeup ADC analog 0 input pin |
| 65 | P0_26 | A | GPIO port |
| | ADC0_AN7 | | ADC ch.7 analog input pin |
| | EINT5_0 | | External interrupt ch.5 input pin_0 |
| | PCMP0_BH_0 | | PCM_PWM ch.0 BH output pin_0 |
| | BT0_TIOA1_0 | | Base timer0 ch.1 TIOA output pin_0 |
| | OCU0_OUT1_0 | | Output compare0 ch.1 output pin_0 |
| | ICU0_IN1_0 | | Input capture0 ch.1 input pin_0 |
| | QPRC8_BIN | | Quadrature position and revolution counter ch.8 BIN input pin |
| | RLT0_TOT_0 | | Reload timer ch.0 output pin_0 |
| | FRT4/8/9/10_TEXT | | Free-run timer ch.4/8/9/10 clock input pin |
| | CAN0_TX_0 | | CAN ch.0 transmission data output pin_0 |
| | MFS8_SCK_0 | | Multi-function serial ch.8 clock I/O pin_0 |
| | MFS0_SCL | | I ² C ch.0 clock I/O pin |
| | PWU_AN1 | | Partial wakeup ADC analog 1 input pin |
| 66 | P0_27 | A | GPIO port |
| | ADC0_AN8 | | ADC ch.8 analog input pin |
| | EINT6_0 | | External interrupt ch.6 input pin_0 |
| | PCMP0_AL_0 | | PCM_PWM ch.0 AL output pin_0 |
| | SG0_SGA_0 | | Sound generator ch.0 SGA output pin_0 |
| | BT1_TIOA2_0 | | Base timer1 ch.2 TIOA output pin_0 |
| | ICU1_IN0_0 | | Input capture1 ch.0 input pin_0 |
| | QPRC8_ZIN | | Quadrature position and revolution counter ch.8 ZIN input pin |
| | RLT1_TIN_0 | | Reload timer ch.1 event input pin_0 |
| | CAN1_RX_0 | | CAN ch.1 reception data input pin_0 |
| | MFS8_SIN_0 | | Multi-function serial ch.8 serial data input pin_0 |
| | PWU_AN2 | | Partial wakeup ADC analog 2 input pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 67 | P0_28 | A | GPIO port |
| | ADC0_AN9 | | ADC ch.9 analog input pin |
| | EINT7_0 | | External interrupt ch.7 input pin_0 |
| | PCMP0_AH_0 | | PCM_PWM ch.0 AH output pin_0 |
| | SG0_SGO_0 | | Sound generator ch.0 SGO output pin_0 |
| | BT1_TIOA3_0 | | Base timer1 ch.3 TIOA output pin_0 |
| | ICU1_IN1_0 | | Input capture1 ch.1 input pin_0 |
| | QPRC9_AIN | | Quadrature position and revolution counter ch.9 AIN input pin |
| | RLT1_TOT_0 | | Reload timer ch.1 output pin_0 |
| | CAN1_TX_0 | | CAN ch.1 transmission data output pin_0 |
| | MFS8_CS0_0 | | Multi-function serial ch.8 serial chip select 0 I/O pin_0 |
| | PWUTRG_0 | | Partial wakeup trigger output pin_0 |
| | 68 | | P0_29 |
| ADC0_AN10 | | ADC ch.10 analog input pin | |
| EINT12_1 | | External interrupt ch.12 input pin_1 | |
| BT9_TIOA18_1 | | Base timer9 ch.18 TIOA output pin_1 | |
| OCU8_OUT0_1 | | Output compare8 ch.0 output pin_1 | |
| ICU8_IN0_1 | | Input capture8 ch.0 input pin_1 | |
| RLT17_TIN_1 | | Reload timer ch.17 event input pin_1 | |
| MFS10_CS0_1 | | Multi-function serial ch.10 serial chip select 0 I/O pin_1 | |
| 69 | NMIX | I | Non-maskable interrupt input pin |
| 70 | X0A | L | Sub clock oscillation input pin |
| | P0_30 | | GPIO port |
| | EINT8_0 | | External interrupt ch.8 input pin_0 |
| | BT4_TIOA8_0 | | Base timer4 ch.8 TIOA output pin_0 |
| | OCU8_OUT0_0 | | Output compare8 ch.0 output pin_0 |
| | ICU9_IN0_0 | | Input capture9 ch.0 input pin_0 |
| | RLT17_TIN_0 | | Reload timer ch.17 event input pin_0 |
| | MFS6_CS0_0 | | Multi-function serial ch.6 serial chip select 0 I/O pin_0 |
| 71 | X1A | L | Sub clock oscillation output pin |
| | P0_31 | | GPIO port |
| | EINT9_0 | | External interrupt ch.9 input pin_0 |
| | BT4_TIOA9_0 | | Base timer4 ch.9 TIOA output pin_0 |
| | OCU8_OUT1_0 | | Output compare8 ch.1 output pin_0 |
| | ICU9_IN1_0 | | Input capture9 ch.1 input pin_0 |
| | RLT17_TOT_0 | | Reload timer ch.17 output pin_0 |
| | MFS6_CS1_0 | | Multi-function serial ch.6 serial chip select 1 output pin_0 |
| 72 | VSS | - | GND |
| 73 | VCC5 | - | +5.0 V power supply pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 74 | P1_00 | A | GPIO port |
| | ADC0_AN11 | | ADC ch.11 analog input pin |
| | EINT10_0 | | External interrupt ch.10 input pin_0 |
| | PCMP1_BL_0 | | PCM_PWM ch.1 BL output pin_0 |
| | SG1_SGA_0 | | Sound generator ch.1 SGA output pin_0 |
| | BT2_TIOA4_0 | | Base timer2 ch.4 TIOA output pin_0 |
| | OCU1_OUT0_0 | | Output compare1 ch.0 output pin_0 |
| | ICU2_IN0_0 | | Input capture2 ch.0 input pin_0 |
| | QPRC9_BIN | | Quadrature position and revolution counter ch.9 BIN input pin |
| | RLT16_TIN_0 | | Reload timer ch.16 event input pin_0 |
| | CAN2_RX_0 | | CAN ch.2 reception data input pin_0 |
| | IND0_OUT_0 | | Indicator PWM output pin_0 |
| | TRACE0_0 | | Trace data 0 output pin_0 |
| | 75 | | P1_01 |
| ADC0_AN12 | | ADC ch.12 analog input pin | |
| EINT11_0 | | External interrupt ch.11 input pin_0 | |
| PCMP1_BH_0 | | PCM_PWM ch.1 BH output pin_0 | |
| SG1_SGO_0 | | Sound generator ch.1 SGO output pin_0 | |
| BT2_TIOA5_0 | | Base timer2 ch.5 TIOA output pin_0 | |
| OCU1_OUT1_0 | | Output compare1 ch.1 output pin_0 | |
| ICU2_IN1_0 | | Input capture2 ch.1 input pin_0 | |
| QPRC9_ZIN | | Quadrature position and revolution counter ch.9 ZIN input pin | |
| RLT16_TOT_0 | | Reload timer ch.16 output pin_0 | |
| CAN2_TX_0 | | CAN ch.2 transmission data output pin_0 | |
| TRACE1_0 | | Trace data 1 output pin_0 | |
| PWU_AN3 | | Partial wakeup ADC analog 3 input pin | |
| 76 | | P1_02 | C |
| | ADC0_AN13 | ADC ch.13 analog input pin | |
| | EINT12_0 | External interrupt ch.12 input pin_0 | |
| | PCMP1_AL_0 | PCM_PWM ch.1 AL output pin_0 | |
| | SG2_SGA_0 | Sound generator ch.2 SGA output pin_0 | |
| | BT3_TIOA6_0 | Base timer3 ch.6 TIOA output pin_0 | |
| | OCU2_OUT0_0 | Output compare2 ch.0 output pin_0 | |
| | ICU8_IN0_0 | Input capture8 ch.0 input pin_0 | |
| | MFS6_SOT_0 | Multi-function serial ch.6 serial data output pin_0 | |
| | MFS6_SDA | I ² C ch.6 serial data I/O pin | |
| | TRACE2_0 | Trace data 2 output pin_0 | |
| | PWU_AN4 | Partial wakeup ADC analog 4 input pin | |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 77 | P1_03 | C | GPIO port |
| | ADC0_AN14 | | ADC ch.14 analog input pin |
| | EINT19_3 | | External interrupt ch.19 input pin_3 |
| | PCMP1_AH_0 | | PCM_PWM ch.1 AH output pin_0 |
| | SG2_SGO_0 | | Sound generator ch.2 SGO output pin_0 |
| | BT3_TIOA7_0 | | Base timer3 ch.7 TIOA output pin_0 |
| | OCU2_OUT1_0 | | Output compare2 ch.1 output pin_0 |
| | ICU8_IN1_0 | | Input capture8 ch.1 input pin_0 |
| | MFS6_SCK_0 | | Multi-function serial ch.6 clock I/O pin_0 |
| | MFS6_SCL | | I ² C ch.6 clock I/O pin |
| | TRACE3_0 | | Trace data 3 output pin_0 |
| | PWU_AN5 | | Partial wakeup ADC analog 5 input pin |
| | 78 | | P1_04 |
| ADC0_AN15 | | ADC ch.15 analog input pin | |
| EINT13_0 | | External interrupt ch.13 input pin_0 | |
| SG3_SGA_0 | | Sound generator ch.3 SGA output pin_0 | |
| BT9_TIOA19_1 | | Base timer9 ch.19 TIOA output pin_1 | |
| OCU8_OUT1_1 | | Output compare8 ch.1 output pin_1 | |
| ICU8_IN1_1 | | Input capture8 ch.1 input pin_1 | |
| RLT17_TOT_1 | | Reload timer ch.17 output pin_1 | |
| MFS6_SIN_0 | | Multi-function serial ch.6 serial data input pin_0 | |
| TRACE_CLK_0 | | Trace clock output pin_0 | |
| PWU_AN6 | | Partial wakeup ADC analog 6 input pin | |
| 79 | P1_05 | C | GPIO port |
| | ADC0_AN16 | | ADC ch.16 analog input pin |
| | EINT14_0 | | External interrupt ch.14 input pin_0 |
| | SG3_SGO_0 | | Sound generator ch.3 SGO output pin_0 |
| | BT0_TIOB0/BT1_TIOB2/BT2_TIOB4/BT3_TIOB6/BT4_TIOB8/BT5_TIOB10_1 | | Base timer0/1/2/3/4/5 ch.0/2/4/6/8/10 TIOB input pin_1 |
| | OCU9_OUT0_1 | | Output compare9 ch.0 output pin_1 |
| | ICU9_IN0_1 | | Input capture9 ch.0 input pin_1 |
| | RLT2_TIN_1 | | Reload timer ch.2 event input pin_1 |
| | CAN3_RX_0 | | CAN ch.3 reception data input pin_0 |
| | MFS7_SOT_0 | | Multi-function serial ch.7 serial data output pin_0 |
| | MFS7_SDA | | I ² C ch.7 serial data I/O pin |
| | TRACE_CTL_0 | | Trace control output pin_0 |
| | PWU_AN7 | | Partial wakeup ADC analog 7 input pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 80 | P1_06 | C | GPIO port |
| | ADC0_AN17 | | ADC ch.17 analog input pin |
| | EINT14_1 | | External interrupt ch.14 input pin_1 |
| | SG4_SGA_0 | | Sound generator ch.4 SGA output pin_0 |
| | BT6_TIOB12/BT7_TIOB14/BT8_TIOB16/BT9_TIOB18/BT10_TIOB20/BT11_TIOB22_1 | | Base timer6/7/8/9/10/11 ch.12/14/16/18/20/22 TIOB input pin_1 |
| | OCU9_OUT1_1 | | Output compare9 ch.1 output pin_1 |
| | ICU9_IN1_1 | | Input capture9 ch.1 input pin_1 |
| | RLT2_TOT_1 | | Reload timer ch.2 output pin_1 |
| | CAN3_TX_0 | | CAN ch.3 transmission data output pin_0 |
| | MFS7_SCK_0 | | Multi-function serial ch.7 clock I/O pin_0 |
| | MFS7_SCL | | I ² C ch.7 clock I/O pin |
| 81 | P1_07 | A | GPIO port |
| | ADC0_AN18 | | ADC ch.18 analog input pin |
| | EINT15_0 | | External interrupt ch.15 input pin_0 |
| | SG4_SGO_0 | | Sound generator ch.4 SGO output pin_0 |
| | BT5_TIOA10_0 | | Base timer5 ch.10 TIOA output pin_0 |
| | OCU9_OUT0_0 | | Output compare9 ch.0 output pin_0 |
| | ICU10_IN0_0 | | Input capture10 ch.0 input pin_0 |
| | RLT2_TOT_0 | | Reload timer ch.2 output pin_0 |
| | MFS7_SIN_0 | | Multi-function serial ch.7 serial data input pin_0 |
| | SYSC0_CLK_1 | | System clock output pin_1 |
| 82 | P3_14 | A | GPIO port |
| | ADC0_AN19 | | ADC ch.19 analog input pin |
| | EINT1_4 | | External interrupt ch.1 input pin_4 |
| | CAN2_RX_1 | | CAN ch.2 reception data input pin_1 |
| 83 | P3_15 | A | GPIO port |
| | ADC0_AN20 | | ADC ch.20 analog input pin |
| | EINT20_1 | | External interrupt ch.20 input pin_1 |
| | BT11_TIOA22_1 | | Base timer11 ch.22 TIOA output pin_1 |
| | OCU10_OUT0_1 | | Output compare10 ch.0 output pin_1 |
| | ICU10_IN0_1 | | Input capture10 ch.0 input pin_1 |
| | CAN2_TX_1 | | CAN ch.2 transmission data output pin_1 |
| 84 | AVCC5 | - | Analog power supply pin |
| 85 | AVSS | - | Analog GND pin |
| 86 | AVRL5 | - | ADC low reference voltage pin |
| 87 | AVRH5 | - | ADC high reference voltage pin |
| 88 | VCC5 | - | +5.0 V power supply pin |
| 89 | VSS | A | GND |
| 90 | P3_16 | A | GPIO port |
| | EINT0_4 | | External interrupt ch.0 input pin_4 |
| | OCU9_OUT1_0 | | Output compare9 ch.1 output pin_0 |
| | RLT2_TIN_0 | | Reload timer ch.2 event input pin_0 |
| | MFS9_SOT_1 | | Multi-function serial ch.9 serial data output pin_1 |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 91 | P3_17 | A | GPIO port |
| | EINT17_1 | | External interrupt ch.17 input pin_1 |
| | BT11_TIOA23_1 | | Base timer11 ch.23 TIOA output pin_1 |
| | OCU10_OUT1_1 | | Output compare10 ch.1 output pin_1 |
| | ICU10_IN1_1 | | Input capture10 ch.1 input pin_1 |
| | CAN3_RX_1 | | CAN ch.3 reception data input pin_1 |
| | MFS9_SCK_1 | | Multi-function serial ch.9 clock I/O pin_1 |
| 92 | P3_18 | A | GPIO port |
| | EINT2_4 | | External interrupt ch.2 input pin_4 |
| | BT10_TIOA21_1 | | Base timer10 ch.21 TIOA output pin_1 |
| | RLT3_TIN_1 | | Reload timer ch.3 event input pin_1 |
| | CAN3_TX_1 | | CAN ch.3 transmission data output pin_1 |
| | MFS9_SIN_1 | | Multi-function serial ch.9 serial data input pin_1 |
| 93 | P3_19 | A | GPIO port |
| | EINT3_4 | | External interrupt ch.3 input pin_4 |
| | SG3_SGA_1 | | Sound generator ch.3 SGA output pin_1 |
| | RLT3_TOT_1 | | Reload timer ch.3 output pin_1 |
| | MFS9_CS0_1 | | Multi-function serial ch.9 serial chip select 0 I/O pin_1 |
| 94 | P3_20 | A | GPIO port |
| | EINT19_1 | | External interrupt ch.19 input pin_1 |
| | SG3_SGO_1 | | Sound generator ch.3 SGO output pin_1 |
| | MFS9_CS1_1 | | Multi-function serial ch.9 serial chip select 1 output pin_1 |
| 95 | P3_21 | A | GPIO port |
| | ADC0_AN21 | | ADC ch.21 analog input pin |
| | EINT4_4 | | External interrupt ch.4 input pin_4 |
| | MFS5_SOT_1 | | Multi-function serial ch.5 serial data output pin_1 |
| | PWUTRG_1 | | Partial wakeup trigger output pin_1 |
| 96 | P1_08 | A | GPIO port |
| | ADC0_TRG0_1 | | ADC external trigger ch.0 input pin_1 |
| | EINT16_0 | | External interrupt ch.16 input pin_0 |
| | BT5_TIOA11_0 | | Base timer5 ch.11 TIOA output pin_0 |
| | OCU10_OUT0_0 | | Output compare10 ch.0 output pin_0 |
| | ICU10_IN1_0 | | Input capture10 ch.1 input pin_0 |
| | RLT3_TIN_0 | | Reload timer ch.3 event input pin_0 |
| | MFS7_CS0_0 | | Multi-function serial ch.7 serial chip select 0 I/O pin_0 |
| | MFS5_SCK_1 | | Multi-function serial ch.5 clock I/O pin_1 |
| | IND0_OUT_1 | | Indicator PWM output pin_1 |
| 97 | P3_22 | A | GPIO port |
| | ADC0_AN22 | | ADC ch.22 analog input pin |
| | EINT5_4 | | External interrupt ch.5 input pin_4 |
| | SG4_SGA_1 | | Sound generator ch.4 SGA output pin_1 |
| | MFS5_SIN_1 | | Multi-function serial ch.5 serial data input pin_1 |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 98 | P3_23 | A | GPIO port |
| | ADC0_AN23 | | ADC ch.23 analog input pin |
| | EINT6_4 | | External interrupt ch.6 input pin_4 |
| | SG4_SGO_1 | | Sound generator ch.4 SGO output pin_1 |
| | MFS5_CS0_1 | | Multi-function serial ch.5 serial chip select 0 I/O pin_1 |
| 99 | VSS | - | GND |
| 100 | VCC5 | - | +5.0 V power supply pin |
| 101 | P1_09 | A | GPIO port |
| | ADC0_TRG0_0 | | ADC external trigger ch.0 input pin_0 |
| | EINT9_4 | | External interrupt ch.9 input pin_4 |
| | BT0_TIOB0/BT1_TIOB2/BT2_TIOB4/BT3_TIOB6/BT4_TIOB8/BT5_TIOB10_0 | | Base timer0/1/2/3/4/5 ch.0/2/4/6/8/10 TIOB input pin_0 |
| | OCU10_OUT1_0 | | Output compare10 ch.1 output pin_0 |
| | RLT3_TOT_0 | | Reload timer ch.3 output pin_0 |
| | MFS7_CS1_0 | | Multi-function serial ch.7 serial chip select 1 output pin_0 |
| | RTC0_WOT | | RTC overflow output pin |
| | SYSC0_CLK_0 | | System clock output pin_0 |
| 102 | DVSS | - | SMC high current port GND pin |
| 103 | DVCC | - | SMC high current port power supply pin |
| 104 | P1_10 | O | GPIO port |
| | ADC0_AN24 | | ADC ch.24 analog input pin |
| | SMC0_PWM1P | | Stepper motor controller ch.0 PWM1P output pin |
| | EINT17_0 | | External interrupt ch.17 input pin_0 |
| | BT6_TIOA12_0 | | Base timer6 ch.12 TIOA output pin_0 |
| 105 | P1_11 | O | GPIO port |
| | ADC0_AN25 | | ADC ch.25 analog input pin |
| | SMC0_PWM1M | | Stepper motor controller ch.0 PWM1M output pin |
| | EINT11_4 | | External interrupt ch.11 input pin_4 |
| | BT6_TIOA13_0 | | Base timer6 ch.13 TIOA output pin_0 |
| 106 | P1_12 | O | GPIO port |
| | ADC0_AN26 | | ADC ch.26 analog input pin |
| | SMC0_PWM2P | | Stepper motor controller ch.0 PWM2P output pin |
| | EINT18_0 | | External interrupt ch.18 input pin_0 |
| | BT7_TIOA14_0 | | Base timer7 ch.14 TIOA output pin_0 |
| | MFS0_SOT_0 | | Multi-function serial ch.0 serial data output pin_0 |
| | MFS8_SDA | | I ² C ch.8 serial data I/O pin |
| 107 | P1_13 | O | GPIO port |
| | ADC0_AN27 | | ADC ch.27 analog input pin |
| | SMC0_PWM2M | | Stepper motor controller ch.0 PWM2M output pin |
| | EINT12_4 | | External interrupt ch.12 input pin_4 |
| | BT7_TIOA15_0 | | Base timer7 ch.15 TIOA output pin_0 |
| | MFS0_SCK_0 | | Multi-function serial ch.0 clock I/O pin_0 |
| | MFS8_SCL | | I ² C ch.8 clock I/O pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 108 | P1_14 | O | GPIO port |
| | ADC0_AN28 | | ADC ch.28 analog input pin |
| | SMC1_PWM1P | | Stepper motor controller ch.1 PWM1P output pin |
| | EINT19_0 | | External interrupt ch.19 input pin_0 |
| | BT8_TIOA16_0 | | Base timer8 ch.16 TIOA output pin_0 |
| | MFS0_SIN_0 | | Multi-function serial ch.0 serial data input pin_0 |
| 109 | P1_15 | O | GPIO port |
| | ADC0_AN29 | | ADC ch.29 analog input pin |
| | SMC1_PWM1M | | Stepper motor controller ch.1 PWM1M output pin |
| | EINT13_4 | | External interrupt ch.13 input pin_4 |
| | BT8_TIOA17_0 | | Base timer8 ch.17 TIOA output pin_0 |
| | MFS0_CS0_0 | | Multi-function serial ch.0 serial chip select 0 I/O pin_0 |
| 110 | P1_16 | O | GPIO port |
| | ADC0_AN30 | | ADC ch.30 analog input pin |
| | SMC1_PWM2P | | Stepper motor controller ch.1 PWM2P output pin |
| | EINT14_4 | | External interrupt ch.14 input pin_4 |
| | BT9_TIOA18_0 | | Base timer9 ch.18 TIOA output pin_0 |
| | MFS9_CS0_0 | | Multi-function serial ch.9 serial chip select 0 I/O pin_0 |
| 111 | P1_17 | O | GPIO port |
| | ADC0_AN31 | | ADC ch.31 analog input pin |
| | SMC1_PWM2M | | Stepper motor controller ch.1 PWM2M output pin |
| | EINT15_4 | | External interrupt ch.15 input pin_4 |
| | BT9_TIOA19_0 | | Base timer9 ch.19 TIOA output pin_0 |
| | MFS9_CS1_0 | | Multi-function serial ch.9 serial chip select 1 output pin_0 |
| 112 | DVSS | - | SMC high current port GND pin |
| 113 | DVCC | - | SMC high current port power supply pin |
| 114 | P1_18 | O | GPIO port |
| | ADC0_AN32 | | ADC ch.32 analog input pin |
| | SMC2_PWM1P | | Stepper motor controller ch.2 PWM1P output pin |
| | EINT17_4 | | External interrupt ch.17 input pin_4 |
| | BT10_TIOA20_0 | | Base timer10 ch.20 TIOA output pin_0 |
| | MFS9_SOT_0 | | Multi-function serial ch.9 serial data output pin_0 |
| | MFS9_SDA | | I ² C ch.9 serial data I/O pin |
| 115 | P1_19 | O | GPIO port |
| | ADC0_AN33 | | ADC ch.33 analog input pin |
| | SMC2_PWM1M | | Stepper motor controller ch.2 PWM1M output pin |
| | EINT18_4 | | External interrupt ch.18 input pin_4 |
| | BT10_TIOA21_0 | | Base timer10 ch.21 TIOA output pin_0 |
| | MFS9_SCK_0 | | Multi-function serial ch.9 clock I/O pin_0 |
| | MFS9_SCL | | I ² C ch.9 clock I/O pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 116 | P1_20 | O | GPIO port |
| | ADC0_AN34 | | ADC ch.34 analog input pin |
| | SMC2_PWM2P | | Stepper motor controller ch.2 PWM2P output pin |
| | EINT20_0 | | External interrupt ch.20 input pin_0 |
| | BT11_TIOA22_0 | | Base timer11 ch.22 TIOA output pin_0 |
| | MFS9_SIN_0 | | Multi-function serial ch.9 serial data input pin_0 |
| 117 | P1_21 | O | GPIO port |
| | ADC0_AN35 | | ADC ch.35 analog input pin |
| | SMC2_PWM2M | | Stepper motor controller ch.2 PWM2M output pin |
| | EINT20_4 | | External interrupt ch.20 input pin_4 |
| | BT11_TIOA23_0 | | Base timer11 ch.23 TIOA output pin_0 |
| | MFS10_SOT_0 | | Multi-function serial ch.10 serial data output pin_0 |
| | MFS10_SDA | | I ² C ch.10 serial data I/O pin |
| 118 | P1_22 | O | GPIO port |
| | ADC0_AN36 | | ADC ch.36 analog input pin |
| | SMC3_PWM1P | | Stepper motor controller ch.3 PWM1P output pin |
| | EINT21_4 | | External interrupt ch.21 input pin_4 |
| | BT6_TIOB12/BT7_TIOB14/BT8_TIOB16/BT9_TIOB18/BT10_TIOB20/BT11_TIOB22_0 | | Base timer6/7/8/9/10/11 ch.12/14/16/18/20/22 TIOB input pin_0 |
| | MFS10_SCK_0 | | Multi-function serial ch.10 clock I/O pin_0 |
| | MFS10_SCL | | I ² C ch.10 clock I/O pin |
| 119 | P1_23 | O | GPIO port |
| | ADC0_AN37 | | ADC ch.37 analog input pin |
| | SMC3_PWM1M | | Stepper motor controller ch.3 PWM1M output pin |
| | EINT21_0 | | External interrupt ch.21 input pin_0 |
| | BT12_TIOA24_0 | | Base timer12 ch.24 TIOA output pin_0 |
| | MFS10_SIN_0 | | Multi-function serial ch.10 serial data input pin_0 |
| 120 | P1_24 | O | GPIO port |
| | ADC0_AN38 | | ADC ch.38 analog input pin |
| | SMC3_PWM2P | | Stepper motor controller ch.3 PWM2P output pin |
| | EINT22_4 | | External interrupt ch.22 input pin_4 |
| | BT12_TIOA25_0 | | Base timer12 ch.25 TIOA output pin_0 |
| | MFS10_CS0_0 | | Multi-function serial ch.10 serial chip select 0 I/O pin_0 |
| 121 | P1_25 | O | GPIO port |
| | ADC0_AN39 | | ADC ch.39 analog input pin |
| | SMC3_PWM2M | | Stepper motor controller ch.3 PWM2M output pin |
| | EINT0_5 | | External interrupt ch.0 input pin_5 |
| | BT13_TIOA26_0 | | Base timer13 ch.26 TIOA output pin_0 |
| | MFS11_CS0_0 | | Multi-function serial ch.11 serial chip select 0 I/O pin_0 |
| 122 | DVSS | - | SMC high current port GND pin |
| 123 | DVCC | - | SMC high current port power supply pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 124 | P1_26 | O | GPIO port |
| | ADC0_AN40 | | ADC ch.40 analog input pin |
| | SMC4_PWM1P | | Stepper motor controller ch.4 PWM1P output pin |
| | EINT2_5 | | External interrupt ch.2 input pin_5 |
| | BT13_TIOA27_0 | | Base timer13 ch.27 TIOA output pin_0 |
| | MFS11_CS1_0 | | Multi-function serial ch.11 serial chip select 1 output pin_0 |
| 125 | P1_27 | O | GPIO port |
| | ADC0_AN41 | | ADC ch.41 analog input pin |
| | SMC4_PWM1M | | Stepper motor controller ch.4 PWM1M output pin |
| | EINT3_5 | | External interrupt ch.3 input pin_5 |
| | BT14_TIOA28_0 | | Base timer14 ch.28 TIOA output pin_0 |
| | MFS11_SOT_0 | | Multi-function serial ch.11 serial data output pin_0 |
| 126 | P1_28 | O | GPIO port |
| | ADC0_AN42 | | ADC ch.42 analog input pin |
| | SMC4_PWM2P | | Stepper motor controller ch.4 PWM2P output pin |
| | EINT4_5 | | External interrupt ch.4 input pin_5 |
| | BT14_TIOA29_0 | | Base timer14 ch.29 TIOA output pin_0 |
| | MFS11_SCK_0 | | Multi-function serial ch.11 clock I/O pin_0 |
| 127 | P1_29 | O | GPIO port |
| | ADC0_AN43 | | ADC ch.43 analog input pin |
| | SMC4_PWM2M | | Stepper motor controller ch.4 PWM2M output pin |
| | EINT22_0 | | External interrupt ch.22 input pin_0 |
| | BT15_TIOA30_0 | | Base timer15 ch.30 TIOA output pin_0 |
| | MFS11_SIN_0 | | Multi-function serial ch.11 serial data input pin_0 |
| 128 | P1_30 | O | GPIO port |
| | ADC0_AN44 | | ADC ch.44 analog input pin |
| | SMC5_PWM1P | | Stepper motor controller ch.5 PWM1P output pin |
| | EINT6_5 | | External interrupt ch.6 input pin_5 |
| | BT15_TIOA31_0 | | Base timer15 ch.31 TIOA output pin_0 |
| | MFS5_SOT_0 | | Multi-function serial ch.5 serial data output pin_0 |
| 129 | P1_31 | O | GPIO port |
| | ADC0_AN45 | | ADC ch.45 analog input pin |
| | SMC5_PWM1M | | Stepper motor controller ch.5 PWM1M output pin |
| | EINT7_5 | | External interrupt ch.7 input pin_5 |
| | BT12_TIOB24/BT13_TIOB26/BT14_TIOB28/BT15_TIOB30_0 | | Base timer12/13/14/15 ch.24/26/28/30 TIOB input pin_0 |
| | MFS5_SCK_0 | | Multi-function serial ch.5 clock I/O pin_0 |
| | MFS5_SCL | | I ² C ch.5 clock I/O pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 130 | P2_00 | O | GPIO port |
| | ADC0_AN46 | | ADC ch.46 analog input pin |
| | SMC5_PWM2P | | Stepper motor controller ch.5 PWM2P output pin |
| | EINT23_0 | | External interrupt ch.23 input pin_0 |
| | MFS5_SIN_0 | | Multi-function serial ch.5 serial data input pin_0 |
| 131 | P2_01 | O | GPIO port |
| | ADC0_AN47 | | ADC ch.47 analog input pin |
| | SMC5_PWM2M | | Stepper motor controller ch.5 PWM2M output pin |
| | EINT9_5 | | External interrupt ch.9 input pin_5 |
| | MFS5_CS0_0 | | Multi-function serial ch.5 serial chip select 0 I/O pin_0 |
| 132 | DVSS | - | SMC high current port GND pin |
| 133 | DVCC | - | SMC high current port power supply pin |
| 134 | P3_24 | A | GPIO port |
| 135 | P3_25 | A | GPIO port |
| 136 | VSS | - | GND |
| 137 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 138 | P3_26 | A | GPIO port |
| 139 | P3_27 | A | GPIO port |
| 140 | P3_28 | A | GPIO port |
| | MFS2_CS2_1 | | Multi-function serial ch.2 serial chip select 2 output pin_1 |
| 141 | P3_29 | A | GPIO port |
| | MFS2_CS3_1 | | Multi-function serial ch.2 serial chip select 3 output pin_1 |
| 142 | P2_02 | Q | GPIO port |
| | LCD0_V3 | | LCD controller reference voltage V3 input pin |
| | EINT2_1 | | External interrupt ch.2 input pin_1 |
| 143 | P2_03 | A | GPIO port |
| | MRDY | | External bus interface ready input pin |
| | LCD0_V2 | | LCD controller reference voltage V2 input pin |
| | EINT10_5 | | External interrupt ch.10 input pin_5 |
| 144 | P2_04 | A | GPIO port |
| | I2S0_ECLK_1 | | I2S ch.0 external clock input pin_1 |
| | MDATA8 | | External bus interface data I/O pin |
| | LCD0_V1 | | LCD controller reference voltage V1 input pin |
| | EINT11_5 | | External interrupt ch.11 input pin_5 |
| | BT12_TIOA24_1 | | Base timer12 ch.24 TIOA output pin_1 |
| | MFS2_SOT_1 | | Multi-function serial ch.2 serial data output pin_1 |
| 145 | P2_05 | A | GPIO port |
| | I2S0_SD_1 | | I2S ch.0 serial data I/O pin_1 |
| | MDATA9 | | External bus interface data I/O pin |
| | LCD0_V0 | | LCD controller reference voltage V0 input pin |
| | EINT12_5 | | External interrupt ch.12 input pin_5 |
| | BT12_TIOA25_1 | | Base timer12 ch.25 TIOA output pin_1 |
| | MFS2_SCK_1 | | Multi-function serial ch.2 clock I/O pin_1 |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 146 | P2_06 | P | GPIO port |
| | I2S0_WS_1 | | I2S ch.0 word select pin_1 |
| | MDATA10 | | External bus interface data I/O pin |
| | LCD0_COM3 | | LCD controller common output pin |
| | EINT13_5 | | External interrupt ch.13 input pin_5 |
| | BT13_TIOA26_1 | | Base timer13 ch.26 TIOA output pin_1 |
| | MFS2_SIN_1 | | Multi-function serial ch.2 serial data input pin_1 |
| 147 | P2_07 | P | GPIO port |
| | I2S0_SCK_1 | | I2S ch.0 serial clock pin_1 |
| | MDATA11 | | External bus interface data I/O pin |
| | LCD0_COM2 | | LCD controller common output pin |
| | EINT14_5 | | External interrupt ch.14 input pin_5 |
| | BT13_TIOA27_1 | | Base timer13 ch.27 TIOA output pin_1 |
| | MFS2_CS0_1 | | Multi-function serial ch.2 serial chip select 0 I/O pin_1 |
| 148 | P2_08 | P | GPIO port |
| | MCSX0 | | External bus interface chip select output pin |
| | LCD0_COM1 | | LCD controller common output pin |
| | EINT15_5 | | External interrupt ch.15 input pin_5 |
| | BT14_TIOA28_1 | | Base timer14 ch.28 TIOA output pin_1 |
| | MFS2_CS1_1 | | Multi-function serial ch.2 serial chip select 1 output pin_1 |
| 149 | VSS | - | GND |
| 150 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 151 | P2_09 | P | GPIO port |
| | MDATA12 | | External bus interface data I/O pin |
| | LCD0_COM0 | | LCD controller common output pin |
| | EINT3_1 | | External interrupt ch.3 input pin_1 |
| | BT14_TIOA29_1 | | Base timer14 ch.29 TIOA output pin_1 |
| | MFS3_SOT_1 | | Multi-function serial ch.3 serial data output pin_1 |
| 152 | P2_10 | P | GPIO port |
| | MDATA13 | | External bus interface data I/O pin |
| | LCD0_SEG31 | | LCD controller segment output pin |
| | EINT16_5 | | External interrupt ch.16 input pin_5 |
| | SG0_SGA_2 | | Sound generator ch.0 SGA output pin_2 |
| | BT15_TIOA30_1 | | Base timer15 ch.30 TIOA output pin_1 |
| | MFS3_SCK_1 | | Multi-function serial ch.3 clock I/O pin_1 |
| 153 | P2_11 | P | GPIO port |
| | MDATA14 | | External bus interface data I/O pin |
| | LCD0_SEG30 | | LCD controller segment output pin |
| | EINT17_5 | | External interrupt ch.17 input pin_5 |
| | SG0_SGO_2 | | Sound generator ch.0 SGO output pin_2 |
| | BT15_TIOA31_1 | | Base timer15 ch.31 TIOA output pin_1 |
| | MFS3_SIN_1 | | Multi-function serial ch.3 serial data input pin_1 |

| TEQFP176 | | | |
|----------|---|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 154 | P2_12 | P | GPIO port |
| | MDATA15 | | External bus interface data I/O pin |
| | LCD0_SEG29 | | LCD controller segment output pin |
| | EINT18_5 | | External interrupt ch.18 input pin_5 |
| | SG1_SGA_2 | | Sound generator ch.1 SGA output pin_2 |
| | BT12_TIOB24/BT13_TIOB26/BT14_TIOB28/BT15_TIOB30_1 | | Base timer12/13/14/15 ch.24/26/28/30 TIOB input pin_1 |
| | MFS3_CS0_1 | | Multi-function serial ch.3 serial chip select 0 I/O pin_1 |
| 155 | P2_13 | P | GPIO port |
| | MCSX1 | | External bus interface chip select output pin |
| | LCD0_SEG28 | | LCD controller segment output pin |
| | EINT19_5 | | External interrupt ch.19 input pin_5 |
| | SG1_SGO_2 | | Sound generator ch.1 SGO output pin_2 |
| | MFS3_CS1_1 | | Multi-function serial ch.3 serial chip select 1 output pin_1 |
| 156 | P2_14 | P | GPIO port |
| | MDATA0 | | External bus interface data I/O pin |
| | LCD0_SEG27 | | LCD controller segment output pin |
| | EINT20_5 | | External interrupt ch.20 input pin_5 |
| | MFS3_CS2_1 | | Multi-function serial ch.3 serial chip select 2 output pin_1 |
| 157 | P2_15 | P | GPIO port |
| | MDATA1 | | External bus interface data I/O pin |
| | LCD0_SEG26 | | LCD controller segment output pin |
| | EINT21_5 | | External interrupt ch.21 input pin_5 |
| | MFS3_CS3_1 | | Multi-function serial ch.3 serial chip select 3 output pin_1 |
| | LCDD0 | | LCD bus interface data I/O pin |
| 158 | P2_16 | P | GPIO port |
| | MDATA2 | | External bus interface data I/O pin |
| | LCD0_SEG25 | | LCD controller segment output pin |
| | EINT22_5 | | External interrupt ch.22 input pin_5 |
| | MFS4_SOT_0 | | Multi-function serial ch.4 serial data output pin_0 |
| | MFS4_SDA | | I ² C ch.4 serial data I/O pin |
| | LCDD1 | | LCD bus interface data I/O pin |
| 159 | P2_17 | P | GPIO port |
| | MDATA3 | | External bus interface data I/O pin |
| | LCD0_SEG24 | | LCD controller segment output pin |
| | EINT23_5 | | External interrupt ch.23 input pin_5 |
| | MFS4_SCK_0 | | Multi-function serial ch.4 clock I/O pin_0 |
| | MFS4_SCL | | I ² C ch.4 clock I/O pin |
| | LCDD2 | | LCD bus interface data I/O pin |

| TEQFP176 | | | |
|----------|------------|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 160 | P2_18 | P | GPIO port |
| | MDATA4 | | External bus interface data I/O pin |
| | LCD0_SEG23 | | LCD controller segment output pin |
| | EINT0_0 | | External interrupt ch.0 input pin_0 |
| | MFS4_SIN_0 | | Multi-function serial ch.4 serial data input pin_0 |
| | LCDD3 | | LCD bus interface data I/O pin |
| 161 | P2_19 | P | GPIO port |
| | MDATA5 | | External bus interface data I/O pin |
| | LCD0_SEG22 | | LCD controller segment output pin |
| | EINT0_6 | | External interrupt ch.0 input pin_6 |
| | MFS4_CS0_0 | | Multi-function serial ch.4 serial chip select 0 I/O pin_0 |
| 162 | P2_20 | P | GPIO port |
| | MDATA6 | | External bus interface data I/O pin |
| | LCD0_SEG21 | | LCD controller segment output pin |
| | EINT1_6 | | External interrupt ch.1 input pin_6 |
| | MFS4_CS1_0 | | Multi-function serial ch.4 serial chip select 1 output pin_0 |
| 163 | P2_21 | P | GPIO port |
| | MDATA7 | | External bus interface data I/O pin |
| | LCD0_SEG20 | | LCD controller segment output pin |
| | EINT2_6 | | External interrupt ch.2 input pin_6 |
| | MFS4_CS2_0 | | Multi-function serial ch.4 serial chip select 2 output pin_0 |
| 164 | VSS | - | GND |
| 165 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 166 | P2_22 | P | GPIO port |
| | MAD0 | | External bus interface address output pin |
| | LCD0_SEG19 | | LCD controller segment output pin |
| | EINT3_6 | | External interrupt ch.3 input pin_6 |
| | MFS4_CS3_0 | | Multi-function serial ch.4 serial chip select 3 output pin_0 |
| | LCDD4 | | LCD bus interface data I/O pin |
| 167 | P2_23 | P | GPIO port |
| | MAD1 | | External bus interface address output pin |
| | LCD0_SEG18 | | LCD controller segment output pin |
| | EINT0_1 | | External interrupt ch.0 input pin_1 |
| | MFS1_SOT_0 | | Multi-function serial ch.1 serial data output pin_0 |
| | MFS1_SDA | | I ² C ch.1 serial data I/O pin |
| | LCDD5 | | LCD bus interface data I/O pin |
| 168 | P2_24 | P | GPIO port |
| | MAD2 | | External bus interface address output pin |
| | LCD0_SEG17 | | LCD controller segment output pin |
| | EINT4_1 | | External interrupt ch.4 input pin_1 |
| | MFS1_SCK_0 | | Multi-function serial ch.1 clock I/O pin_0 |
| | MFS1_SCL | | I ² C ch.1 clock I/O pin |
| | LCDD6 | | LCD bus interface data I/O pin |

| TEQFP176 | | | |
|----------|-------------|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 169 | P2_25 | P | GPIO port |
| | MAD3 | | External bus interface address output pin |
| | LCD0_SEG16 | | LCD controller segment output pin |
| | EINT1_0 | | External interrupt ch.1 input pin_0 |
| | MFS1_SIN_0 | | Multi-function serial ch.1 serial data input pin_0 |
| | LCDD7 | | LCD bus interface data I/O pin |
| 170 | P2_26 | P | GPIO port |
| | MAD4 | | External bus interface address output pin |
| | LCD0_SEG15 | | LCD controller segment output pin |
| | EINT5_1 | | External interrupt ch.5 input pin_1 |
| | MFS1_CS0_0 | | Multi-function serial ch.1 serial chip select 0 I/O pin_0 |
| | MFS0_CS0_1 | | Multi-function serial ch.0 serial chip select 0 I/O pin_1 |
| | LCDD8 | | LCD bus interface data I/O pin |
| 171 | P3_30 | A | GPIO port |
| | EINT7_1 | | External interrupt ch.7 input pin_1 |
| | CAN0_RX_2 | | CAN ch.0 reception data input pin_2 |
| 172 | P3_31 | A | GPIO port |
| | EINT9_1 | | External interrupt ch.9 input pin_1 |
| | CAN0_TX_2 | | CAN ch.0 transmission data output pin_2 |
| 173 | P2_27 | P | GPIO port |
| | MAD5 | | External bus interface address output pin |
| | LCD0_SEG14 | | LCD controller segment output pin |
| | EINT11_1 | | External interrupt ch.11 input pin_1 |
| | MFS1_CS1_0 | | Multi-function serial ch.1 serial chip select 1 output pin_0 |
| | MFS0_SOT_1 | | Multi-function serial ch.0 serial data output pin_1 |
| | LCDD9 | | LCD bus interface data I/O pin |
| 174 | P2_28 | P | GPIO port |
| | MAD6 | | External bus interface address output pin |
| | LCD0_SEG13 | | LCD controller segment output pin |
| | EINT13_1 | | External interrupt ch.13 input pin_1 |
| | MFS1_CS2_0 | | Multi-function serial ch.1 serial chip select 2 output pin_0 |
| | MFS0_SCK_1 | | Multi-function serial ch.0 clock I/O pin_1 |
| | LCDD10 | | LCD bus interface data I/O pin |
| 175 | P2_29 | P | GPIO port |
| | I2S1_ECLK_0 | | I2S ch.1 external clock input pin_0 |
| | MAD7 | | External bus interface address output pin |
| | LCD0_SEG12 | | LCD controller segment output pin |
| | EINT15_1 | | External interrupt ch.15 input pin_1 |
| | BT0_TIOA0_1 | | Base timer0 ch.0 TIOA output pin_1 |
| | MFS1_CS3_0 | | Multi-function serial ch.1 serial chip select 3 output pin_0 |
| | MFS0_SIN_1 | | Multi-function serial ch.0 serial data input pin_1 |
| | LCDD11 | | LCD bus interface data I/O pin |
| 176 | VSS | - | GND |

5.1.2 LQFP144/ TEQFP144

Table 5-1-2: Pin Descriptions of LQFP144/ TEQFP144

| LQFP144/ TEQFP144 | | | |
|-------------------|--------------------------------|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 1 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 2 | P0_00 | P | GPIO port |
| | I2S1_SD_0 | | I2S ch.1 serial data I/O pin_0 |
| | MAD8 | | External bus interface address output pin |
| | LCD0_SEG11 | | LCD controller segment output pin |
| | EINT23_1 | | External interrupt ch.23 input pin_1 |
| | BT0_TIOA1_1 | | Base timer0 ch.1 TIOA output pin_1 |
| | MFS7_SOT_1 | | Multi-function serial ch.7 serial data output pin_1 |
| | LCDD12 | | LCD bus interface data I/O pin |
| 3 | P0_01 | P | GPIO port |
| | I2S1_WS_0 | | I2S ch.1 word select pin_0 |
| | MAD9 | | External bus interface address output pin |
| | LCD0_SEG10 | | LCD controller segment output pin |
| | EINT0_2 | | External interrupt ch.0 input pin_2 |
| | BT1_TIOA2_1 | | Base timer1 ch.2 TIOA output pin_1 |
| | MFS7_SCK_1 | | Multi-function serial ch.7 clock I/O pin_1 |
| | LCDD13 | | LCD bus interface data I/O pin |
| 4 | P0_02 | P | GPIO port |
| | I2S1_SCK_0 | | I2S ch.1 serial clock pin_0 |
| | MAD10 | | External bus interface address output pin |
| | LCD0_SEG9 | | LCD controller segment output pin |
| | EINT1_2 | | External interrupt ch.1 input pin_2 |
| | BT1_TIOA3_1 | | Base timer1 ch.3 TIOA output pin_1 |
| | MFS7_SIN_1 | | Multi-function serial ch.7 serial data input pin_1 |
| | LCDD14 | | LCD bus interface data I/O pin |
| 5 | P0_03 | P | GPIO port |
| | I2S0_ECLK_0 | | I2S ch.0 external clock input pin_0 |
| | MAD11 | | External bus interface address output pin |
| | LCD0_SEG8 | | LCD controller segment output pin |
| | EINT5_2 | | External interrupt ch.5 input pin_2 |
| | PCMP0_BL_1 | | PCM_PWM ch.0 BL output pin_1 |
| | BT2_TIOA4_1 | | Base timer2 ch.4 TIOA output pin_1 |
| | MFS1_SOT_1 | | Multi-function serial ch.1 serial data output pin_1 |
| LCDD15 | LCD bus interface data I/O pin | | |
| 6 | P0_04 | P | GPIO port |
| | I2S0_SD_0 | | I2S ch.0 serial data I/O pin_0 |
| | MAD12 | | External bus interface address output pin |
| | LCD0_SEG7 | | LCD controller segment output pin |
| | EINT6_2 | | External interrupt ch.6 input pin_2 |
| | PCMP0_BH_1 | | PCM_PWM ch.0 BH output pin_1 |
| | BT2_TIOA5_1 | | Base timer2 ch.5 TIOA output pin_1 |
| | MFS1_SCK_1 | | Multi-function serial ch.1 clock I/O pin_1 |
| LCDD16 | LCD bus interface data I/O pin | | |

| LQFP144/ TEQFP144 | | | |
|-------------------|-------------|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 7 | P0_05 | P | GPIO port |
| | I2S0_WS_0 | | I2S ch.0 word select pin_0 |
| | MAD13 | | External bus interface address output pin |
| | LCD0_SEG6 | | LCD controller segment output pin |
| | EINT7_2 | | External interrupt ch.7 input pin_2 |
| | PCMP0_AL_1 | | PCM_PWM ch.0 AL output pin_1 |
| | BT3_TIOA6_1 | | Base timer3 ch.6 TIOA output pin_1 |
| | MFS1_SIN_1 | | Multi-function serial ch.1 serial data input pin_1 |
| | LCDD17 | | LCD bus interface data I/O pin |
| 8 | P0_06 | P | GPIO port |
| | I2S0_SCK_0 | | I2S ch.0 serial clock pin_0 |
| | MAD14 | | External bus interface address output pin |
| | LCD0_SEG5 | | LCD controller segment output pin |
| | EINT8_2 | | External interrupt ch.8 input pin_2 |
| | PCMP0_AH_1 | | PCM_PWM ch.0 AH output pin_1 |
| | BT3_TIOA7_1 | | Base timer3 ch.7 TIOA output pin_1 |
| | MFS1_CS0_1 | | Multi-function serial ch.1 serial chip select 0 I/O pin_1 |
| | CS# | | LCD bus interface chip select output pin |
| 9 | VCC53_1 | - | +3.3V/ +5.0V selection power supply pin (1) |
| 10 | VSS | - | GND |
| 11 | P0_07 | P | GPIO port |
| | MOEX | | External bus interface read enable signal output pin |
| | LCD0_SEG4 | | LCD controller segment output pin |
| | EINT18_2 | | External interrupt ch.18 input pin_2 |
| | MFS4_SOT_1 | | Multi-function serial ch.4 serial data output pin_1 |
| | WR# | | LCD bus interface write enable output pin |
| 12 | P0_08 | P | GPIO port |
| | MWEX | | External bus interface write enable signal output pin |
| | LCD0_SEG3 | | LCD controller segment output pin |
| | EINT19_2 | | External interrupt ch.19 input pin_2 |
| | MFS4_SCK_1 | | Multi-function serial ch.4 clock I/O pin_1 |
| | RD# | | LCD bus interface read enable output pin |
| 13 | P0_09 | P | GPIO port |
| | MCLK | | External bus interface clock output pin |
| | LCD0_SEG2 | | LCD controller segment output pin |
| | EINT20_2 | | External interrupt ch.20 input pin_2 |
| | PCMP1_BL_1 | | PCM_PWM ch.1 BL output pin_1 |
| | MFS4_SIN_1 | | Multi-function serial ch.4 serial data input pin_1 |

| LQFP144/ TEQFP144 | | | |
|-------------------|------------------|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 14 | P0_10 | P | GPIO port |
| | MDQM0 | | External bus interface byte mask signal output pin |
| | LCD0_SEG1 | | LCD controller segment output pin |
| | EINT21_2 | | External interrupt ch.21 input pin_2 |
| | PCMP1_BH_1 | | PCM_PWM ch.1 BH output pin_1 |
| | MFS4_CS0_1 | | Multi-function serial ch.4 serial chip select 0 I/O pin_1 |
| | RS | | LCD bus interface register select output pin |
| 15 | P0_11 | P | GPIO port |
| | MCSX2 | | External bus interface chip select output pin |
| | LCD0_SEG0 | | LCD controller segment output pin |
| | EINT22_2 | | External interrupt ch.22 input pin_2 |
| | PCMP1_AL_1 | | PCM_PWM ch.1 AL output pin_1 |
| | MFS4_CS1_1 | | Multi-function serial ch.4 serial chip select 1 output pin_1 |
| | RES# | | LCD bus interface reset control output pin |
| 16 | P0_12 | A | GPIO port |
| | MCSX3 | | External bus interface chip select output pin |
| | EINT23_2 | | External interrupt ch.23 input pin_2 |
| | PCMP1_AH_1 | | PCM_PWM ch.1 AH output pin_1 |
| | MFS4_CS2_1 | | Multi-function serial ch.4 serial chip select 2 output pin_1 |
| | TE | | LCD bus interface tearing effect input pin |
| 17 | VCC53_1 | - | +3.3V/ +5.0V selection power supply pin (1) |
| 18 | VSS | - | GND |
| 19 | P0_13 | M | GPIO port |
| | DDRHSSPI1_SDATA0 | | DDR HSSPI serial data I/O pin |
| | EINT1_3 | | External interrupt ch.1 input pin_3 |
| | MFS2_SOT_0 | | Multi-function serial ch.2 serial data output pin_0 |
| | MFS9_SOT_2 | | Multi-function serial ch.9 serial data output pin_2 |
| 20 | P0_14 | M | GPIO port |
| | DDRHSSPI1_SDATA2 | | DDR HSSPI serial data I/O pin |
| | EINT2_3 | | External interrupt ch.2 input pin_3 |
| | MFS2_SCK_0 | | Multi-function serial ch.2 clock I/O pin_0 |
| | MFS9_SCK_2 | | Multi-function serial ch.9 clock I/O pin_2 |
| 21 | P0_15 | M | GPIO port |
| | DDRHSSPI1_SDATA1 | | DDR HSSPI serial data I/O pin |
| | EINT2_0 | | External interrupt ch.2 input pin_0 |
| | MFS2_SIN_0 | | Multi-function serial ch.2 serial data input pin_0 |
| | MFS9_SIN_2 | | Multi-function serial ch.9 serial data input pin_2 |
| 22 | P0_16 | M | GPIO port |
| | DDRHSSPI1_SSEL | | DDR HSSPI select output pin |
| | EINT3_3 | | External interrupt ch.3 input pin_3 |
| | MFS2_CS0_0 | | Multi-function serial ch.2 serial chip select 0 I/O pin_0 |
| | MFS9_CS0_2 | | Multi-function serial ch.9 serial chip select 0 I/O pin_2 |

| LQFP144/ TEQFP144 | | | |
|-------------------|------------------|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 23 | P0_17 | M | GPIO port |
| | DDRHSSPI1_SDATA3 | | DDR HSSPI serial data I/O pin |
| | EINT4_3 | | External interrupt ch.4 input pin_3 |
| | MFS2_CS1_0 | | Multi-function serial ch.2 serial chip select 1 output pin_0 |
| | MFS9_CS1_2 | | Multi-function serial ch.9 serial chip select 1 output pin_2 |
| 24 | VCC53_2 | - | +3.3V/ +5.0V selection power supply pin (2) |
| 25 | VSS | - | GND |
| 26 | P0_18 | M | GPIO port |
| | DDRHSSPI0_SCLK | | DDR HSSPI serial clock output pin |
| | EINT5_3 | | External interrupt ch.5 input pin_3 |
| | MFS2_CS2_0 | | Multi-function serial ch.2 serial chip select 2 output pin_0 |
| 27 | VSS | - | GND |
| 28 | P0_19 | M | GPIO port |
| | DDRHSSPI0_SDATA0 | | DDR HSSPI serial data I/O pin |
| | EINT6_3 | | External interrupt ch.6 input pin_3 |
| | MFS2_CS3_0 | | Multi-function serial ch.2 serial chip select 3 output pin_0 |
| | MFS8_SOT_2 | | Multi-function serial ch.8 serial data output pin_2 |
| 29 | P0_20 | M | GPIO port |
| | DDRHSSPI0_SDATA2 | | DDR HSSPI serial data I/O pin |
| | EINT7_3 | | External interrupt ch.7 input pin_3 |
| | MFS3_SOT_0 | | Multi-function serial ch.3 serial data output pin_0 |
| | MFS8_SCK_2 | | Multi-function serial ch.8 clock I/O pin_2 |
| 30 | P0_21 | M | GPIO port |
| | DDRHSSPI0_SDATA1 | | DDR HSSPI serial data I/O pin |
| | EINT8_3 | | External interrupt ch.8 input pin_3 |
| | MFS3_SCK_0 | | Multi-function serial ch.3 clock I/O pin_0 |
| | MFS8_SIN_2 | | Multi-function serial ch.8 serial data input pin_2 |
| 31 | P0_22 | M | GPIO port |
| | DDRHSSPI0_SSEL | | DDR HSSPI select output pin |
| | ADC0_AN0 | | ADC ch.0 analog input pin |
| | EINT3_0 | | External interrupt ch.3 input pin_0 |
| | MFS3_SIN_0 | | Multi-function serial ch.3 serial data input pin_0 |
| | MFS8_CS0_2 | | Multi-function serial ch.8 serial chip select 0 I/O pin_2 |
| 32 | P0_23 | M | GPIO port |
| | DDRHSSPI0_SDATA3 | | DDR HSSPI serial data I/O pin |
| | ADC0_AN1 | | ADC ch.1 analog input pin |
| | EINT9_3 | | External interrupt ch.9 input pin_3 |
| | MFS3_CS0_0 | | Multi-function serial ch.3 serial chip select 0 I/O pin_0 |
| 33 | VCC53_2 | - | +3.3V/ +5.0V selection power supply pin (2) |
| 34 | VSS | - | GND |
| 35 | P0_24 | M | GPIO port |
| | ADC0_AN2 | | ADC ch.2 analog input pin |
| | EINT10_3 | | External interrupt ch.10 input pin_3 |
| | MFS3_CS1_0 | | Multi-function serial ch.3 serial chip select 1 output pin_0 |

| LQFP144/ TEQFP144 | | | |
|-------------------|------------------|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 36 | VCC53_2 | - | +3.3V/ +5.0V selection power supply pin (2) |
| 37 | VSS | - | GND |
| 38 | X1 | K | Main clock oscillation output pin |
| 39 | X0 | K | Main clock oscillation input pin |
| 40 | MODE | G | Mode pin |
| 41 | RSTX | H | External reset input pin |
| 42 | JTAG_NTRST | D | JTAG test reset input pin |
| 43 | JTAG_TDO | F | JTAG test data output pin |
| 44 | JTAG_TDI | E | JTAG test data input pin |
| 45 | JTAG_TCK | E | JTAG test clock input pin |
| 46 | JTAG_TMS | E | JTAG test mode state input pin |
| 47 | C | - | External capacity connection output pin |
| 48 | VSS | - | GND |
| 49 | VCC5 | - | +5.0 V power supply pin |
| 50 | P0_25 | A | GPIO port |
| | ADC0_AN6 | | ADC ch.6 analog input pin |
| | EINT4_0 | | External interrupt ch.4 input pin_0 |
| | PCMP0_BL_0 | | PCM_PWM ch.0 BL output pin_0 |
| | BT0_TIOA0_0 | | Base timer0 ch.0 TIOA output pin_0 |
| | OCU0_OUT0_0 | | Output compare0 ch.0 output pin_0 |
| | ICU0_IN0_0 | | Input capture0 ch.0 input pin_0 |
| | QPRC8_AIN | | Quadrature position and revolution counter ch.8 AIN input pin |
| | RLT0_TIN_0 | | Reload timer ch.0 event input pin_0 |
| | FRT0/1/2/3_TEXT | | Free-run timer ch.0/1/2/3 clock input pin |
| | CAN0_RX_0 | | CAN ch.0 reception data input pin_0 |
| | MFS8_SOT_0 | | Multi-function serial ch.8 serial data output pin_0 |
| | MFS0_SDA | | I ² C ch.0 serial data I/O pin |
| | PWU_AN0 | | Partial wakeup ADC analog 0 input pin |
| 51 | P0_26 | A | GPIO port |
| | ADC0_AN7 | | ADC ch.7 analog input pin |
| | EINT5_0 | | External interrupt ch.5 input pin_0 |
| | PCMP0_BH_0 | | PCM_PWM ch.0 BH output pin_0 |
| | BT0_TIOA1_0 | | Base timer0 ch.1 TIOA output pin_0 |
| | OCU0_OUT1_0 | | Output compare0 ch.1 output pin_0 |
| | ICU0_IN1_0 | | Input capture0 ch.1 input pin_0 |
| | QPRC8_BIN | | Quadrature position and revolution counter ch.8 BIN input pin |
| | RLT0_TOT_0 | | Reload timer ch.0 output pin_0 |
| | FRT4/8/9/10_TEXT | | Free-run timer ch.4/8/9/10 clock input pin |
| | CAN0_TX_0 | | CAN ch.0 transmission data output pin_0 |
| | MFS8_SCK_0 | | Multi-function serial ch.8 clock I/O pin_0 |
| | MFS0_SCL | | I ² C ch.0 clock I/O pin |
| | PWU_AN1 | | Partial wakeup ADC analog 1 input pin |

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|-------------------|--------------|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 52 | P0_27 | A | GPIO port |
| | ADC0_AN8 | | ADC ch.8 analog input pin |
| | EINT6_0 | | External interrupt ch.6 input pin_0 |
| | PCMP0_AL_0 | | PCM_PWM ch.0 AL output pin_0 |
| | SG0_SGA_0 | | Sound generator ch.0 SGA output pin_0 |
| | BT1_TIOA2_0 | | Base timer1 ch.2 TIOA output pin_0 |
| | ICU1_IN0_0 | | Input capture1 ch.0 input pin_0 |
| | QPRC8_ZIN | | Quadrature position and revolution counter ch.8 ZIN input pin |
| | RLT1_TIN_0 | | Reload timer ch.1 event input pin_0 |
| | CAN1_RX_0 | | CAN ch.1 reception data input pin_0 |
| | MFS8_SIN_0 | | Multi-function serial ch.8 serial data input pin_0 |
| | PWU_AN2 | | Partial wakeup ADC analog 2 input pin |
| 53 | P0_28 | A | GPIO port |
| | ADC0_AN9 | | ADC ch.9 analog input pin |
| | EINT7_0 | | External interrupt ch.7 input pin_0 |
| | PCMP0_AH_0 | | PCM_PWM ch.0 AH output pin_0 |
| | SG0_SGO_0 | | Sound generator ch.0 SGO output pin_0 |
| | BT1_TIOA3_0 | | Base timer1 ch.3 TIOA output pin_0 |
| | ICU1_IN1_0 | | Input capture1 ch.1 input pin_0 |
| | QPRC9_AIN | | Quadrature position and revolution counter ch.9 AIN input pin |
| | RLT1_TOT_0 | | Reload timer ch.1 output pin_0 |
| | CAN1_TX_0 | | CAN ch.1 transmission data output pin_0 |
| | MFS8_CS0_0 | | Multi-function serial ch.8 serial chip select 0 I/O pin_0 |
| | PWUTRG_0 | | Partial wakeup trigger output pin_0 |
| 54 | P0_29 | A | GPIO port |
| | ADC0_AN10 | | ADC ch.10 analog input pin |
| | EINT12_1 | | External interrupt ch.12 input pin_1 |
| | BT9_TIOA18_1 | | Base timer9 ch.18 TIOA output pin_1 |
| | OCU8_OUT0_1 | | Output compare8 ch.0 output pin_1 |
| | ICU8_IN0_1 | | Input capture8 ch.0 input pin_1 |
| | RLT17_TIN_1 | | Reload timer ch.17 event input pin_1 |
| 55 | NMIX | I | Non-maskable interrupt input pin |
| 56 | X0A | L | Sub clock oscillation input pin |
| | P0_30 | | GPIO port |
| | EINT8_0 | | External interrupt ch.8 input pin_0 |
| | BT4_TIOA8_0 | | Base timer4 ch.8 TIOA output pin_0 |
| | OCU8_OUT0_0 | | Output compare8 ch.0 output pin_0 |
| | ICU9_IN0_0 | | Input capture9 ch.0 input pin_0 |
| | RLT17_TIN_0 | | Reload timer ch.17 event input pin_0 |
| | MFS6_CS0_0 | | Multi-function serial ch.6 serial chip select 0 I/O pin_0 |

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|-------------------|-------------|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 57 | X1A | L | Sub clock oscillation output pin |
| | P0_31 | | GPIO port |
| | EINT9_0 | | External interrupt ch.9 input pin_0 |
| | BT4_TIOA9_0 | | Base timer4 ch.9 TIOA output pin_0 |
| | OCU8_OUT1_0 | | Output compare8 ch.1 output pin_0 |
| | ICU9_IN1_0 | | Input capture9 ch.1 input pin_0 |
| | RLT17_TOT_0 | | Reload timer ch.17 output pin_0 |
| | MFS6_CS1_0 | | Multi-function serial ch.6 serial chip select 1 output pin_0 |
| 58 | VSS | - | GND |
| 59 | VCC5 | - | +5.0 V power supply pin |
| 60 | P1_00 | A | GPIO port |
| | ADC0_AN11 | | ADC ch.11 analog input pin |
| | EINT10_0 | | External interrupt ch.10 input pin_0 |
| | PCMP1_BL_0 | | PCM_PWM ch.1 BL output pin_0 |
| | SG1_SGA_0 | | Sound generator ch.1 SGA output pin_0 |
| | BT2_TIOA4_0 | | Base timer2 ch.4 TIOA output pin_0 |
| | OCU1_OUT0_0 | | Output compare1 ch.0 output pin_0 |
| | ICU2_IN0_0 | | Input capture2 ch.0 input pin_0 |
| | QPRC9_BIN | | Quadrature position and revolution counter ch.9 BIN input pin |
| | RLT16_TIN_0 | | Reload timer ch.16 event input pin_0 |
| | CAN2_RX_0 | | CAN ch.2 reception data input pin_0 |
| | IND0_OUT_0 | | Indicator PWM output pin_0 |
| | TRACE0_0 | | Trace data 0 output pin_0 |
| 61 | P1_01 | A | GPIO port |
| | ADC0_AN12 | | ADC ch.12 analog input pin |
| | EINT11_0 | | External interrupt ch.11 input pin_0 |
| | PCMP1_BH_0 | | PCM_PWM ch.1 BH output pin_0 |
| | SG1_SGO_0 | | Sound generator ch.1 SGO output pin_0 |
| | BT2_TIOA5_0 | | Base timer2 ch.5 TIOA output pin_0 |
| | OCU1_OUT1_0 | | Output compare1 ch.1 output pin_0 |
| | ICU2_IN1_0 | | Input capture2 ch.1 input pin_0 |
| | QPRC9_ZIN | | Quadrature position and revolution counter ch.9 ZIN input pin |
| | RLT16_TOT_0 | | Reload timer ch.16 output pin_0 |
| | CAN2_TX_0 | | CAN ch.2 transmission data output pin_0 |
| | TRACE1_0 | | Trace data 1 output pin_0 |
| | PWU_AN3 | | Partial wakeup ADC analog 3 input pin |

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|-------------------|--------------|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 62 | P1_02 | C | GPIO port |
| | ADC0_AN13 | | ADC ch.13 analog input pin |
| | EINT12_0 | | External interrupt ch.12 input pin_0 |
| | PCMP1_AL_0 | | PCM_PWM ch.1 AL output pin_0 |
| | SG2_SGA_0 | | Sound generator ch.2 SGA output pin_0 |
| | BT3_TIOA6_0 | | Base timer3 ch.6 TIOA output pin_0 |
| | OCU2_OUT0_0 | | Output compare2 ch.0 output pin_0 |
| | ICU8_IN0_0 | | Input capture8 ch.0 input pin_0 |
| | MFS6_SOT_0 | | Multi-function serial ch.6 serial data output pin_0 |
| | MFS6_SDA | | I ² C ch.6 serial data I/O pin |
| | TRACE2_0 | | Trace data 2 output pin_0 |
| | PWU_AN4 | | Partial wakeup ADC analog 4 input pin |
| 63 | P1_03 | C | GPIO port |
| | ADC0_AN14 | | ADC ch.14 analog input pin |
| | EINT19_3 | | External interrupt ch.19 input pin_3 |
| | PCMP1_AH_0 | | PCM_PWM ch.1 AH output pin_0 |
| | SG2_SGO_0 | | Sound generator ch.2 SGO output pin_0 |
| | BT3_TIOA7_0 | | Base timer3 ch.7 TIOA output pin_0 |
| | OCU2_OUT1_0 | | Output compare2 ch.1 output pin_0 |
| | ICU8_IN1_0 | | Input capture8 ch.1 input pin_0 |
| | MFS6_SCK_0 | | Multi-function serial ch.6 clock I/O pin_0 |
| | MFS6_SCL | | I ² C ch.6 clock I/O pin |
| | TRACE3_0 | | Trace data 3 output pin_0 |
| | PWU_AN5 | | Partial wakeup ADC analog 5 input pin |
| 64 | P1_04 | A | GPIO port |
| | ADC0_AN15 | | ADC ch.15 analog input pin |
| | EINT13_0 | | External interrupt ch.13 input pin_0 |
| | SG3_SGA_0 | | Sound generator ch.3 SGA output pin_0 |
| | BT9_TIOA19_1 | | Base timer9 ch.19 TIOA output pin_1 |
| | OCU8_OUT1_1 | | Output compare8 ch.1 output pin_1 |
| | ICU8_IN1_1 | | Input capture8 ch.1 input pin_1 |
| | RLT17_TOT_1 | | Reload timer ch.17 output pin_1 |
| | MFS6_SIN_0 | | Multi-function serial ch.6 serial data input pin_0 |
| | TRACE_CLK_0 | | Trace clock output pin_0 |
| | PWU_AN6 | | Partial wakeup ADC analog 6 input pin |

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|-------------------|---|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 65 | P1_05 | C | GPIO port |
| | ADC0_AN16 | | ADC ch.16 analog input pin |
| | EINT14_0 | | External interrupt ch.14 input pin_0 |
| | SG3_SGO_0 | | Sound generator ch.3 SGO output pin_0 |
| | BT0_TIOB0/BT1_TIOB2/BT2_TIOB4/BT3_TIOB6/BT4_TIOB8/BT5_TIOB10_1 | | Base timer0/1/2/3/4/5 ch.0/2/4/6/8/10 TIOB input pin_1 |
| | OCU9_OUT0_1 | | Output compare9 ch.0 output pin_1 |
| | ICU9_IN0_1 | | Input capture9 ch.0 input pin_1 |
| | RLT2_TIN_1 | | Reload timer ch.2 event input pin_1 |
| | CAN3_RX_0 | | CAN ch.3 reception data input pin_0 |
| | MFS7_SOT_0 | | Multi-function serial ch.7 serial data output pin_0 |
| | MFS7_SDA | | I ² C ch.7 serial data I/O pin |
| | TRACE_CTL_0 | | Trace control output pin_0 |
| | PWU_AN7 | | Partial wakeup ADC analog 7 input pin |
| 66 | P1_06 | C | GPIO port |
| | ADC0_AN17 | | ADC ch.17 analog input pin |
| | EINT14_1 | | External interrupt ch.14 input pin_1 |
| | SG4_SGA_0 | | Sound generator ch.4 SGA output pin_0 |
| | BT6_TIOB12/BT7_TIOB14/BT8_TIOB16/BT9_TIOB18/BT10_TIOB20/BT11_TIOB22_1 | | Base timer6/7/8/9/10/11 ch.12/14/16/18/20/22 TIOB input pin_1 |
| | OCU9_OUT1_1 | | Output compare9 ch.1 output pin_1 |
| | ICU9_IN1_1 | | Input capture9 ch.1 input pin_1 |
| | RLT2_TOT_1 | | Reload timer ch.2 output pin_1 |
| | CAN3_TX_0 | | CAN ch.3 transmission data output pin_0 |
| | MFS7_SCK_0 | | Multi-function serial ch.7 clock I/O pin_0 |
| | MFS7_SCL | | I ² C ch.7 clock I/O pin |
| 67 | P1_07 | A | GPIO port |
| | ADC0_AN18 | | ADC ch.18 analog input pin |
| | EINT15_0 | | External interrupt ch.15 input pin_0 |
| | SG4_SGO_0 | | Sound generator ch.4 SGO output pin_0 |
| | BT5_TIOA10_0 | | Base timer5 ch.10 TIOA output pin_0 |
| | OCU9_OUT0_0 | | Output compare9 ch.0 output pin_0 |
| | ICU10_IN0_0 | | Input capture10 ch.0 input pin_0 |
| | MFS7_SIN_0 | | Multi-function serial ch.7 serial data input pin_0 |
| | SYSC0_CLK_1 | | System clock output pin_1 |
| 68 | AVCC5 | - | Analog power supply pin |
| 69 | AVSS | - | Analog GND pin |
| 70 | AVRL5 | - | ADC low reference voltage pin |
| 71 | AVRH5 | - | ADC high reference voltage pin |
| 72 | VCC5 | - | +5.0 V power supply pin |
| 73 | VSS | A | GND |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 74 | P1_08 | A | GPIO port |
| | ADC0_TRG0_1 | | ADC external trigger ch.0 input pin_1 |
| | EINT16_0 | | External interrupt ch.16 input pin_0 |
| | BT5_TIOA11_0 | | Base timer5 ch.11 TIOA output pin_0 |
| | OCU10_OUT0_0 | | Output compare10 ch.0 output pin_0 |
| | ICU10_IN1_0 | | Input capture10 ch.1 input pin_0 |
| | RLT3_TIN_0 | | Reload timer ch.3 event input pin_0 |
| | MFS7_CS0_0 | | Multi-function serial ch.7 serial chip select 0 I/O pin_0 |
| | IND0_OUT_1 | | Indicator PWM output pin_1 |
| 75 | VSS | - | GND |
| 76 | VCC5 | - | +5.0 V power supply pin |
| 77 | P1_09 | A | GPIO port |
| | ADC0_TRG0_0 | | ADC external trigger ch.0 input pin_0 |
| | EINT9_4 | | External interrupt ch.9 input pin_4 |
| | BT0_TIOB0/BT1_TIOB2/BT2_TIOB4/BT3_TIOB6/BT4_TIOB8/BT5_TIOB10_0 | | Base timer0/1/2/3/4/5 ch.0/2/4/6/8/10 TIOB input pin_0 |
| | OCU10_OUT1_0 | | Output compare10 ch.1 output pin_0 |
| | RLT3_TOT_0 | | Reload timer ch.3 output pin_0 |
| | MFS7_CS1_0 | | Multi-function serial ch.7 serial chip select 1 output pin_0 |
| | RTC0_WOT | | RTC overflow output pin |
| | SYSC0_CLK_0 | | System clock output pin_0 |
| 78 | DVSS | - | SMC high current port GND pin |
| 79 | DVCC | - | SMC high current port power supply pin |
| 80 | P1_10 | O | GPIO port |
| | ADC0_AN24 | | ADC ch.24 analog input pin |
| | SMC0_PWM1P | | Stepper motor controller ch.0 PWM1P output pin |
| | EINT17_0 | | External interrupt ch.17 input pin_0 |
| | BT6_TIOA12_0 | | Base timer6 ch.12 TIOA output pin_0 |
| 81 | P1_11 | O | GPIO port |
| | ADC0_AN25 | | ADC ch.25 analog input pin |
| | SMC0_PWM1M | | Stepper motor controller ch.0 PWM1M output pin |
| | EINT11_4 | | External interrupt ch.11 input pin_4 |
| | BT6_TIOA13_0 | | Base timer6 ch.13 TIOA output pin_0 |
| 82 | P1_12 | O | GPIO port |
| | ADC0_AN26 | | ADC ch.26 analog input pin |
| | SMC0_PWM2P | | Stepper motor controller ch.0 PWM2P output pin |
| | EINT18_0 | | External interrupt ch.18 input pin_0 |
| | BT7_TIOA14_0 | | Base timer7 ch.14 TIOA output pin_0 |
| | MFS0_SOT_0 | | Multi-function serial ch.0 serial data output pin_0 |
| | MFS8_SDA | | I ² C ch.8 serial data I/O pin |

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| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 83 | P1_13 | O | GPIO port |
| | ADC0_AN27 | | ADC ch.27 analog input pin |
| | SMC0_PWM2M | | Stepper motor controller ch.0 PWM2M output pin |
| | EINT12_4 | | External interrupt ch.12 input pin_4 |
| | BT7_TIOA15_0 | | Base timer7 ch.15 TIOA output pin_0 |
| | MFS0_SCK_0 | | Multi-function serial ch.0 clock I/O pin_0 |
| | MFS8_SCL | | I ² C ch.8 clock I/O pin |
| 84 | P1_14 | O | GPIO port |
| | ADC0_AN28 | | ADC ch.28 analog input pin |
| | SMC1_PWM1P | | Stepper motor controller ch.1 PWM1P output pin |
| | EINT19_0 | | External interrupt ch.19 input pin_0 |
| | BT8_TIOA16_0 | | Base timer8 ch.16 TIOA output pin_0 |
| | MFS0_SIN_0 | | Multi-function serial ch.0 serial data input pin_0 |
| 85 | P1_15 | O | GPIO port |
| | ADC0_AN29 | | ADC ch.29 analog input pin |
| | SMC1_PWM1M | | Stepper motor controller ch.1 PWM1M output pin |
| | EINT13_4 | | External interrupt ch.13 input pin_4 |
| | BT8_TIOA17_0 | | Base timer8 ch.17 TIOA output pin_0 |
| | MFS0_CS0_0 | | Multi-function serial ch.0 serial chip select 0 I/O pin_0 |
| 86 | P1_16 | O | GPIO port |
| | ADC0_AN30 | | ADC ch.30 analog input pin |
| | SMC1_PWM2P | | Stepper motor controller ch.1 PWM2P output pin |
| | EINT14_4 | | External interrupt ch.14 input pin_4 |
| | BT9_TIOA18_0 | | Base timer9 ch.18 TIOA output pin_0 |
| | MFS9_CS0_0 | | Multi-function serial ch.9 serial chip select 0 I/O pin_0 |
| 87 | P1_17 | O | GPIO port |
| | ADC0_AN31 | | ADC ch.31 analog input pin |
| | SMC1_PWM2M | | Stepper motor controller ch.1 PWM2M output pin |
| | EINT15_4 | | External interrupt ch.15 input pin_4 |
| | BT9_TIOA19_0 | | Base timer9 ch.19 TIOA output pin_0 |
| | MFS9_CS1_0 | | Multi-function serial ch.9 serial chip select 1 output pin_0 |
| 88 | DVSS | - | SMC high current port GND pin |
| 89 | DVCC | - | SMC high current port power supply pin |
| 90 | P1_18 | O | GPIO port |
| | ADC0_AN32 | | ADC ch.32 analog input pin |
| | SMC2_PWM1P | | Stepper motor controller ch.2 PWM1P output pin |
| | EINT17_4 | | External interrupt ch.17 input pin_4 |
| | BT10_TIOA20_0 | | Base timer10 ch.20 TIOA output pin_0 |
| | MFS9_SOT_0 | | Multi-function serial ch.9 serial data output pin_0 |
| | MFS9_SDA | | I ² C ch.9 serial data I/O pin |

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|-------------------|---|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 91 | P1_19 | O | GPIO port |
| | ADC0_AN33 | | ADC ch.33 analog input pin |
| | SMC2_PWM1M | | Stepper motor controller ch.2 PWM1M output pin |
| | EINT18_4 | | External interrupt ch.18 input pin_4 |
| | BT10_TIOA21_0 | | Base timer10 ch.21 TIOA output pin_0 |
| | MFS9_SCK_0 | | Multi-function serial ch.9 clock I/O pin_0 |
| | MFS9_SCL | | I ² C ch.9 clock I/O pin |
| 92 | P1_20 | O | GPIO port |
| | ADC0_AN34 | | ADC ch.34 analog input pin |
| | SMC2_PWM2P | | Stepper motor controller ch.2 PWM2P output pin |
| | EINT20_0 | | External interrupt ch.20 input pin_0 |
| | BT11_TIOA22_0 | | Base timer11 ch.22 TIOA output pin_0 |
| | MFS9_SIN_0 | | Multi-function serial ch.9 serial data input pin_0 |
| 93 | P1_21 | O | GPIO port |
| | ADC0_AN35 | | ADC ch.35 analog input pin |
| | SMC2_PWM2M | | Stepper motor controller ch.2 PWM2M output pin |
| | EINT20_4 | | External interrupt ch.20 input pin_4 |
| | BT11_TIOA23_0 | | Base timer11 ch.23 TIOA output pin_0 |
| | MFS10_SOT_0 | | Multi-function serial ch.10 serial data output pin_0 |
| | MFS10_SDA | | I ² C ch.10 serial data I/O pin |
| 94 | P1_22 | O | GPIO port |
| | ADC0_AN36 | | ADC ch.36 analog input pin |
| | SMC3_PWM1P | | Stepper motor controller ch.3 PWM1P output pin |
| | EINT21_4 | | External interrupt ch.21 input pin_4 |
| | BT6_TIOB12/BT7_TIOB14/BT8_TIOB16/BT9_TIOB18/BT10_TIOB20/BT11_TIOB22_0 | | Base timer6/7/8/9/10/11 ch.12/14/16/18/20/22 TIOB input pin_0 |
| | MFS10_SCK_0 | | Multi-function serial ch.10 clock I/O pin_0 |
| | MFS10_SCL | | I ² C ch.10 clock I/O pin |
| 95 | P1_23 | O | GPIO port |
| | ADC0_AN37 | | ADC ch.37 analog input pin |
| | SMC3_PWM1M | | Stepper motor controller ch.3 PWM1M output pin |
| | EINT21_0 | | External interrupt ch.21 input pin_0 |
| | BT12_TIOA24_0 | | Base timer12 ch.24 TIOA output pin_0 |
| | MFS10_SIN_0 | | Multi-function serial ch.10 serial data input pin_0 |
| 96 | P1_24 | O | GPIO port |
| | ADC0_AN38 | | ADC ch.38 analog input pin |
| | SMC3_PWM2P | | Stepper motor controller ch.3 PWM2P output pin |
| | EINT22_4 | | External interrupt ch.22 input pin_4 |
| | BT12_TIOA25_0 | | Base timer12 ch.25 TIOA output pin_0 |
| | MFS10_CS0_0 | | Multi-function serial ch.10 serial chip select 0 I/O pin_0 |

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|-------------------|---------------|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 97 | P1_25 | O | GPIO port |
| | ADC0_AN39 | | ADC ch.39 analog input pin |
| | SMC3_PWM2M | | Stepper motor controller ch.3 PWM2M output pin |
| | EINT0_5 | | External interrupt ch.0 input pin_5 |
| | BT13_TIOA26_0 | | Base timer13 ch.26 TIOA output pin_0 |
| | MFS11_CS0_0 | | Multi-function serial ch.11 serial chip select 0 I/O pin_0 |
| 98 | DVSS | - | SMC high current port GND pin |
| 99 | DVCC | - | SMC high current port power supply pin |
| 100 | P1_26 | O | GPIO port |
| | ADC0_AN40 | | ADC ch.40 analog input pin |
| | SMC4_PWM1P | | Stepper motor controller ch.4 PWM1P output pin |
| | EINT2_5 | | External interrupt ch.2 input pin_5 |
| | BT13_TIOA27_0 | | Base timer13 ch.27 TIOA output pin_0 |
| | MFS11_CS1_0 | | Multi-function serial ch.11 serial chip select 1 output pin_0 |
| 101 | P1_27 | O | GPIO port |
| | ADC0_AN41 | | ADC ch.41 analog input pin |
| | SMC4_PWM1M | | Stepper motor controller ch.4 PWM1M output pin |
| | EINT3_5 | | External interrupt ch.3 input pin_5 |
| | BT14_TIOA28_0 | | Base timer14 ch.28 TIOA output pin_0 |
| | MFS11_SOT_0 | | Multi-function serial ch.11 serial data output pin_0 |
| | MFS11_SDA | | I ² C ch.11 serial data I/O pin |
| 102 | P1_28 | O | GPIO port |
| | ADC0_AN42 | | ADC ch.42 analog input pin |
| | SMC4_PWM2P | | Stepper motor controller ch.4 PWM2P output pin |
| | EINT4_5 | | External interrupt ch.4 input pin_5 |
| | BT14_TIOA29_0 | | Base timer14 ch.29 TIOA output pin_0 |
| | MFS11_SCK_0 | | Multi-function serial ch.11 clock I/O pin_0 |
| | MFS11_SCL | | I ² C ch.11 clock I/O pin |
| 103 | P1_29 | O | GPIO port |
| | ADC0_AN43 | | ADC ch.43 analog input pin |
| | SMC4_PWM2M | | Stepper motor controller ch.4 PWM2M output pin |
| | EINT22_0 | | External interrupt ch.22 input pin_0 |
| | BT15_TIOA30_0 | | Base timer15 ch.30 TIOA output pin_0 |
| | MFS11_SIN_0 | | Multi-function serial ch.11 serial data input pin_0 |
| 104 | P1_30 | O | GPIO port |
| | ADC0_AN44 | | ADC ch.44 analog input pin |
| | SMC5_PWM1P | | Stepper motor controller ch.5 PWM1P output pin |
| | EINT6_5 | | External interrupt ch.6 input pin_5 |
| | BT15_TIOA31_0 | | Base timer15 ch.31 TIOA output pin_0 |
| | MFS5_SOT_0 | | Multi-function serial ch.5 serial data output pin_0 |
| | MFS5_SDA | | I ² C ch.5 serial data I/O pin |

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|-------------------|---|------------------|---|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 105 | P1_31 | O | GPIO port |
| | ADC0_AN45 | | ADC ch.45 analog input pin |
| | SMC5_PWM1M | | Stepper motor controller ch.5 PWM1M output pin |
| | EINT7_5 | | External interrupt ch.7 input pin_5 |
| | BT12_TIOB24/BT13_TIOB26/BT14_TIOB28/BT15_TIOB30_0 | | Base timer12/13/14/15 ch.24/26/28/30 TIOB input pin_0 |
| | MFS5_SCK_0 | | Multi-function serial ch.5 clock I/O pin_0 |
| | MFS5_SCL | | I ² C ch.5 clock I/O pin |
| 106 | P2_00 | O | GPIO port |
| | ADC0_AN46 | | ADC ch.46 analog input pin |
| | SMC5_PWM2P | | Stepper motor controller ch.5 PWM2P output pin |
| | EINT23_0 | | External interrupt ch.23 input pin_0 |
| | MFS5_SIN_0 | | Multi-function serial ch.5 serial data input pin_0 |
| 107 | P2_01 | O | GPIO port |
| | ADC0_AN47 | | ADC ch.47 analog input pin |
| | SMC5_PWM2M | | Stepper motor controller ch.5 PWM2M output pin |
| | EINT9_5 | | External interrupt ch.9 input pin_5 |
| | MFS5_CS0_0 | | Multi-function serial ch.5 serial chip select 0 I/O pin_0 |
| 108 | DVSS | - | SMC high current port GND pin |
| 109 | DVCC | - | SMC high current port power supply pin |
| 110 | VSS | - | GND |
| 111 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 112 | P2_02 | Q | General-purpose input port |
| | LCD0_V3 | | LCD controller reference voltage V3 input pin |
| | EINT2_1 | | External interrupt ch.2 input pin_1 |
| 113 | P2_03 | A | GPIO port |
| | MRDY | | External bus interface ready input pin |
| | LCD0_V2 | | LCD controller reference voltage V2 input pin |
| | EINT10_5 | | External interrupt ch.10 input pin_5 |
| 114 | P2_04 | A | GPIO port |
| | I2S0_ECLK_1 | | I2S ch.0 external clock input pin_1 |
| | MDATA8 | | External bus interface data I/O pin |
| | LCD0_V1 | | LCD controller reference voltage V1 input pin |
| | EINT11_5 | | External interrupt ch.11 input pin_5 |
| | BT12_TIOA24_1 | | Base timer12 ch.24 TIOA output pin_1 |
| | MFS2_SOT_1 | | Multi-function serial ch.2 serial data output pin_1 |
| 115 | P2_05 | A | GPIO port |
| | I2S0_SD_1 | | I2S ch.0 serial data I/O pin_1 |
| | MDATA9 | | External bus interface data I/O pin |
| | LCD0_V0 | | LCD controller reference voltage V0 input pin |
| | EINT12_5 | | External interrupt ch.12 input pin_5 |
| | BT12_TIOA25_1 | | Base timer12 ch.25 TIOA output pin_1 |
| | MFS2_SCK_1 | | Multi-function serial ch.2 clock I/O pin_1 |

| LQFP144/ TEQFP144 | | | |
|-------------------|---------------|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 116 | P2_06 | P | GPIO port |
| | I2S0_WS_1 | | I2S ch.0 word select pin_1 |
| | MDATA10 | | External bus interface data I/O pin |
| | LCD0_COM3 | | LCD controller common output pin |
| | EINT13_5 | | External interrupt ch.13 input pin_5 |
| | BT13_TIOA26_1 | | Base timer13 ch.26 TIOA output pin_1 |
| | MFS2_SIN_1 | | Multi-function serial ch.2 serial data input pin_1 |
| 117 | P2_07 | P | GPIO port |
| | I2S0_SCK_1 | | I2S ch.0 serial clock pin_1 |
| | MDATA11 | | External bus interface data I/O pin |
| | LCD0_COM2 | | LCD controller common output pin |
| | EINT14_5 | | External interrupt ch.14 input pin_5 |
| | BT13_TIOA27_1 | | Base timer13 ch.27 TIOA output pin_1 |
| | MFS2_CS0_1 | | Multi-function serial ch.2 serial chip select 0 I/O pin_1 |
| 118 | P2_08 | P | GPIO port |
| | MCSX0 | | External bus interface chip select output pin |
| | LCD0_COM1 | | LCD controller common output pin |
| | EINT15_5 | | External interrupt ch.15 input pin_5 |
| | BT14_TIOA28_1 | | Base timer14 ch.28 TIOA output pin_1 |
| | MFS2_CS1_1 | | Multi-function serial ch.2 serial chip select 1 output pin_1 |
| 119 | VSS | - | GND |
| 120 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 121 | P2_09 | P | GPIO port |
| | MDATA12 | | External bus interface data I/O pin |
| | LCD0_COM0 | | LCD controller common output pin |
| | EINT3_1 | | External interrupt ch.3 input pin_1 |
| | BT14_TIOA29_1 | | Base timer14 ch.29 TIOA output pin_1 |
| | MFS3_SOT_1 | | Multi-function serial ch.3 serial data output pin_1 |
| 122 | P2_10 | P | GPIO port |
| | MDATA13 | | External bus interface data I/O pin |
| | LCD0_SEG31 | | LCD controller segment output pin |
| | EINT16_5 | | External interrupt ch.16 input pin_5 |
| | SG0_SGA_2 | | Sound generator ch.0 SGA output pin_2 |
| | BT15_TIOA30_1 | | Base timer15 ch.30 TIOA output pin_1 |
| | MFS3_SCK_1 | | Multi-function serial ch.3 clock I/O pin_1 |
| 123 | P2_11 | P | GPIO port |
| | MDATA14 | | External bus interface data I/O pin |
| | LCD0_SEG30 | | LCD controller segment output pin |
| | EINT17_5 | | External interrupt ch.17 input pin_5 |
| | SG0_SGO_2 | | Sound generator ch.0 SGO output pin_2 |
| | BT15_TIOA31_1 | | Base timer15 ch.31 TIOA output pin_1 |
| | MFS3_SIN_1 | | Multi-function serial ch.3 serial data input pin_1 |

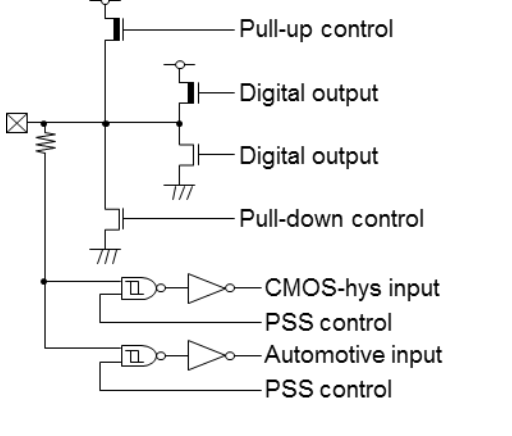
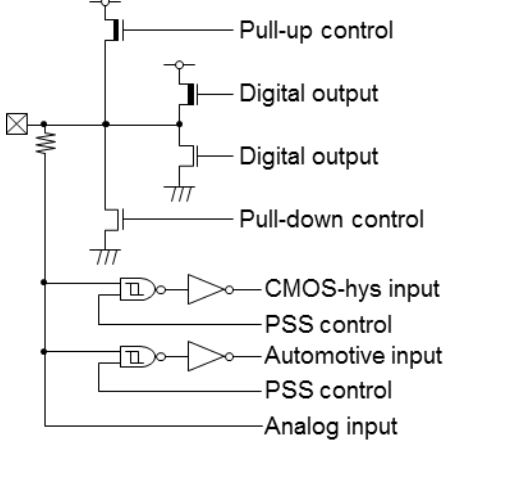
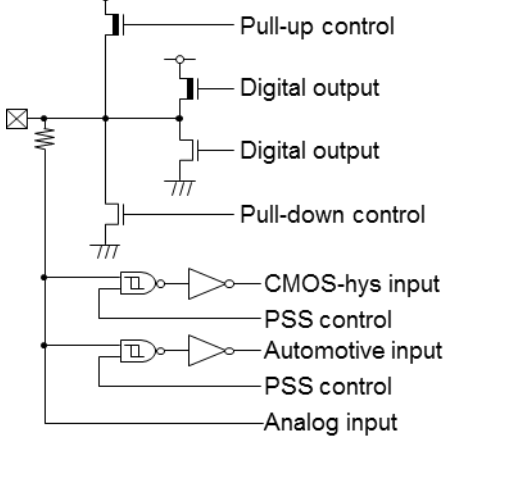
| LQFP144/ TEQFP144 | | | |
|-------------------|---|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 124 | P2_12 | P | GPIO port |
| | MDATA15 | | External bus interface data I/O pin |
| | LCD0_SEG29 | | LCD controller segment output pin |
| | EINT18_5 | | External interrupt ch.18 input pin_5 |
| | SG1_SGA_2 | | Sound generator ch.1 SGA output pin_2 |
| | BT12_TIOB24/BT13_TIOB26/BT14_TIOB28/BT15_TIOB30_1 | | Base timer12/13/14/15 ch.24/26/28/30 TIOB input pin_1 |
| | MFS3_CS0_1 | | Multi-function serial ch.3 serial chip select 0 I/O pin_1 |
| 125 | P2_13 | P | GPIO port |
| | MCSX1 | | External bus interface chip select output pin |
| | LCD0_SEG28 | | LCD controller segment output pin |
| | EINT19_5 | | External interrupt ch.19 input pin_5 |
| | SG1_SGO_2 | | Sound generator ch.1 SGO output pin_2 |
| | MFS3_CS1_1 | | Multi-function serial ch.3 serial chip select 1 output pin_1 |
| 126 | P2_14 | P | GPIO port |
| | MDATA0 | | External bus interface data I/O pin |
| | LCD0_SEG27 | | LCD controller segment output pin |
| | EINT20_5 | | External interrupt ch.20 input pin_5 |
| | MFS3_CS2_1 | | Multi-function serial ch.3 serial chip select 2 output pin_1 |
| 127 | P2_15 | P | GPIO port |
| | MDATA1 | | External bus interface data I/O pin |
| | LCD0_SEG26 | | LCD controller segment output pin |
| | EINT21_5 | | External interrupt ch.21 input pin_5 |
| | MFS3_CS3_1 | | Multi-function serial ch.3 serial chip select 3 output pin_1 |
| | LCDD0 | | LCD bus interface data I/O pin |
| 128 | P2_16 | P | GPIO port |
| | MDATA2 | | External bus interface data I/O pin |
| | LCD0_SEG25 | | LCD controller segment output pin |
| | EINT22_5 | | External interrupt ch.22 input pin_5 |
| | MFS4_SOT_0 | | Multi-function serial ch.4 serial data output pin_0 |
| | MFS4_SDA | | I ² C ch.4 serial data I/O pin |
| | LCDD1 | | LCD bus interface data I/O pin |
| 129 | P2_17 | P | GPIO port |
| | MDATA3 | | External bus interface data I/O pin |
| | LCD0_SEG24 | | LCD controller segment output pin |
| | EINT23_5 | | External interrupt ch.23 input pin_5 |
| | MFS4_SCK_0 | | Multi-function serial ch.4 clock I/O pin_0 |
| | MFS4_SCL | | I ² C ch.4 clock I/O pin |
| | LCDD2 | | LCD bus interface data I/O pin |

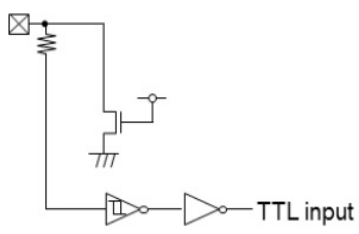
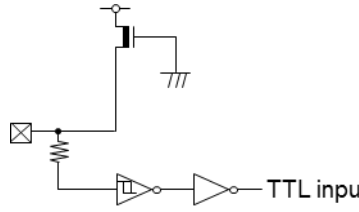
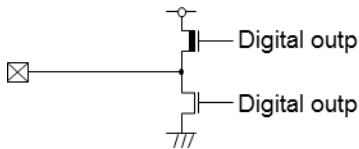
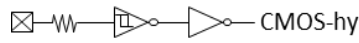
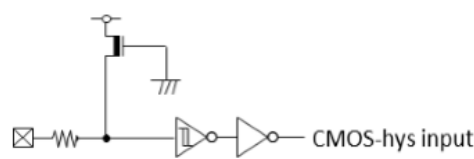
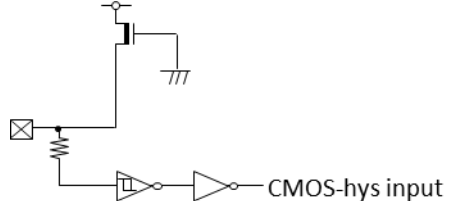
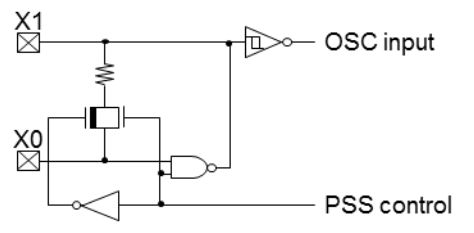
| LQFP144/ TEQFP144 | | | |
|-------------------|------------|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 130 | P2_18 | P | GPIO port |
| | MDATA4 | | External bus interface data I/O pin |
| | LCD0_SEG23 | | LCD controller segment output pin |
| | EINT0_0 | | External interrupt ch.0 input pin_0 |
| | MFS4_SIN_0 | | Multi-function serial ch.4 serial data input pin_0 |
| | LCDD3 | | LCD bus interface data I/O pin |
| 131 | P2_19 | P | GPIO port |
| | MDATA5 | | External bus interface data I/O pin |
| | LCD0_SEG22 | | LCD controller segment output pin |
| | EINT0_6 | | External interrupt ch.0 input pin_6 |
| | MFS4_CS0_0 | | Multi-function serial ch.4 serial chip select 0 I/O pin_0 |
| 132 | P2_20 | P | GPIO port |
| | MDATA6 | | External bus interface data I/O pin |
| | LCD0_SEG21 | | LCD controller segment output pin |
| | EINT1_6 | | External interrupt ch.1 input pin_6 |
| | MFS4_CS1_0 | | Multi-function serial ch.4 serial chip select 1 output pin_0 |
| 133 | P2_21 | P | GPIO port |
| | MDATA7 | | External bus interface data I/O pin |
| | LCD0_SEG20 | | LCD controller segment output pin |
| | EINT2_6 | | External interrupt ch.2 input pin_6 |
| | MFS4_CS2_0 | | Multi-function serial ch.4 serial chip select 2 output pin_0 |
| 134 | VSS | - | GND |
| 135 | VCC53_1 | - | +3.3 V/ +5.0 V selection power supply pin (1) |
| 136 | P2_22 | P | GPIO port |
| | MAD0 | | External bus interface address output pin |
| | LCD0_SEG19 | | LCD controller segment output pin |
| | EINT3_6 | | External interrupt ch.3 input pin_6 |
| | MFS4_CS3_0 | | Multi-function serial ch.4 serial chip select 3 output pin_0 |
| | LCDD4 | | LCD bus interface data I/O pin |
| 137 | P2_23 | P | GPIO port |
| | MAD1 | | External bus interface address output pin |
| | LCD0_SEG18 | | LCD controller segment output pin |
| | EINT0_1 | | External interrupt ch.0 input pin_1 |
| | MFS1_SOT_0 | | Multi-function serial ch.1 serial data output pin_0 |
| | MFS1_SDA | | I ² C ch.1 serial data I/O pin |
| | LCDD5 | | LCD bus interface data I/O pin |
| 138 | P2_24 | P | GPIO port |
| | MAD2 | | External bus interface address output pin |
| | LCD0_SEG17 | | LCD controller segment output pin |
| | EINT4_1 | | External interrupt ch.4 input pin_1 |
| | MFS1_SCK_0 | | Multi-function serial ch.1 clock I/O pin_0 |
| | MFS1_SCL | | I ² C ch.1 clock I/O pin |
| | LCDD6 | | LCD bus interface data I/O pin |

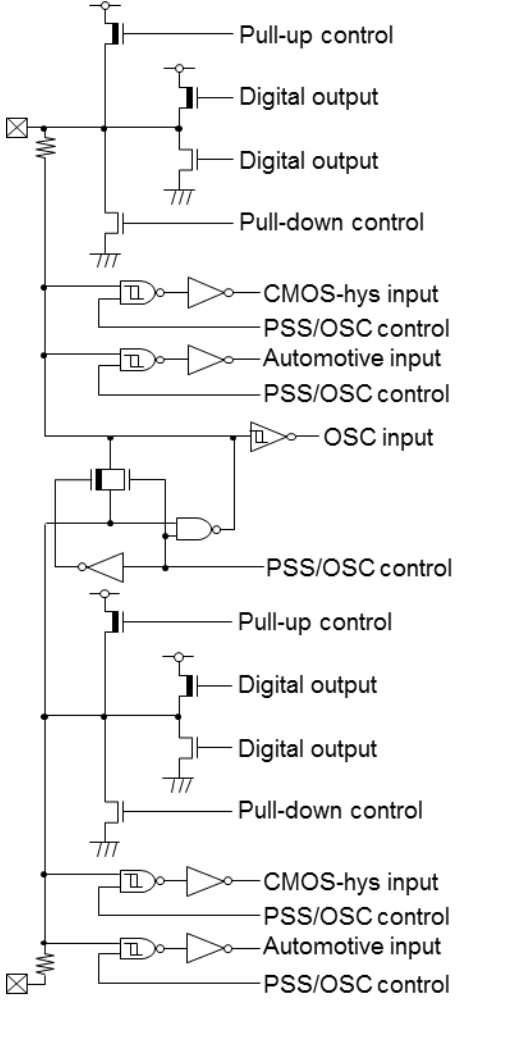
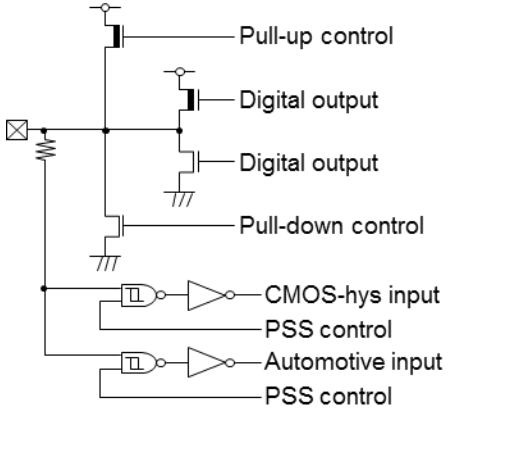
| LQFP144/ TEQFP144 | | | |
|-------------------|-------------|------------------|--|
| Pin No. | Pin Name | I/O Circuit Type | Function Description |
| 139 | P2_25 | P | GPIO port |
| | MAD3 | | External bus interface address output pin |
| | LCD0_SEG16 | | LCD controller segment output pin |
| | EINT1_0 | | External interrupt ch.1 input pin_0 |
| | MFS1_SIN_0 | | Multi-function serial ch.1 serial data input pin_0 |
| | LCDD7 | | LCD bus interface data I/O pin |
| 140 | P2_26 | P | GPIO port |
| | MAD4 | | External bus interface address output pin |
| | LCD0_SEG15 | | LCD controller segment output pin |
| | EINT5_1 | | External interrupt ch.5 input pin_1 |
| | MFS1_CS0_0 | | Multi-function serial ch.1 serial chip select 0 I/O pin_0 |
| | MFS0_CS0_1 | | Multi-function serial ch.0 serial chip select 0 I/O pin_1 |
| | LCDD8 | | LCD bus interface data I/O pin |
| 141 | P2_27 | P | GPIO port |
| | MAD5 | | External bus interface address output pin |
| | LCD0_SEG14 | | LCD controller segment output pin |
| | EINT11_1 | | External interrupt ch.11 input pin_1 |
| | MFS1_CS1_0 | | Multi-function serial ch.1 serial chip select 1 output pin_0 |
| | MFS0_SOT_1 | | Multi-function serial ch.0 serial data output pin_1 |
| | LCDD9 | | LCD bus interface data I/O pin |
| 142 | P2_28 | P | GPIO port |
| | MAD6 | | External bus interface address output pin |
| | LCD0_SEG13 | | LCD controller segment output pin |
| | EINT13_1 | | External interrupt ch.13 input pin_1 |
| | MFS1_CS2_0 | | Multi-function serial ch.1 serial chip select 2 output pin_0 |
| | MFS0_SCK_1 | | Multi-function serial ch.0 clock I/O pin_1 |
| | LCDD10 | | LCD bus interface data I/O pin |
| 143 | P2_29 | P | GPIO port |
| | I2S1_ECLK_0 | | I2S ch.1 external clock input pin_0 |
| | MAD7 | | External bus interface address output pin |
| | LCD0_SEG12 | | LCD controller segment output pin |
| | EINT15_1 | | External interrupt ch.15 input pin_1 |
| | BT0_TIOA0_1 | | Base timer0 ch.0 TIOA output pin_1 |
| | MFS1_CS3_0 | | Multi-function serial ch.1 serial chip select 3 output pin_0 |
| | MFS0_SIN_1 | | Multi-function serial ch.0 serial data input pin_1 |
| | LCDD11 | | LCD bus interface data I/O pin |
| 144 | VSS | - | GND |

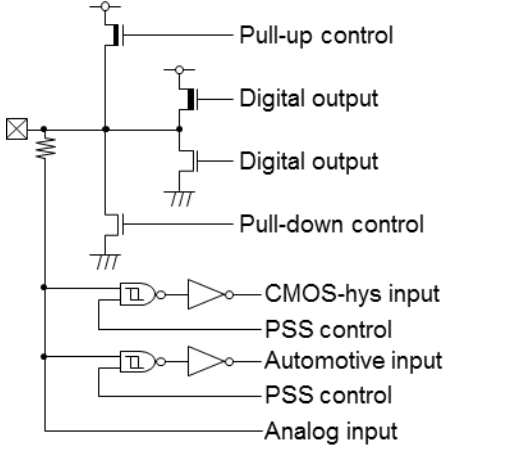
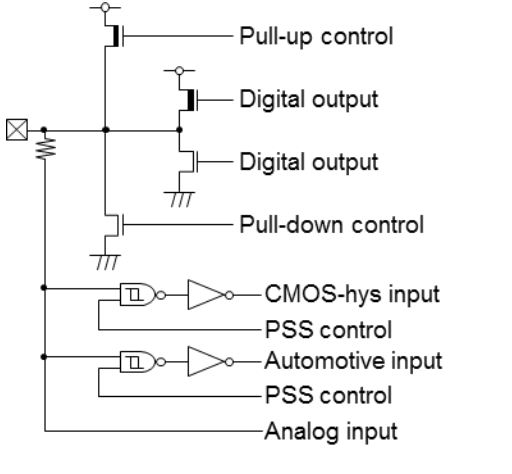
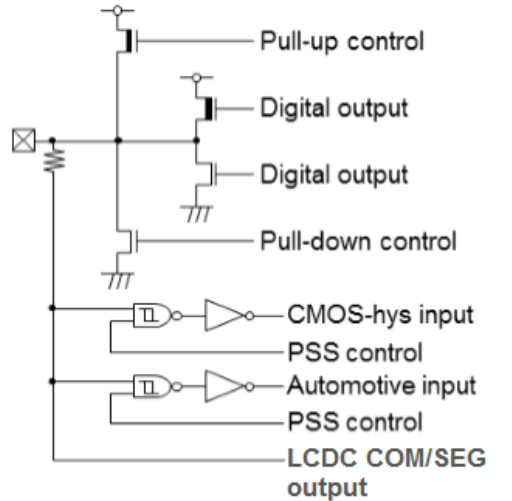
5.2 I/O Circuit Type

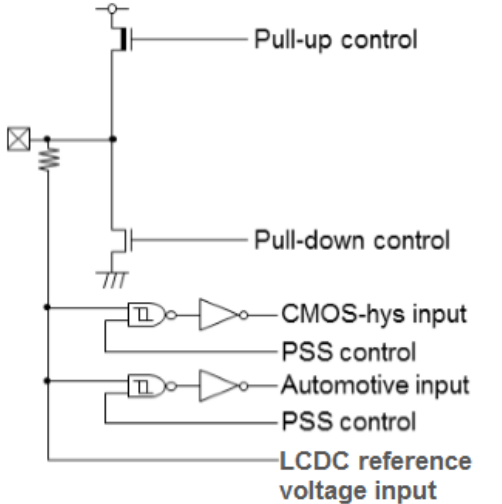
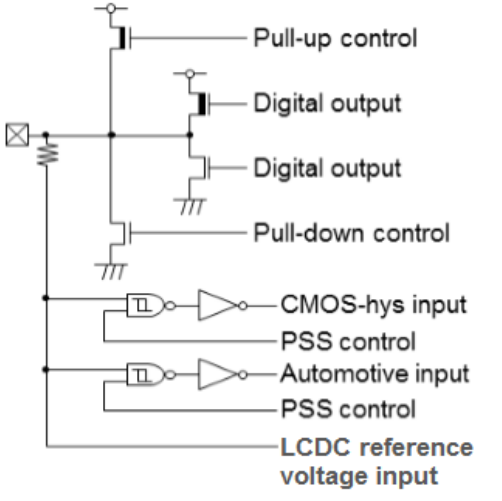
Table 5-2: I/O Circuit Types

| Type | Circuit | Remark |
|------|---|---|
| A |  | <ul style="list-style-type: none"> - GPIO port - Output 1 mA, 2 mA, or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |
| B |  | <ul style="list-style-type: none"> - GPIO port with analog input - Output 1 mA, 2 mA, or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |
| C |  | <ul style="list-style-type: none"> - GPIO port with analog input - Output 1 mA, 2 mA, 3 mA(I²C), or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |

| Type | Circuit | Remark |
|------|---|---|
| D |  | <ul style="list-style-type: none"> - JTAG_NTRST - 50 kΩ with pull-down resistor - TTL hysteresis input |
| E |  | <ul style="list-style-type: none"> - JTAG_TDI/TCK/TMS - 50 kΩ with pull-up resistor - TTL hysteresis input |
| F |  | <ul style="list-style-type: none"> - JTAG_TDO - Output 5 mA |
| G |  | <ul style="list-style-type: none"> - Mode input - CMOS hysteresis input |
| H |  | <ul style="list-style-type: none"> - Reset input - 50 kΩ with pull-up resistor - CMOS hysteresis input |
| I |  | <ul style="list-style-type: none"> - NMIX input - 50 kΩ with pull-up resistor - CMOS hysteresis input |
| K |  | <ul style="list-style-type: none"> - Main oscillation I/O - Feedback resistor = approx.2.1 MΩ |

| Type | Circuit | Remark |
|------|--|---|
| L |  <p> Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS/OSC control Automotive input PSS/OSC control OSC input PSS/OSC control Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS/OSC control Automotive input PSS/OSC control </p> | <ul style="list-style-type: none"> - Sub oscillation I/O shared GPIO port - Feedback resistor = approx. 13 MΩ - Output 1 mA, 2 mA, or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |
| M |  <p> Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS control Automotive input PSS control </p> | <ul style="list-style-type: none"> - GPIO port - Output 1 mA or 2 mA selectable ($V_{CC53_2} = 4.5\text{ V to }5.5\text{ V}$) - Output 5 mA or 15 mA selectable ($V_{CC53_2} = 3.0\text{ V to }3.6\text{ V}$) - 50 k$\Omega$ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |

| Type | Circuit | Remark |
|------|---|---|
| N |  <p>Labels in diagram: Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS control Automotive input PSS control Analog input</p> | <ul style="list-style-type: none"> - GPIO port with analog input - Output 1 mA or 2 mA selectable ($V_{CC53_2} = 4.5\text{ V to }5.5\text{ V}$) - Output 5 mA or 15 mA selectable ($V_{CC53_2} = 3.0\text{ V to }3.6\text{ V}$) - 50 k$\Omega$ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |
| O |  <p>Labels in diagram: Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS control Automotive input PSS control Analog input</p> | <ul style="list-style-type: none"> - GPIO port with analog input - Output 1 mA, 2 mA, 5 mA, or 30 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |
| P |  <p>Labels in diagram: Pull-up control Digital output Digital output Pull-down control CMOS-hys input PSS control Automotive input PSS control LCDC COM/SEG output</p> | <ul style="list-style-type: none"> - GPIO port with LCDC COM/SEG output - Output 1 mA, 2 mA or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |

| Type | Circuit | Remark |
|------|--|---|
| Q |  | <ul style="list-style-type: none"> - General-purpose input port with LCDC reference voltage input - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |
| R |  | <ul style="list-style-type: none"> - GPIO port with LCDC reference voltage input - Output 1 mA, 2 mA, or 5 mA selectable - 50 kΩ with pull-up resistor control - 50 kΩ with pull-down resistor control - CMOS hysteresis or automotive hysteresis input selectable |

5.3 Input Level Setting/ Output Drive Capacity Setting

(1) When Power Supply Pin of Each I/O is Used at 5 V

Table 5-3-1: Input Level Setting/ Output Drive Capacity Setting

| Pin No. of LQFP/TEQFP Package | | Port Name | Input Level Setting | | Output Drive Capacity Setting | | | | Power of Pin (Pin Group) | Remark |
|-------------------------------|---------|-----------|---------------------|------------|-------------------------------|------|---|------|--------------------------|---------------------|
| 144-Pin | 176-Pin | | | | | | | | | |
| 2 | 2 | P0_00 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | V _{CC53_1} | |
| 3 | 3 | P0_01 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 4 | 4 | P0_02 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 5 | 5 | P0_03 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 6 | 6 | P0_04 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 7 | 7 | P0_05 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 8 | 8 | P0_06 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 11 | 19 | P0_07 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 12 | 20 | P0_08 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 13 | 21 | P0_09 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 14 | 22 | P0_10 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 15 | 23 | P0_11 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 16 | 24 | P0_12 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 19 | 27 | P0_13 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | V _{CC53_2} |
| 20 | 28 | P0_14 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 21 | 29 | P0_15 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 22 | 30 | P0_16 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 23 | 31 | P0_17 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 26 | 34 | P0_18 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 28 | 36 | P0_19 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 29 | 37 | P0_20 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 30 | 38 | P0_21 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 31 | 39 | P0_22 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 32 | 40 | P0_23 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 35 | 43 | P0_24 | CMOS-hys | Automotive | 1 mA | 2 mA | - | - | | |
| 50 | 64 | P0_25 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | V _{CC5} | *2 |
| 51 | 65 | P0_26 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | *2 |
| 52 | 66 | P0_27 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 53 | 67 | P0_28 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 54 | 68 | P0_29 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 56 | 70 | P0_30 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 57 | 71 | P0_31 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 60 | 74 | P1_00 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 61 | 75 | P1_01 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 62 | 76 | P1_02 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | *1 |
| 63 | 77 | P1_03 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | *1 |
| 64 | 78 | P1_04 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 65 | 79 | P1_05 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | *1 | |
| 66 | 80 | P1_06 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | *1 | |

| Pin No. of LQFP/TEQFP Package | | Port Name | Input Level Setting | | Output Drive Capacity Setting | | | | Power of Pin (Pin Group) | Remark |
|-------------------------------|---------|-----------|---------------------|------------|-------------------------------|------|------|-------|--------------------------|------------|
| 144-Pin | 176-Pin | | | | | | | | | |
| 67 | 81 | P1_07 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | V _{CC5} | |
| 74 | 96 | P1_08 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 77 | 101 | P1_09 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 80 | 104 | P1_10 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | DV _{CC} | |
| 81 | 105 | P1_11 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 82 | 106 | P1_12 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 83 | 107 | P1_13 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 84 | 108 | P1_14 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 85 | 109 | P1_15 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 86 | 110 | P1_16 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 87 | 111 | P1_17 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 90 | 114 | P1_18 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 91 | 115 | P1_19 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 92 | 116 | P1_20 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 93 | 117 | P1_21 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 94 | 118 | P1_22 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 95 | 119 | P1_23 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 96 | 120 | P1_24 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 97 | 121 | P1_25 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 100 | 124 | P1_26 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 101 | 125 | P1_27 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 102 | 126 | P1_28 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 103 | 127 | P1_29 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 104 | 128 | P1_30 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 105 | 129 | P1_31 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | *2 |
| 106 | 130 | P2_00 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 107 | 131 | P2_01 | CMOS-hys | Automotive | 1 mA | 2 mA | 5 mA | 30 mA | | |
| 112 | 142 | P2_02 | CMOS-hys | Automotive | - | | | | V _{CC53_1} | Input only |
| 113 | 143 | P2_03 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 114 | 144 | P2_04 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 115 | 145 | P2_05 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 116 | 146 | P2_06 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 117 | 147 | P2_07 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 118 | 148 | P2_08 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 121 | 151 | P2_09 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 122 | 152 | P2_10 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 123 | 153 | P2_11 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 124 | 154 | P2_12 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 125 | 155 | P2_13 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 126 | 156 | P2_14 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 127 | 157 | P2_15 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 128 | 158 | P2_16 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | *2 |

| Pin No. of LQFP/TEQFP Package | | Port Name | Input Level Setting | | Output Drive Capacity Setting | | | | Power of Pin (Pin Group) | Remark |
|-------------------------------|---------|-----------|---------------------|------------|-------------------------------|------|---|------|--------------------------|--------|
| 144-Pin | 176-Pin | | | | | | | | | |
| 129 | 159 | P2_17 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | V _{CC53_1} | *2 |
| 130 | 160 | P2_18 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 131 | 161 | P2_19 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 132 | 162 | P2_20 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 133 | 163 | P2_21 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 136 | 166 | P2_22 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 137 | 167 | P2_23 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | *2 |
| 138 | 168 | P2_24 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | *2 |
| 139 | 169 | P2_25 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 140 | 170 | P2_26 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 141 | 173 | P2_27 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 142 | 174 | P2_28 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| 143 | 175 | P2_29 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 9 | P3_00 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | V _{CC5} | |
| - | 10 | P3_01 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 11 | P3_02 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 14 | P3_03 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 15 | P3_04 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 16 | P3_05 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 17 | P3_06 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 18 | P3_07 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 58 | P3_08 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 59 | P3_09 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 60 | P3_10 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 61 | P3_11 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 62 | P3_12 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 63 | P3_13 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 82 | P3_14 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 83 | P3_15 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 90 | P3_16 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 91 | P3_17 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 92 | P3_18 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 93 | P3_19 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 94 | P3_20 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 95 | P3_21 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 97 | P3_22 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 98 | P3_23 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 134 | P3_24 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | V _{CC53_1} | |
| - | 135 | P3_25 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 138 | P3_26 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 139 | P3_27 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 140 | P3_28 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |
| - | 141 | P3_29 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |

| Pin No. of LQFP/TEQFP Package | | Port Name | Input Level Setting | | Output Drive Capacity Setting | | | | Power of Pin (Pin Group) | Remark |
|-------------------------------|---------|-----------|---------------------|------------|-------------------------------|------|---|------|--------------------------|--------|
| 144-Pin | 176-Pin | | | | | | | | | |
| - | 171 | P3_30 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | V _{CC53_1} | |
| - | 172 | P3_31 | CMOS-hys | Automotive | 1 mA | 2 mA | - | 5 mA | | |

Note:

- "CMOS-hys" is CMOS hysteresis input level.
- "Automotive" is automotive hysteresis input level.
- *1 When the port setting is "SDA or SCL function setting", the output drive capacity is "I²C". Then, the port status is to be the open drain, and IOL is to be 3 mA.
- *2 When the port setting is "SDA or SCL function setting", the port status is to be the pseudo open drain, and IOL is to be the configured value for "Output Drive Capacity Setting".
- The "Output Drive Capacity Setting" values in above table are IOH/IOL values, when port power supply voltage is 5 V. For details of drive capability, see section [7.3 DC Characteristics](#).

(2) When Power Supply Pin of Each I/O is Used at 3.3 V

Table 5-3-2: Input Level Setting/ Output Drive Capacity Setting

| Pin No. of LQFP/TEQFP Package | | Port Name | Input Level Setting | | Output Drive Capacity Setting | | | | Power of Pin (Pin Group) | Remark | |
|-------------------------------|---------|-----------|---------------------|------------|-------------------------------|------|------|-------|--------------------------|---------------------|----|
| 144-Pin | 176-Pin | | | | | | | | | | |
| 2 | 2 | P0_00 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | V _{CC53_1} | | |
| 3 | 3 | P0_01 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 4 | 4 | P0_02 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 5 | 5 | P0_03 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 6 | 6 | P0_04 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 7 | 7 | P0_05 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 8 | 8 | P0_06 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 11 | 19 | P0_07 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 12 | 20 | P0_08 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 13 | 21 | P0_09 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 14 | 22 | P0_10 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 15 | 23 | P0_11 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 16 | 24 | P0_12 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 19 | 27 | P0_13 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | V _{CC53_2} | |
| 20 | 28 | P0_14 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 21 | 29 | P0_15 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 22 | 30 | P0_16 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 23 | 31 | P0_17 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 26 | 34 | P0_18 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 28 | 36 | P0_19 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 29 | 37 | P0_20 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 30 | 38 | P0_21 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 31 | 39 | P0_22 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 32 | 40 | P0_23 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 35 | 43 | P0_24 | CMOS-hys | Automotive | - | - | 5 mA | 15 mA | | | |
| 50 | 64 | P0_25 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | V _{CC5} | | *2 |
| 51 | 65 | P0_26 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | *2 |
| 52 | 66 | P0_27 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 53 | 67 | P0_28 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 54 | 68 | P0_29 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 56 | 70 | P0_30 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 57 | 71 | P0_31 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 60 | 74 | P1_00 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 61 | 75 | P1_01 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 62 | 76 | P1_02 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | *1 | |
| 63 | 77 | P1_03 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | *1 | |
| 64 | 78 | P1_04 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | | |
| 65 | 79 | P1_05 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | *1 | |
| 66 | 80 | P1_06 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | *1 | |

| Pin No. of LQFP/TEQFP Package | | Port Name | Input Level Setting | | Output Drive Capacity Setting | | | | Power of Pin (Pin Group) | Remark |
|-------------------------------|---------|-----------|---------------------|------------|-------------------------------|------|------|------|--------------------------|------------|
| 144-Pin | 176-Pin | | | | | | | | | |
| 67 | 81 | P1_07 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | V _{CC5} | |
| 74 | 96 | P1_08 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 77 | 101 | P1_09 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 80 | 104 | P1_10 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | DV _{CC} | |
| 81 | 105 | P1_11 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 82 | 106 | P1_12 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | *2 |
| 83 | 107 | P1_13 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | *2 |
| 84 | 108 | P1_14 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 85 | 109 | P1_15 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 86 | 110 | P1_16 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 87 | 111 | P1_17 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 90 | 114 | P1_18 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | *2 |
| 91 | 115 | P1_19 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | *2 |
| 92 | 116 | P1_20 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 93 | 117 | P1_21 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | *2 |
| 94 | 118 | P1_22 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | *2 |
| 95 | 119 | P1_23 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 96 | 120 | P1_24 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 97 | 121 | P1_25 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 100 | 124 | P1_26 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 101 | 125 | P1_27 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | *2 |
| 102 | 126 | P1_28 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | *2 |
| 103 | 127 | P1_29 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 104 | 128 | P1_30 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | *2 | |
| 105 | 129 | P1_31 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | *2 | |
| 106 | 130 | P2_00 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 107 | 131 | P2_01 | CMOS-hys | Automotive | 0.5 mA | 1 mA | 2 mA | - | | |
| 112 | 142 | P2_02 | CMOS-hys | Automotive | - | | | | | Input only |
| 113 | 143 | P2_03 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | V _{CC53_1} | |
| 114 | 144 | P2_04 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 115 | 145 | P2_05 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 116 | 146 | P2_06 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 117 | 147 | P2_07 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 118 | 148 | P2_08 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 121 | 151 | P2_09 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 122 | 152 | P2_10 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 123 | 153 | P2_11 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 124 | 154 | P2_12 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 125 | 155 | P2_13 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 126 | 156 | P2_14 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 127 | 157 | P2_15 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 128 | 158 | P2_16 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | *2 |

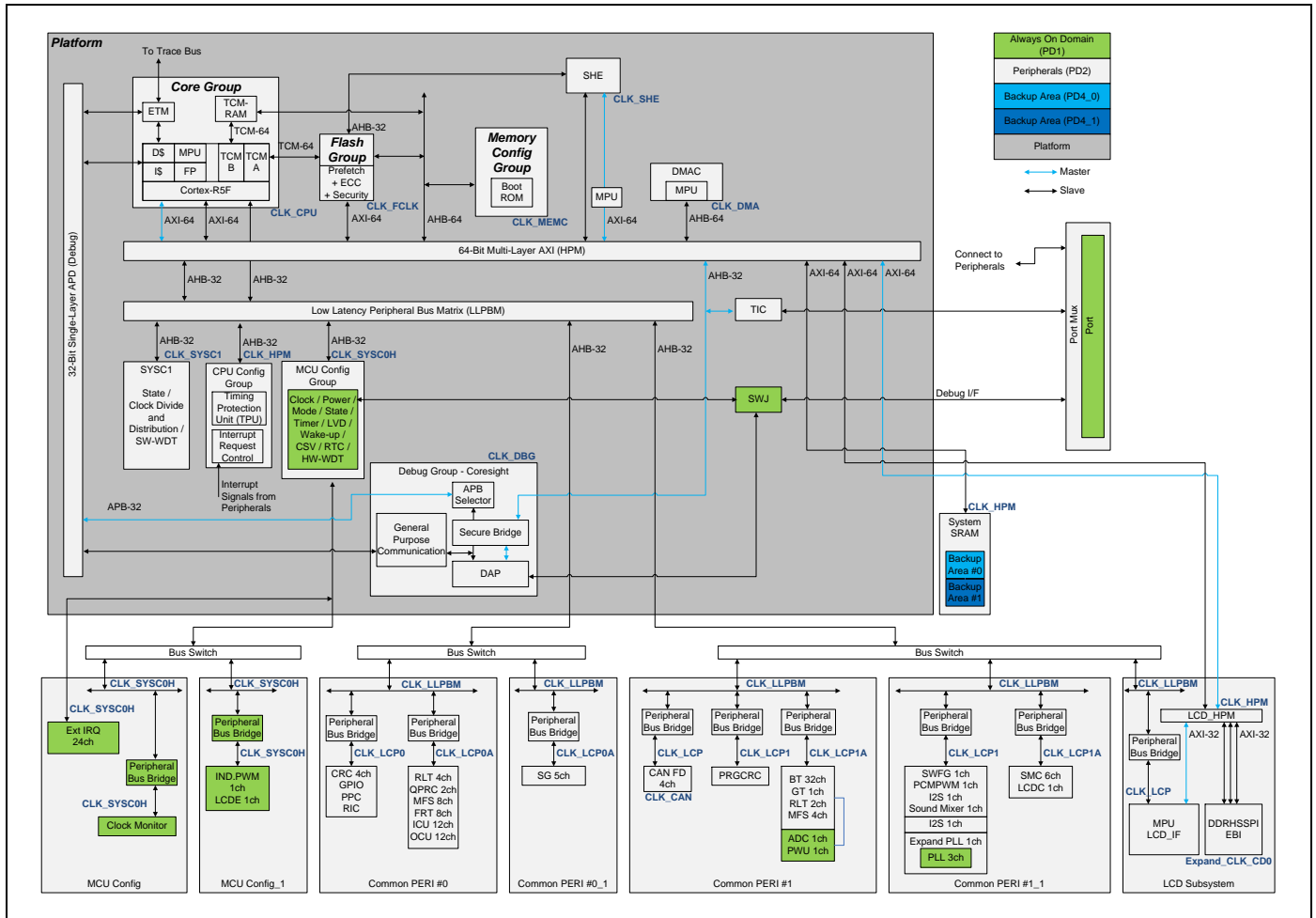
| Pin No. of LQFP/TEQFP Package | | Port Name | Input Level Setting | | Output Drive Capacity Setting | | | | Power of Pin (Pin Group) | Remark |
|-------------------------------|---------|-----------|---------------------|------------|-------------------------------|------|---|------|--------------------------|--------|
| 144-Pin | 176-Pin | | | | | | | | | |
| 129 | 159 | P2_17 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | V _{CC53_1} | *2 |
| 130 | 160 | P2_18 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 131 | 161 | P2_19 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 132 | 162 | P2_20 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 133 | 163 | P2_21 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 136 | 166 | P2_22 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 137 | 167 | P2_23 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | *2 |
| 138 | 168 | P2_24 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | *2 |
| 139 | 169 | P2_25 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 140 | 170 | P2_26 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 141 | 173 | P2_27 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 142 | 174 | P2_28 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| 143 | 175 | P2_29 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 9 | P3_00 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | V _{CC5} | |
| - | 10 | P3_01 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 11 | P3_02 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 14 | P3_03 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 15 | P3_04 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 16 | P3_05 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 17 | P3_06 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 18 | P3_07 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 58 | P3_08 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 59 | P3_09 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 60 | P3_10 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 61 | P3_11 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 62 | P3_12 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 63 | P3_13 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 82 | P3_14 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 83 | P3_15 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 90 | P3_16 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 91 | P3_17 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 92 | P3_18 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 93 | P3_19 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 94 | P3_20 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 95 | P3_21 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 97 | P3_22 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 98 | P3_23 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 134 | P3_24 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | V _{CC53_1} | |
| - | 135 | P3_25 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 138 | P3_26 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 139 | P3_27 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 140 | P3_28 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |
| - | 141 | P3_29 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |

| Pin No. of LQFP/TEQFP Package | | Port Name | Input Level Setting | | Output Drive Capacity Setting | | | | Power of Pin (Pin Group) | Remark |
|-------------------------------|---------|-----------|---------------------|------------|-------------------------------|------|---|------|--------------------------|--------|
| 144-Pin | 176-Pin | | | | | | | | | |
| - | 171 | P3_30 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | V _{CC53_1} | |
| - | 172 | P3_31 | CMOS-hys | Automotive | 0.5 mA | 1 mA | - | 2 mA | | |

Note:

- "CMOS-hys" is CMOS hysteresis input level.
- "Automotive" is automotive hysteresis input level.
- *1 When the port setting is "SDA or SCL function setting", the output drive capacity is "I²C". Then, the port status is to be the open drain, and IOL is to be 3 mA.
- *2 When the port setting is "SDA or SCL function setting", the port status is to be the pseudo open drain, and IOL is to be the configured value for "Output Drive Capacity Setting".
- The "Output Drive Capacity Setting" values in above table are IOH/IOL values, when port power supply voltage is 3.3 V. For details of drive capability, see section 7.3 DC Characteristics.

6. Block Diagram



7. Electrical Characteristics

7.1 Absolute Maximum Ratings

| Parameter | Symbol | Value | | Unit | Remarks |
|--|----------------------|-----------------------|---------------------------|------|--|
| | | Min | Max | | |
| Power supply voltage ^{*1, *2} | V _{CC5} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | |
| | V _{CC53_1} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | V _{CC53_1} ≤ V _{CC5} |
| | V _{CC53_2} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | V _{CC53_2} ≤ V _{CC5} |
| | DV _{CC} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | |
| Analog supply voltage ^{*1, *2} | AV _{CC5} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | AV _{CC5} ≤ V _{CC5} |
| Analog reference voltage ^{*1} | AV _{RH5} | V _{SS} - 0.3 | V _{SS} + 6.0 | V | AV _{RH5} ≤ AV _{CC5} |
| Input voltage ^{*1} | V _{I1} | V _{SS} - 0.3 | V _{CC5} + 0.3 | V | GPIO of V _{CC5} ^{*6} MODE, RSTX, NMIX, JTAG_TDI, JTAG_TMS, JTAG_TCK, JTAG_NTRST |
| | V _{I2} | V _{SS} - 0.3 | V _{CC53_1} + 0.3 | V | GPIO of V _{CC53_1} ^{*6} |
| | V _{I3} | V _{SS} - 0.3 | V _{CC53_2} + 0.3 | V | GPIO of V _{CC53_2} ^{*6} |
| | V _{I4} | V _{SS} - 0.3 | DV _{CC} + 0.3 | V | GPIO of DV _{CC} ^{*6} |
| Analog pin input voltage ^{*1} | V _{IA} | V _{SS} - 0.3 | AV _{CC5} + 0.3 | V | ^{*8} |
| Output voltage ^{*1} | V _{O1} | V _{SS} - 0.3 | V _{CC5} + 0.3 | V | GPIO of V _{CC5} ^{*6, *8} JTAG_TDO |
| | V _{O2} | V _{SS} - 0.3 | V _{CC53_1} + 0.3 | V | GPIO of V _{CC53_1} ^{*6} |
| | V _{O3} | V _{SS} - 0.3 | V _{CC53_2} + 0.3 | V | GPIO of V _{CC53_2} ^{*6, *8} |
| | V _{O4} | V _{SS} - 0.3 | DV _{CC} + 0.3 | V | GPIO of DV _{CC} ^{*6, *8} |
| Maximum clamp current | I _{CLAMP} | - | 4 | mA | ^{*7, *A} |
| Total maximum clamp current | Σ I _{CLAMP} | - | 20 | mA | ^{*7, *A} |
| L-level maximum output current ^{*3} | I _{OL1} | - | 3.5 | mA | When setting is 1 mA ALL GPIO ^{*6} |
| | I _{OL2} | - | 7 | mA | When setting is 2 mA ALL GPIO ^{*6} |
| | I _{OL3} | - | 10 | mA | When setting is 5 mA GPIO of V _{CC5} /V _{CC53_1} /DV _{CC} ^{*6} |
| | I _{OL3} | - | 10 | mA | When setting is 5 mA GPIO of V _{CC53_2} ^{*6} |
| | I _{OL4} | - | 20 | mA | When setting is 15 mA GPIO of V _{CC53_2} ^{*6} |
| | I _{OL5} | - | 40 | mA | When setting is 30 mA GPIO of DV _{CC} ^{*6} |
| | I _{OL6} | - | 8 | mA | When setting is 3 mA GPIO of V _{CC5} ^{*6} |

| Parameter | Symbol | Value | | Unit | Remarks |
|--|--------------------|-------|------|------|---|
| | | Min | Max | | |
| L-level average output current ^{*4} | I _{OLAV1} | - | 1 | mA | When setting is 1 mA ALL GPIO ^{*6} |
| | I _{OLAV2} | - | 2 | mA | When setting is 2 mA ALL GPIO ^{*6} |
| | I _{OLAV3} | - | 5 | mA | When setting is 5 mA GPIO of V _{CC5} /V _{CC53_1} /DV _{CC} ^{*6} |
| | I _{OLAV3} | - | 5 | mA | When setting is 5 mA GPIO of V _{CC53_2} ^{*6} |
| | I _{OLAV4} | - | 15 | mA | When setting is 15 mA GPIO of V _{CC53_2} ^{*6} |
| | I _{OLAV5} | - | 30 | mA | When setting is 30 mA GPIO of DV _{CC} ^{*6} |
| | I _{OLAV6} | - | 3 | mA | When setting is 3 mA (I ² C) GPIO of V _{CC5} ^{*6} |
| L-level total output current ^{*5} | ΣI _{OL1} | - | 50 | mA | GPIO of (V _{CC5} + V _{CC53_1} + V _{CC53_2}) ^{*6} |
| | ΣI _{OL2} | - | 250 | mA | GPIO of DV _{CC} ^{*6} |
| H-level maximum output current ^{*3} | I _{OH1} | - | -3.5 | mA | When setting is 1 mA ALL GPIO ^{*6} |
| | I _{OH2} | - | -7 | mA | When setting is 2 mA ALL GPIO ^{*6} |
| | I _{OH3} | - | -10 | mA | When setting is 5 mA GPIO of V _{CC5} /V _{CC53_1} /DV _{CC} ^{*6} |
| | I _{OH3} | - | -10 | mA | When setting is 5 mA GPIO of V _{CC53_2} ^{*6} |
| | I _{OH4} | - | -20 | mA | When setting is 15 mA GPIO of V _{CC53_2} ^{*6} |
| | I _{OH5} | - | -40 | mA | When setting is 30 mA GPIO of DV _{CC} ^{*6} |
| H-level average output current ^{*4} | I _{OHAV1} | - | -1 | mA | When setting is 1 mA ALL GPIO ^{*6} |
| | I _{OHAV2} | - | -2 | mA | When setting is 2 mA ALL GPIO ^{*6} |
| | I _{OHAV3} | - | -5 | mA | When setting is 5 mA GPIO of V _{CC5} /V _{CC53_1} /DV _{CC} ^{*6} |
| | I _{OHAV3} | - | -5 | mA | When setting is 5 mA GPIO of V _{CC53_2} ^{*6} |
| | I _{OHAV4} | - | -15 | mA | When setting is 15 mA GPIO of V _{CC53_2} ^{*6} |
| | I _{OHAV5} | - | -30 | mA | When setting is 30 mA GPIO of DV _{CC} ^{*6} |
| H-level total output current ^{*5} | ΣI _{OH1} | - | -50 | mA | GPIO of (V _{CC5} + V _{CC53_1} + V _{CC53_2}) ^{*6} |
| | ΣI _{OH2} | - | -250 | mA | GPIO of DV _{CC} ^{*6} |
| Power consumption | P _D | - | 1100 | mW | TEQFP package |
| | | - | 950 | mW | LQFP package |
| Operating temperature | T _A | -40 | 105 | °C | |
| Storage temperature | T _{stg} | -55 | 150 | °C | |

*1: These parameters are based on the condition that V_{SS} = AV_{SS} = DV_{SS} = 0.0 V.

*2: [For S6J33xxxS or S6J33xxxT or S6J33xxxU or S6J33xxxV part number]

Take care that DV_{CC}, AV_{CC5}, V_{CC53_1}, V_{CC53_2} do not exceed V_{CC5}.

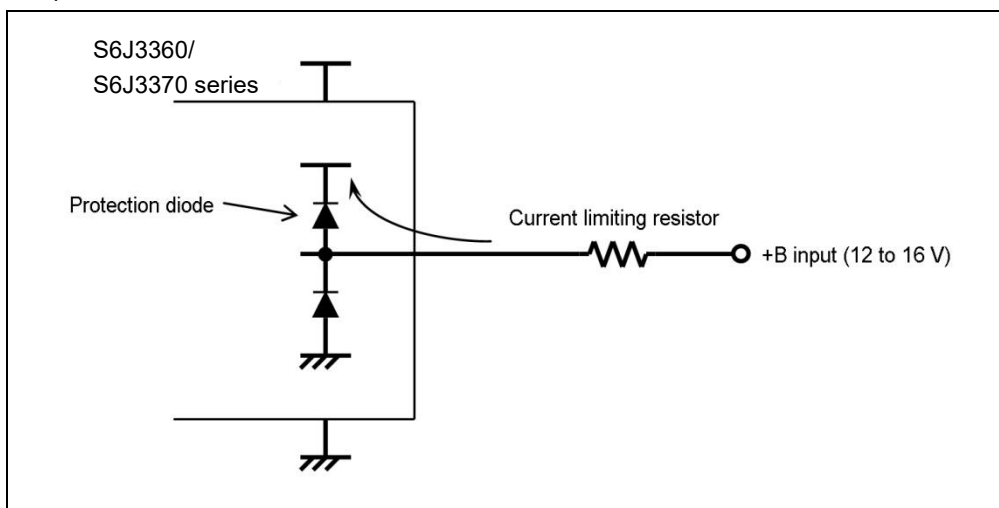
[For S6J33xxxA or S6J33xxxE or S6J33xxxC or S6J33xxxG part number]

Take care that AV_{CC5} , V_{CC53_1} , V_{CC53_2} do not exceed V_{CC5} .

DV_{CC} is possible to exceed V_{CC5} .

- *3: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
 - *4: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10-ms period. The average value is the operation current \times the operation ratio.
 - *5: The total output current is defined as the maximum current value flowing through all of corresponding pins.
 - *6: For the details of GPIO group and setting, See section [5.3 Input Level Setting/ Output Drive Capacity Setting](#).
 - *7: VI or VO should never exceed the specified ratings. However, if the maximum current to/from an input is limited by a suitable external resistor, the ICLAMP rating supersedes the VI rating.
 - *8: Take care that the output voltage does not exceed $AV_{CC5} + 0.3$ V because ADC Analog input pins (ADC0_ANx) are internally connected to the analog elements. In case of use ADC, analog input voltage do not exceed AV_{CC5} .
- *A: Relevant pins: All general-purpose ports and analog input pins
- Corresponding pins: all general-purpose ports
 - Use within recommended operating conditions.
 - Use at DC voltage (current).
 - The +B signal should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
 - The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneous or constant +B signal input.
 - When the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
 - If the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may not operate completely.
 - If the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
 - Do not leave + B input pins open.

Example of a recommended circuit



WARNING:

- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

7.2 Recommended Operating Conditions

(1) Recommended Operation Conditions for S6J33nnnXnnnnnnnn (X = S, T, U, V)

| Parameter | Symbol | Value | | Unit | Remarks |
|-----------------------------------|---|---|------------------|------|---|
| | | Min | Max | | |
| Supply voltage | V _{CC5} | 4.5 | 5.5 | V | Recommended operation assurance range (case1) ^{*1} |
| | V _{CC53_1} | 4.5 | 5.5 | V | |
| | | 3.0 | 3.6 | V | |
| | V _{CC53_2} | 4.5 | 5.5 | V | |
| | | 3.0 | 3.6 | V | |
| | DV _{CC} | 4.5 | 5.5 | V | |
| | AV _{CC5} | 4.5 | 5.5 | V | |
| | Recommended operation assurance range (case2) ^{*1} | V _{CC5} | 3.0 | 3.6 | V |
| | | V _{CC53_1} | 3.0 | 3.6 | V |
| | | V _{CC53_2} | 3.0 | 3.6 | V |
| | | DV _{CC} | 3.0 | 3.6 | V |
| | | AV _{CC5} | 3.0 | 3.6 | V |
| | | Operation assurance range ^{*2} | V _{CC5} | 2.7 | 5.5 |
| | V _{CC53_1} | | 2.7 | 5.5 | V |
| | V _{CC53_2} | | 2.7 | 5.5 | V |
| DV _{CC} | 2.7 | | 5.5 | V | |
| AV _{CC5} | 2.7 | | 5.5 | V | |
| Smoothing capacitor ^{*3} | C _S | 4.7 | | μF | Tolerance of up to ±40 % |
| Operating temperature | T _A | -40 | 105 | °C | |

(2) Recommended Operation Conditions for S6J33nnnXnnnnnnnn (X = A, E, C, G)

| Parameter | Symbol | Value | | Unit | Remarks |
|-----------------------------------|---|---|------------------|------|---|
| | | Min | Max | | |
| Supply voltage | V _{CC5} | 4.5 | 5.5 | V | Recommended operation assurance range (case1) ^{*1} |
| | V _{CC53_1} | 4.5 | 5.5 | V | |
| | | 3.0 | 3.6 | V | |
| | V _{CC53_2} | 4.5 | 5.5 | V | |
| | | 3.0 | 3.6 | V | |
| | DV _{CC} | 4.5 | 5.5 | V | |
| | AV _{CC5} | 4.5 | 5.5 | V | |
| | Recommended operation assurance range (case2) ^{*1} | V _{CC5} | 3.0 | 3.6 | V |
| | | V _{CC53_1} | 3.0 | 3.6 | V |
| | | V _{CC53_2} | 3.0 | 3.6 | V |
| | | DV _{CC} | 3.0 | 3.6 | V |
| | | AV _{CC5} | 3.0 | 3.6 | V |
| | | Recommended operation assurance range (case3) ^{*1} | V _{CC5} | 3.0 | 3.6 |
| | V _{CC53_1} | | 3.0 | 3.6 | V |
| | V _{CC53_2} | | 3.0 | 3.6 | V |
| | DV _{CC} | | 4.5 | 5.5 | V |
| | AV _{CC5} | | 3.0 | 3.6 | V |
| | Operation assurance range ^{*2} | | V _{CC5} | 2.7 | 5.5 |
| V _{CC53_1} | | 2.7 | 5.5 | V | |
| V _{CC53_2} | | 2.7 | 5.5 | V | |
| DV _{CC} | | 2.7 | 5.5 | V | |
| AV _{CC5} | | 2.7 | 5.5 | V | |
| Smoothing capacitor ^{*3} | C _S | 4.7 | | μF | Tolerance of up to ±40 % |
| Operating temperature | T _A | -40 | 105 | °C | |

Notes:

*1: Recommendation of S6J3360/S6J3370 series power supply voltage combination is as follows.

| | VCC5 [V] | VCC53_1 [V] | VCC53_2 [V] | DVCC [V] | AVCC5 [V] |
|-------|----------|-------------|-------------|----------|-----------|
| Case1 | 5.0 | 5.0 | 5.0 | 5.0 | 5.0 |
| | 5.0 | 5.0 | 3.3 | 5.0 | 5.0 |
| | 5.0 | 3.3 | 5.0 | 5.0 | 5.0 |
| | 5.0 | 3.3 | 3.3 | 5.0 | 5.0 |
| Case2 | 3.3 | 3.3 | 3.3 | 3.3 | 3.3 |
| Case3 | 3.3 | 3.3 | 3.3 | 5.0 | 3.3 |

Other voltage combinations are out of recommendation. The typical values which are described in the above table.

• In all cases, recommended power supply sequence is the following.

VCC5 -> [DVCC or VCC53_1 or VCC53_2 or AVCC5]*

* Note that power supplies inside "[]" can be turned on in arbitrary order.

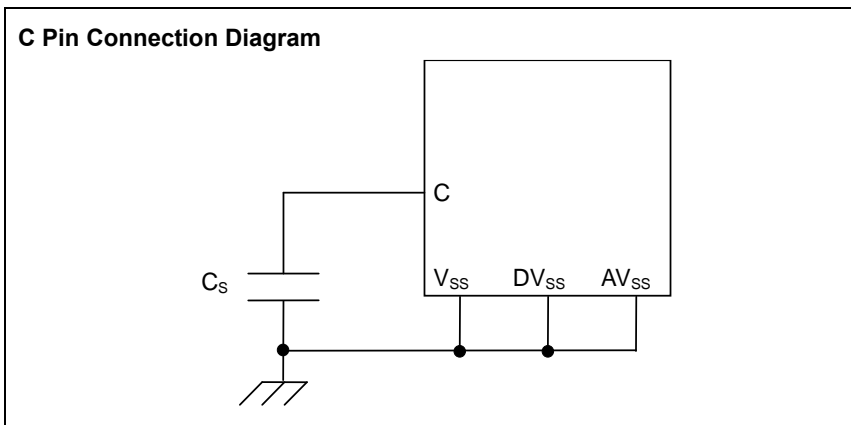
For details of the power supply sequence, see section 7.4.5.2 Power Supply Sequence.

*2: When it is used outside recommended operation guarantee range (range of the operation guarantee), contact your sales representative.

The initial detection voltage of the external low voltage detection is 2.6 V±3.5 % (2.51 V to 2.69 V).

This LVD setting and internal LVD (LVDL0/LVDL1) cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.

*3: For the connections of smoothing capacitor C_s, see the following diagram.



WARNING:

- The recommended operating conditions are required to ensure the normal operation of the semiconductor device. All the device's electrical characteristics are guaranteed when the device is operated under these conditions.
- Any use of semiconductor devices will be under their recommended operating conditions.
- Operation under any conditions other than these conditions may adversely affect reliability of device and can result in device failure.
- No guarantee is made with respect to any use, operating conditions, or combinations not represented on this datasheet. If you want to operate the application under any conditions other than listed here, contact the sales representatives.

Notes:

- The following conditions should be satisfied in order to facilitate heat dissipation:
 1. Four or more layers PCB should be used.
 2. The area of PCB should be 114.3 mm x 76.2 mm or more, and the thickness should be 1.6 mm or more. (JEDEC standard)
 3. One layer of middle layers at least should be used for dedicated layer to radiate heat with residual copper rate 90 % or more. The layer can be used for system ground.
 4. 35 % or more of the die stage area which is exposed at back surface of package should be soldered to a part of 1st layer.
 5. Set via on PCB surface to ensure heat dissipation in order to connect die joint stage with heat dissipation stage by via. Or the part of 1st layer should be connected to the dedicated heat radiation layer with more than 10 thermal via holes.

Mounting condition is operation recommendation condition from JEDEC.

Figure 7-1: Example Thermal Via Holes on PCB.



Notes:

- [Figure 7-1](#) is a schematic diagram showing PCB in section.
- [Figure 7-2](#), [Figure 7-3](#), [Figure 7-4](#) in the following pages are recommended land patterns for each package series. Thermal via holes should closely be placed and aligned with lands.
- If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

Figure 7-2: Example Land Pattern for TEQFP176 (LEF176)

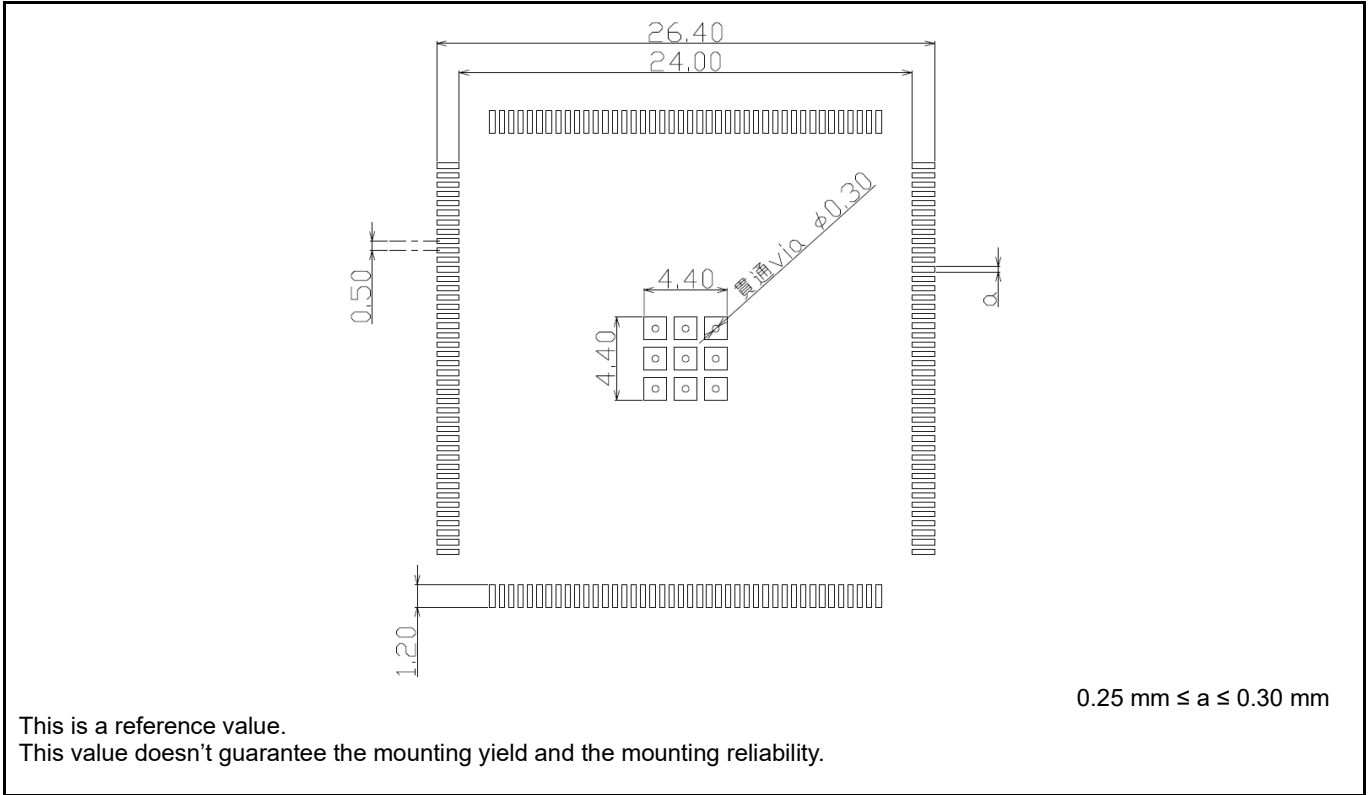


Figure 7-3: Example Land Pattern for TEQFP144 (LEJ144)

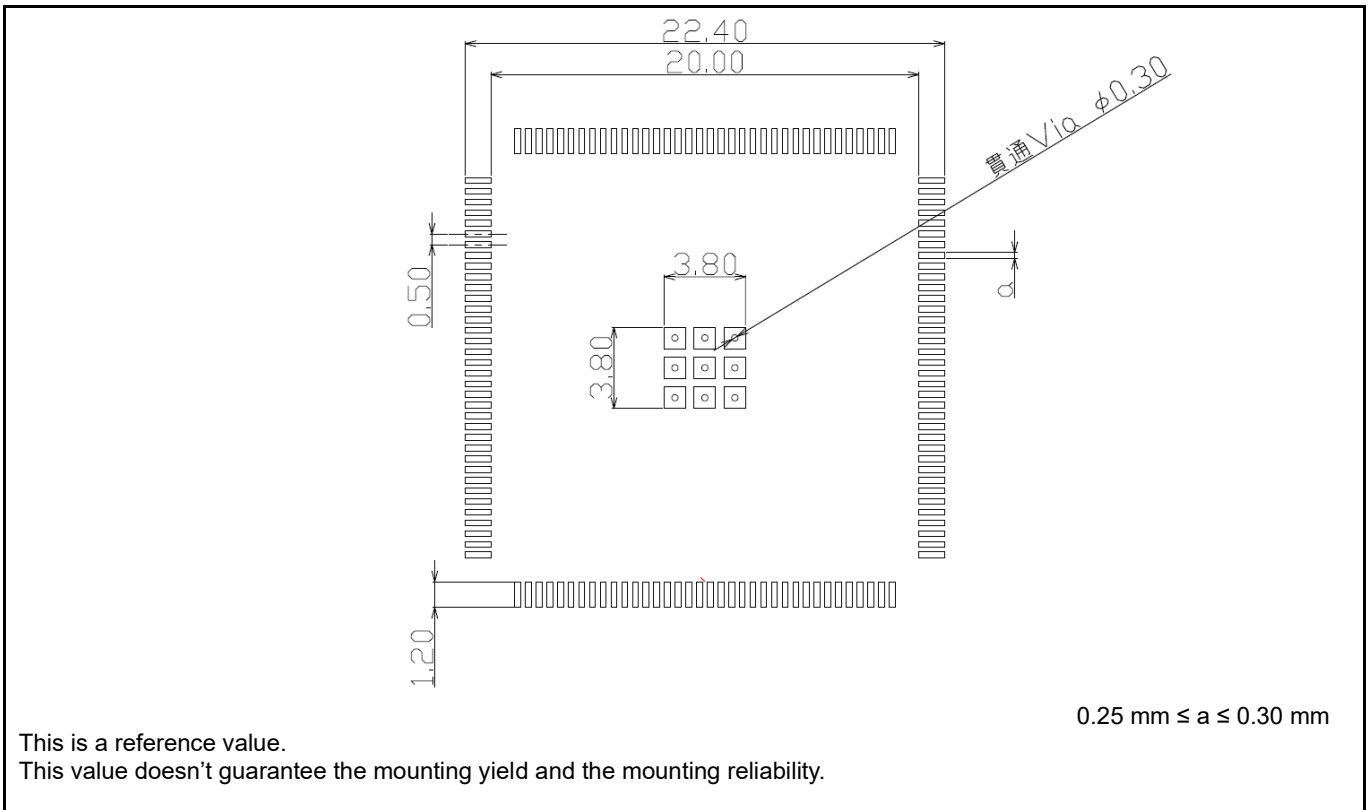
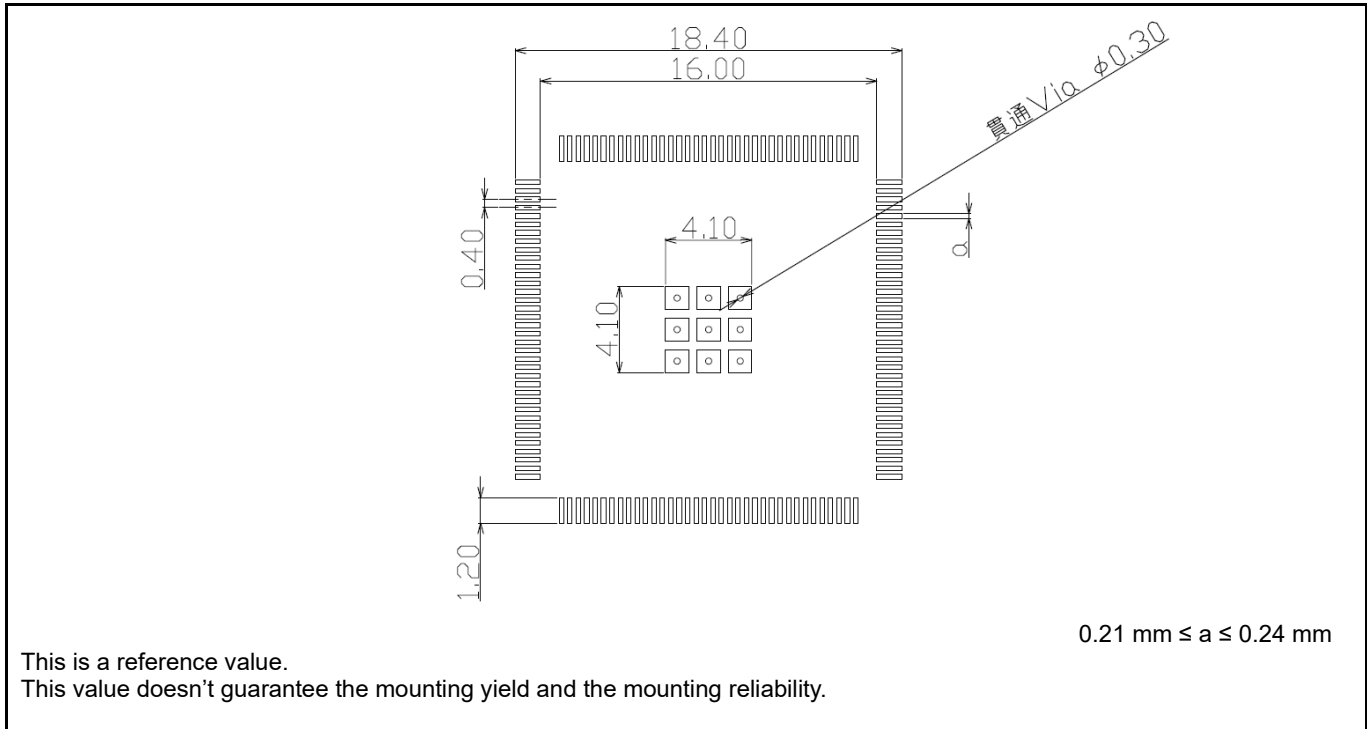


Figure 7-4: Example Land Pattern for TEQFP144 (LEG144)



7.3 DC Characteristics

7.3.1 Port Function Characteristics

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name*1 | Conditions | Value | | | Unit | Remarks |
|-------------------------|-------------------|--|---|---------------------------|-----|---------------------------|------|---------|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | V _{IH1} | GPIO of V _{CC5} | CMOS hysteresis input level is selected | 0.7 x V _{CC5} | - | V _{CC5} + 0.3 | V | |
| | V _{IH2} | | Automotive input level is selected | 0.8 x V _{CC5} | - | V _{CC5} + 0.3 | V | |
| | V _{IH3} | GPIO of V _{CC53_1} | CMOS hysteresis input level is selected | 0.7 x V _{CC53_1} | - | V _{CC53_1} + 0.3 | V | |
| | V _{IH4} | | Automotive input level is selected | 0.8 x V _{CC53_1} | - | V _{CC53_1} + 0.3 | V | |
| | V _{IH5} | GPIO of V _{CC53_2} | CMOS hysteresis input level is selected | 0.7 x V _{CC53_2} | - | V _{CC53_2} + 0.3 | V | |
| | V _{IH6} | | Automotive input level is selected | 0.8 x V _{CC53_2} | - | V _{CC53_2} + 0.3 | V | |
| | V _{IH7} | GPIO of DV _{CC} | CMOS hysteresis input level is selected | 0.7 x DV _{CC} | - | DV _{CC} + 0.3 | V | |
| | V _{IH8} | | Automotive input level is selected | 0.8 x DV _{CC} | - | DV _{CC} + 0.3 | V | |
| | V _{IH9} | RSTX, NMIX | CMOS hysteresis input level | 0.7 x V _{CC5} | - | V _{CC5} + 0.3 | V | |
| | V _{IH10} | MODE | CMOS hysteresis input level | 0.7 x V _{CC5} | - | V _{CC5} + 0.3 | V | |
| | V _{IH11} | JTAG_NTRST, JTAG_TCK, JTAG_TDI, JTAG_TMS | TTL input level | 2.7 | - | V _{CC5} + 0.3 | V | |
| "L" level input voltage | V _{IL1} | GPIO of V _{CC5} | CMOS hysteresis input level is selected | V _{SS} - 0.3 | - | 0.3 x V _{CC5} | V | |
| | V _{IL2} | | Automotive input level is selected | V _{SS} - 0.3 | - | 0.5 x V _{CC5} | V | |
| | V _{IL3} | GPIO of V _{CC53_1} | CMOS hysteresis input level is selected | V _{SS} - 0.3 | - | 0.3 x V _{CC53_1} | V | |
| | V _{IL4} | | Automotive input level is selected | V _{SS} - 0.3 | - | 0.5 x V _{CC53_1} | V | |
| | V _{IL5} | GPIO of V _{CC53_2} | CMOS hysteresis input level is selected | V _{SS} - 0.3 | - | 0.3 x V _{CC53_2} | V | |
| | V _{IL6} | | Automotive input level is selected | V _{SS} - 0.3 | - | 0.5 x V _{CC53_2} | V | |
| | V _{IL7} | GPIO of DV _{CC} | CMOS hysteresis input level is selected | V _{SS} - 0.3 | - | 0.3 x DV _{CC} | V | |
| | V _{IL8} | | Automotive input level is selected | V _{SS} - 0.3 | - | 0.5 x DV _{CC} | V | |
| | V _{IL9} | RSTX, NMIX | CMOS hysteresis input level | V _{SS} - 0.3 | - | 0.3 x V _{CC5} | V | |
| | V _{IL10} | MODE | CMOS hysteresis input level | V _{SS} - 0.3 | - | 0.3 x V _{CC5} | V | |
| | V _{IL11} | JTAG_NTRST, JTAG_TCK, JTAG_TDI, JTAG_TMS | TTL input level | V _{SS} - 0.3 | - | 0.8 | V | |

*1: For the details of GPIO group, see section 5.3 Input Level Setting/ Output Drive Capacity Setting.

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name*1 | Conditions | Value | | | Unit | Remarks |
|--------------------|--------------------|--|---|-------|----------------------------|-----|------|---------|
| | | | | Min | Typ | Max | | |
| Hysteresis voltage | V _{HYS1} | GPIO of V _{CC5} | CMOS hysteresis input level is selected | - | 0.05 x V _{CC5} | - | V | |
| | V _{HYS2} | | Automotive input level is selected | - | 0.03 x V _{CC5} | - | V | |
| | V _{HYS3} | GPIO of V _{CC53_1} | CMOS hysteresis input level is selected | - | 0.05 x V _{CC53_1} | - | V | |
| | V _{HYS4} | | Automotive input level is selected | - | 0.03 x V _{CC53_1} | - | V | |
| | V _{HYS5} | GPIO of V _{CC53_2} | CMOS hysteresis input level is selected | - | 0.05 x V _{CC53_2} | - | V | |
| | V _{HYS6} | | Automotive input level is selected | - | 0.03 x V _{CC53_2} | - | V | |
| | V _{HYS7} | GPIO of DV _{CC} | CMOS hysteresis input level is selected | - | 0.05 x DV _{CC} | - | V | |
| | V _{HYS8} | | Automotive input level is selected | - | 0.03 x DV _{CC} | - | V | |
| | V _{HYS9} | RSTX, NMIX | CMOS hysteresis input level | - | 0.05 x V _{CC5} | - | V | |
| | V _{HYS10} | MODE | CMOS hysteresis input level | - | 0.05 x V _{CC5} | - | V | |
| | V _{HYS11} | JTAG_NTRST, JTAG_TCK, JTAG_TDI, JTAG_TMS | TTL input level | - | 0.035 | - | V | |

*1: For the details of GPIO group, see section 5.3 Input Level Setting/ Output Drive Capacity Setting.

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name*1 | Conditions | Value | | | Unit | Remarks |
|--------------------------|---|---|--|---------------------------|---------------------|---------------------|------|---------|
| | | | | Min | Typ | Max | | |
| "H" level output voltage | V _{OH1} | GPIO of V _{CC5} (except P202) | V _{CC5} = 4.5 V, I _{OH} = -1.0 mA | V _{CC5} - 0.5 | - | V _{CC5} | V | |
| | | | V _{CC5} = 3.0 V, I _{OH} = -0.5 mA | V _{CC5} - 0.5 | - | V _{CC5} | V | |
| | V _{OH2} | | V _{CC5} = 4.5 V, I _{OH} = -2.0 mA | V _{CC5} - 0.5 | - | V _{CC5} | V | |
| | | | V _{CC5} = 3.0 V, I _{OH} = -1.0 mA | V _{CC5} - 0.5 | - | V _{CC5} | V | |
| | V _{OH3} | | V _{CC5} = 4.5 V, I _{OH} = -5.0 mA | V _{CC5} - 0.5 | - | V _{CC5} | V | |
| | | | V _{CC5} = 3.0 V, I _{OH} = -2.0 mA | V _{CC5} - 0.5 | - | V _{CC5} | V | |
| | V _{OH4} | GPIO of V _{CC53_1} | V _{CC53_1} = 4.5 V, I _{OH} = -1.0 mA | V _{CC53_1} - 0.5 | - | V _{CC53_1} | V | |
| | | | V _{CC53_1} = 3.0 V, I _{OH} = -0.5 mA | V _{CC53_1} - 0.5 | - | V _{CC53_1} | V | |
| | V _{OH5} | | V _{CC53_1} = 4.5 V, I _{OH} = -2.0 mA | V _{CC53_1} - 0.5 | - | V _{CC53_1} | V | |
| | | | V _{CC53_1} = 3.0 V, I _{OH} = -1.0 mA | V _{CC53_1} - 0.5 | - | V _{CC53_1} | V | |
| | V _{OH6} | | V _{CC53_1} = 4.5 V, I _{OH} = -5.0 mA | V _{CC53_1} - 0.5 | - | V _{CC53_1} | V | |
| | | | V _{CC53_1} = 3.0 V, I _{OH} = -2.0 mA | V _{CC53_1} - 0.5 | - | V _{CC53_1} | V | |
| | V _{OH7} | GPIO of V _{CC53_2} | V _{CC53_2} = 4.5 V, I _{OH} = -1.0 mA | V _{CC53_2} - 0.5 | - | V _{CC53_2} | V | |
| | V _{OH8} | | V _{CC53_2} = 4.5 V, I _{OH} = -2.0 mA | V _{CC53_2} - 0.5 | - | V _{CC53_2} | V | |
| | V _{OH9} | | V _{CC53_2} = 3.0 V, I _{OH} = -5 mA | V _{CC53_2} - 0.5 | - | V _{CC53_2} | V | |
| V _{OH10} | V _{CC53_2} = 3.0 V, I _{OH} = -15 mA | | V _{CC53_2} - 0.5 | - | V _{CC53_2} | V | | |
| V _{OH11} | GPIO of DV _{CC} | DV _{CC} = 4.5 V, I _{OH} = -1.0 mA | DV _{CC} - 0.5 | - | DV _{CC} | V | | |
| | | DV _{CC} = 3.0 V, I _{OH} = -0.5 mA | DV _{CC} - 0.5 | - | DV _{CC} | V | | |
| V _{OH12} | | DV _{CC} = 4.5 V, I _{OH} = -2.0 mA | DV _{CC} - 0.5 | - | DV _{CC} | V | | |
| | | DV _{CC} = 3.0 V, I _{OH} = -1.0 mA | DV _{CC} - 0.5 | - | DV _{CC} | V | | |
| V _{OH13} | | DV _{CC} = 4.5 V, I _{OH} = -5.0 mA | DV _{CC} - 0.5 | - | DV _{CC} | V | | |
| | | DV _{CC} = 3.0 V, I _{OH} = -2.0 mA | DV _{CC} - 0.5 | - | DV _{CC} | V | | |
| V _{OH14} | DV _{CC} = 4.5 V, I _{OH} = -30 mA | DV _{CC} - 0.5 | - | DV _{CC} | V | | | |
| V _{OH15} | JTAG_TDO | V _{CC5} = 4.5 V, I _{OH} = -5.0 mA | V _{CC5} - 0.5 | - | V _{CC5} | V | | |
| | | V _{CC5} = 3.0 V, I _{OH} = -2.0 mA | V _{CC5} - 0.5 | - | V _{CC5} | V | | |

*1: For the details of GPIO group, see section 5.3 Input Level Setting/ Output Drive Capacity Setting.

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name*1 | Conditions | Value | | | Unit | Remarks |
|--------------------------|--|---|---|-------|-----|-----|------|---------|
| | | | | Min | Typ | Max | | |
| "L" level output voltage | V _{OL1} | GPIO of V _{CC5} (except P202) | V _{CC5} = 4.5 V, I _{OL} = 1.0 mA | 0 | - | 0.4 | V | |
| | | | V _{CC5} = 3.0 V, I _{OL} = 0.5 mA | 0 | - | 0.4 | V | |
| | V _{OL2} | | V _{CC5} = 4.5 V, I _{OL} = 2.0 mA | 0 | - | 0.4 | V | |
| | | | V _{CC5} = 3.0 V, I _{OL} = 1.0 mA | 0 | - | 0.4 | V | |
| | V _{OL3} | | V _{CC5} = 4.5 V, I _{OL} = 5.0 mA | 0 | - | 0.4 | V | |
| | | | V _{CC5} = 3.0 V, I _{OL} = 2.0 mA | 0 | - | 0.4 | V | |
| | V _{OL4} | GPIO of V _{CC53_1} | V _{CC53_1} = 4.5 V, I _{OL} = 1.0 mA | 0 | - | 0.4 | V | |
| | | | V _{CC53_1} = 3.0 V, I _{OL} = 0.5 mA | 0 | - | 0.4 | V | |
| | V _{OL5} | | V _{CC53_1} = 4.5 V, I _{OL} = 2.0 mA | 0 | - | 0.4 | V | |
| | | | V _{CC53_1} = 3.0 V, I _{OL} = 1.0 mA | 0 | - | 0.4 | V | |
| | V _{OL6} | | V _{CC53_1} = 4.5 V, I _{OL} = 5.0 mA | 0 | - | 0.4 | V | |
| | | | V _{CC53_1} = 3.0 V, I _{OL} = 2.0 mA | 0 | - | 0.4 | V | |
| | V _{OL7} | GPIO of V _{CC53_2} | V _{CC53_2} = 4.5 V, I _{OL} = 1.0 mA | 0 | - | 0.4 | V | |
| | V _{OL8} | | V _{CC53_2} = 4.5 V, I _{OL} = 2.0 mA | 0 | - | 0.4 | V | |
| | V _{OL9} | | V _{CC53_2} = 3.0 V, I _{OL} = 5.0 mA | 0 | - | 0.4 | V | |
| V _{OL10} | V _{CC53_2} = 3.0 V, I _{OL} = 15 mA | | 0 | - | 0.4 | V | | |
| V _{OL11} | GPIO of DV _{CC} | DV _{CC} = 4.5 V, I _{OL} = 1.0 mA | 0 | - | 0.4 | V | | |
| | | DV _{CC} = 3.0 V, I _{OL} = 0.5 mA | 0 | - | 0.4 | V | | |
| V _{OL12} | | DV _{CC} = 4.5 V, I _{OL} = 2.0 mA | 0 | - | 0.4 | V | | |
| | | DV _{CC} = 3.0 V, I _{OL} = 1.0 mA | 0 | - | 0.4 | V | | |
| V _{OL13} | | DV _{CC} = 4.5 V, I _{OL} = 5.0 mA | 0 | - | 0.4 | V | | |
| | | DV _{CC} = 3.0 V, I _{OL} = 2.0 mA | 0 | - | 0.4 | V | | |
| V _{OL14} | DV _{CC} = 4.5 V, I _{OL} = 30 mA | 0 | - | 0.55 | V | | | |
| V _{OL15} | JTAG_TDO | V _{CC5} = 4.5 V, I _{OL} = 5.0 mA | 0 | - | 0.4 | V | | |
| | | V _{CC5} = 3.0 V, I _{OL} = 2.0 mA | 0 | - | 0.4 | V | | |
| "L" level output voltage | V _{OL16} | GPIO of V _{CC5} (GPIO shared I ² C) | V _{CC5} = 4.5 V, I _{OL} = 3.0 mA | 0 | - | 0.4 | V | |
| | | | V _{CC5} = 3.0 V, I _{OL} = 3.0 mA | 0 | - | 0.4 | V | |

*1: For details of the GPIO group, see section 5.3 Input Level Setting/ Output Drive Capacity Setting.

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name*1 | Conditions | Value | | | Unit | Remarks |
|--|--------------------|--|--|-------|------|-----|------|---------|
| | | | | Min | Typ | Max | | |
| Input leakage current | I _{IL} | ALL GPIO | V _{CC5} = V _{CC53_1} = V _{CC53_2} = DV _{CC} = AV _{CC5} = 5.5 V, V _{SS} < V _I < V _{CC5} | -5 | - | 5 | μA | |
| | | | V _{CC5} = V _{CC53_1} = V _{CC53_2} = DV _{CC} = AV _{CC5} = 3.6 V, V _{SS} < V _I < V _{CC5} | -5 | - | 5 | μA | |
| Pull-up resistor | R _{UP1} | RSTX, NMIX | V _{CC5} = 4.5 V to 5.5 V | 25 | 50 | 100 | kΩ | |
| | | | V _{CC5} = 3.0 V to 3.6 V | 25 | 50 | 100 | kΩ | |
| | R _{UP2} | ALL GPIO | Pull-up resistor selected V _{CC5} /V _{CC53_1} /V _{CC53_2} / DV _{CC} = 4.5 V to 5.5 V | 25 | 50 | 100 | kΩ | |
| | | | Pull-up resistor selected V _{CC5} /V _{CC53_1} /V _{CC53_2} / DV _{CC} = 3.0 V to 3.6 V | 25 | 50 | 100 | kΩ | |
| | R _{UP3} | JTAG_TDI, JTAG_TMS, JTAG_TCK | V _{CC5} = 4.5 V to 5.5 V | 25 | 50 | 100 | kΩ | |
| | | | V _{CC5} = 3.0 V to 3.6 V | 25 | 50 | 100 | kΩ | |
| Pull-down resistor | R _{down1} | ALL GPIO | Pull-down resistor selected V _{CC5} /V _{CC53_1} /V _{CC53_2} / DV _{CC} = 4.5 V to 5.5 V | 25 | 50 | 100 | kΩ | |
| | | | Pull-down resistor Selected V _{CC5} = 3.0 V to 3.6 V | 25 | 50 | 100 | kΩ | |
| | R _{down2} | JTAG_NTRST | V _{CC5} = 4.5 V to 5.5 V | 25 | 50 | 100 | kΩ | |
| | | | V _{CC5} = 3.0 V to 3.6 V | 25 | 50 | 100 | kΩ | |
| Input capacitance | C _{IN1} | GPIO (except GPIO of DV _{CC}) | - | - | 5 | 15 | pF | |
| | C _{IN2} | GPIO of DV _{CC} | - | - | 15 | 45 | pF | |
| High current output drive capacity Phase-to-phase deviation1 | ΔV _{OH14} | GPIO of DV _{CC} | DV _{CC} = 4.5 V I _{OH} = -30 mA Maximum deviation of V _{OH14} | - | - | 90 | mV | *2 |
| High current output drive capacity Phase-to-phase deviation2 | ΔV _{OL14} | GPIO of DV _{CC} | DV _{CC} = 4.5 V I _{OL} = 30 mA Maximum deviation of V _{OL14} | - | - | 90 | mV | *2 |
| LCD divider resistor | R _{LCD} | V0 to V1, V1 to V2, V2 to V3 | - | 6.25 | 12.5 | 25 | kΩ | |
| COM0 to COM3 output impedance | R _{VCOM} | COM _m (m = 0 to 3) | - | - | - | 4.5 | kΩ | |
| SEG0 to SEG31 output impedance | R _{VSEG} | SEG _n (n = 0 to 31) | - | - | - | 17 | kΩ | |
| LCD leak current | I _{LCDC} | V0 to V3, COM _m (m = 0 to 3) SEG _n (n = 0 to 31) | T _A = +25 °C | -0.5 | - | 0.5 | μA | |

*1: For the details of GPIO group, see section 5.3 Input Level Setting/ Output Drive Capacity Setting.

*2: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of V_{OH14}/V_{OL14} for each pin is defined. Same for other channels.

7.3.2 Power Supply Current

(1) Power Supply Current for S6J3360 Series

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks | |
|----------------------|-------------------|-------------------------------------|--------------------------------------|-------|-----|-----|------------------------|---|--|
| | | | | Min | Typ | Max | | | |
| Power supply current | I _{CC5} | V _{CC5} | Normal operation | - | 70 | 164 | mA | Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz | |
| | | | Work Flash write/erase | - | 81 | 174 | mA | | |
| | | | TC Flash write/erase | - | 75 | 170 | mA | | |
| | | | Normal operation | - | 68 | 162 | mA | | Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz |
| | | | Work Flash write/erase | - | 79 | 172 | mA | | |
| | | | TC Flash write/erase | - | 72 | 166 | mA | | |
| | I _{CCP} | | PWU mode (Shutdown) | - | 56 | 130 | μA | T _A = 25 °C (PWU operation cycle 16 ms) | |
| | | | | - | 50 | 120 | μA | T _A = 25 °C (PWU operation cycle 32 ms) | |
| | I _{CC52} | | Timer mode (Shutdown ^{*1}) | - | 330 | 390 | μA | T _A = 25 °C, When using 4 MHz crystal for main oscillator. C _L = 10 pF, MCGAIN = 0b00 (4 MHz) | |
| | | | | - | 410 | 470 | μA | T _A = 25 °C, When using 8 MHz crystal for main oscillator. C _L = 10 pF, MCGAIN = 0b01 (8 MHz) | |
| | | | | - | 55 | 100 | μA | T _A = 25 °C, When using Slow-CR oscillation. | |
| | | | | - | 60 | 120 | μA | T _A = 25 °C, When using 32 kHz sub oscillation. | |
| | I _{CC52} | Stop mode (Shutdown ^{*1}) | - | 55 | 95 | μA | T _A = 25 °C | | |

*1: BackupRAM 24 KB retention.

(2) Power Supply Current for S6J3370 Series

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks | |
|----------------------|-------------------|------------------------|-------------------------|-------|-----|-----|------------------------|---|--|
| | | | | Min | Typ | Max | | | |
| Power supply current | I _{CC5} | V _{CC5} | Normal operation | - | 56 | 148 | mA | Operating at 132 MHz, HPM 33 MHz, Peripheral 33 MHz | |
| | | | Work Flash write/erase | - | 67 | 158 | mA | | |
| | | | TC Flash write/erase | - | 62 | 153 | mA | | |
| | | | Normal operation | - | 54 | 146 | mA | | Operating at 80 MHz, HPM 40 MHz, Peripheral 40 MHz |
| | | | Work Flash write/erase | - | 65 | 156 | mA | | |
| | | | TC Flash write/erase | - | 59 | 150 | mA | | |
| | I _{CCP} | | PWU mode (Shutdown) | - | 56 | 130 | μA | T _A = 25 °C (PWU operation cycle 16 ms) | |
| | | | | - | 50 | 120 | μA | T _A = 25 °C (PWU operation cycle 32 ms) | |
| | I _{CC52} | | Timer mode (Shutdown*1) | - | 330 | 390 | μA | T _A = 25 °C, When using 4 MHz crystal for main oscillator. C _L = 10 pF, MCGAIN = 0b00 (4 MHz) | |
| | | | | - | 410 | 470 | μA | T _A = 25 °C, When using 8 MHz crystal for main oscillator. C _L = 10 pF, MCGAIN = 0b01 (8 MHz) | |
| | | | | - | 55 | 100 | μA | T _A = 25 °C, When using Slow-CR oscillation. | |
| | | | | - | 60 | 120 | μA | T _A = 25 °C, When using 32 kHz sub oscillation. | |
| | I _{CC52} | Stop mode (Shutdown*1) | - | 55 | 95 | μA | T _A = 25 °C | | |

*1: BackupRAM 24 KB retention.

7.4 AC Characteristics

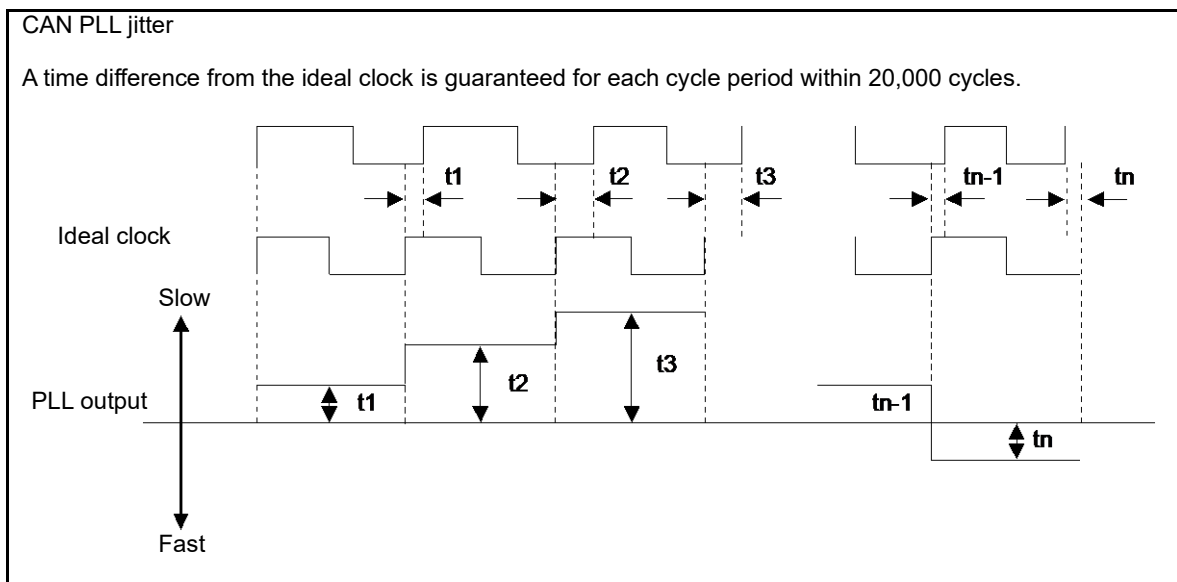
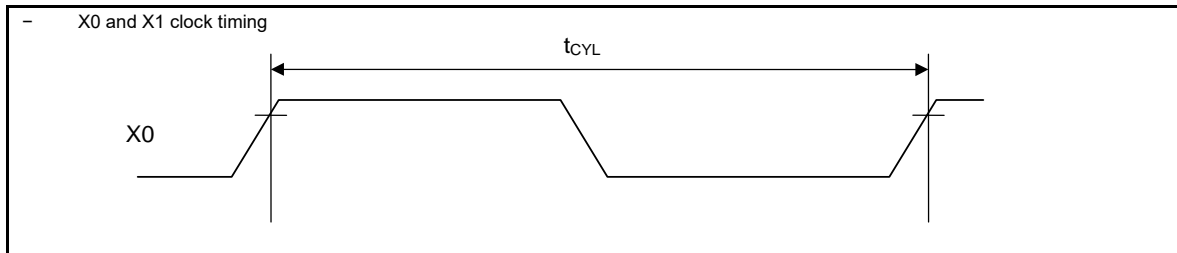
7.4.1 Source Clock Timing

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|--|-----------|----------|------------|-------|-----|-------|------|-------------|
| | | | | Min | Typ | Max | | |
| Source oscillation clock frequency | F_C | X0, X1 | - | 3.6 | 4 | 16 | MHz | |
| Source oscillation clock cycle time | t_{CYL} | X0, X1 | - | 62.5 | 250 | 277.8 | ns | |
| CAN PLL jitter (when locked) | t_{PJ} | - | - | -10 | - | 10 | ns | |
| Internal Slow CR oscillation frequency | F_{CRS} | - | - | 50 | 100 | 150 | kHz | |
| Internal Fast CR oscillation frequency | F_{CRF} | - | - | 2.4 | 4 | 5.61 | MHz | Before trim |
| | | | | 3.2 | 4 | 4.81 | MHz | After trim |

Notes:

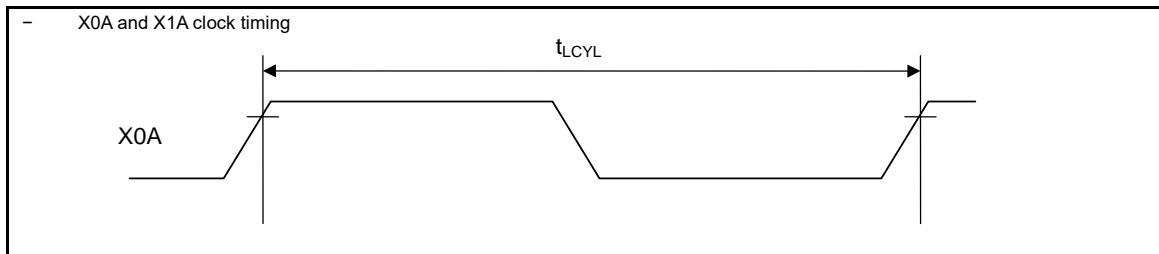
- The maximum/minimum values have been standardized with the main clock and PLL clock in use.
- Jitter of source oscillator must be smaller than 3000 ppm.
- Enough evaluation and adjustment are recommended using oscillator on your system board.



7.4.2 Sub Clock Timing

(Condition: See 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|-------------------------------------|-------------------|----------|------------|-------|--------|-----|------|---------|
| | | | | Min | Typ | Max | | |
| Source oscillation clock frequency | F _{CL} | X0A, X1A | - | - | 32.768 | - | kHz | |
| Source oscillation clock cycle time | t _{LCYL} | X0A, X1A | - | - | 30.52 | - | μs | |



7.4.3 Internal Clock Timing

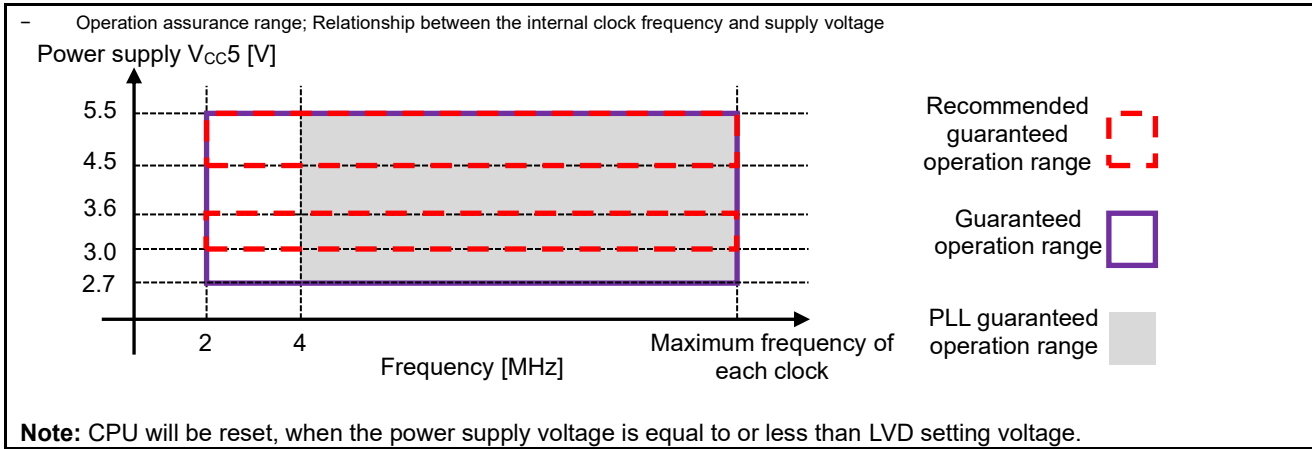
- This section shows the target characteristics for internal clock timing at the current stage.
- Corresponding functions for these clocks are described in Chapter 5: Clock Configuration of the S6J3360/S6J3370 series hardware manual.

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | | Unit | Remarks |
|--------------------------|----------------|----------|------------|-------|-----|-------|-------|------|--|
| | | | | Min | Typ | Max*1 | Max*2 | | |
| Internal clock frequency | FSSCG0out | - | - | 200 | - | 320 | 320 | MHz | |
| | FPLL0out | - | - | 200 | - | 320 | 320 | MHz | |
| | FExpandPLL0out | - | - | 200 | - | 280 | 280 | MHz | |
| | FExpandPLL1out | - | - | 200 | - | 480 | 480 | MHz | |
| | FExpandPLL2out | - | - | 200 | - | 400 | 400 | MHz | |
| | FCLK_CPU | - | - | - | - | 132 | 80 | MHz | |
| | FCLK_SHE | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_FCLK | - | - | - | - | 66 | 80 | MHz | |
| | FCLK_ATB | - | - | - | - | 66 | 40 | MHz | |
| | FCLK_DBG | - | - | - | - | 66 | 40 | MHz | |
| | FCLK_HPM | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_DMA | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_MEMC | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_SYSC1 | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_LLPBM | - | - | - | - | 132 | 80 | MHz | |
| | FCLK_LCP | - | - | - | - | 66 | 80 | MHz | |
| | FCLK_LCP0 | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_LCP0A | - | - | - | - | 40 | 40 | MHz | |
| | FCLK_LCP1 | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_LCP1A | - | - | - | - | 40 | 40 | MHz | |
| | FCLK_TRC | - | - | - | - | 66 | 40 | MHz | |
| | FCLK_SYSC0H | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_COMH | - | - | - | - | 33 | 40 | MHz | |
| | FCLK_CAN | - | - | - | - | 48 | 48 | MHz | |
| | FCLK_JTAG | - | - | - | - | 20 | 20 | MHz | Input clock frequency for JTAG_TCK |
| | FCLK_CLKO | - | - | - | - | 10 | 10 | MHz | Output clock frequency for SYSC0_CLK_0/1 |
| FExpand_CLK_CD0 | - | - | - | - | 140 | 140 | MHz | | |
| FExpand_CLK_CD1 | - | - | - | - | 120 | 120 | MHz | | |
| FExpand_CLK_CD1A | - | - | - | - | 120 | 120 | MHz | | |
| FExpand_CLK_CD1B | - | - | - | - | 60 | 60 | MHz | | |
| FExpand_CLK_CD2 | - | - | - | - | 200 | 200 | MHz | | |

*1: Target maximum clock frequencies when CPU clock is 132 MHz

*2: Target maximum clock frequencies when CPU clock is 80 MHz



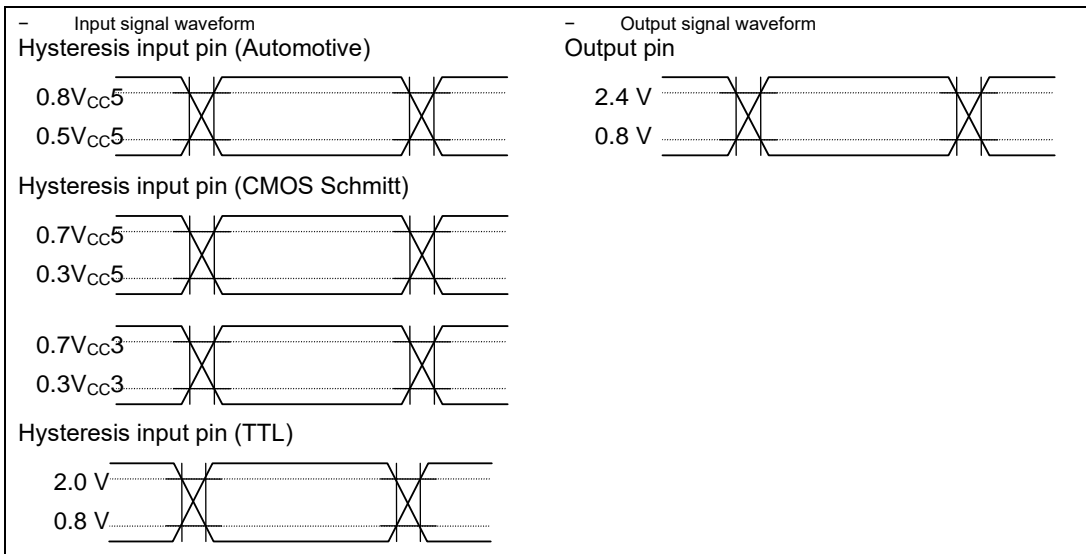
- Relationship between the oscillation clock frequency and internal clock frequency

| Oscillation clock frequency [MHz] | Internal Operation Clock Frequency | | | | | | | | | |
|-----------------------------------|------------------------------------|-----------------|-----------------|-----------------|-----------------|-----|----|-----|------------------|------------------|
| | Main Clock | PLL Clock | | | | | | | Multiplied by 20 | Multiplied by 33 |
| | | Multiplied by 1 | Multiplied by 2 | Multiplied by 3 | Multiplied by 4 | ... | | | | |
| 4 | 2 | 4 | 8 | 12 | 16 | ... | 80 | 132 | | |

- Oscillation circuit example

Note:
For the configuration of an oscillation circuit, request the oscillator manufacturer to perform a circuit matching evaluation before starting design.

AC characteristics are specified by the following measurement reference voltage values.

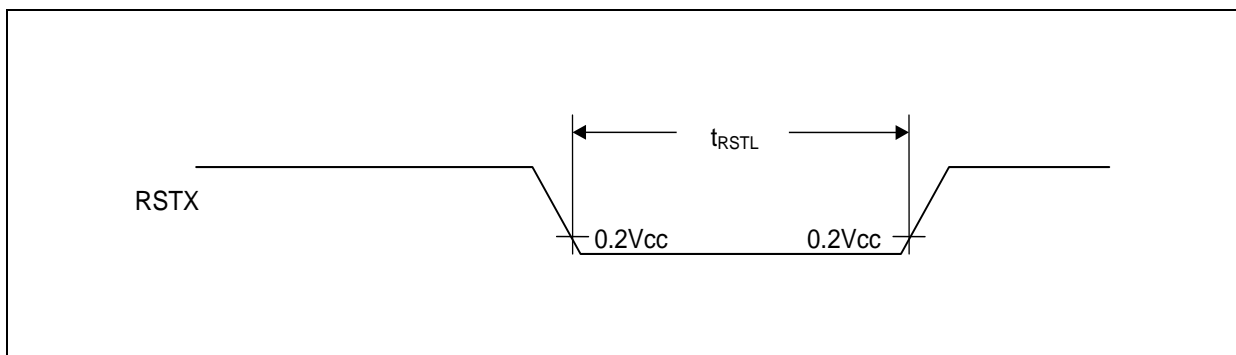


7.4.4 Reset Input

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|----------------------------|-------------------|----------|------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| Reset input time | t _{RSTL} | RSTX | - | 10 | - | μs | |
| Reset input pulse filtered | | | | - | 1 | μs | *1 |

*1: Reset input pulse is filtered up to 1 μs. Filtering of input pulse more than 1 μs is not guaranteed.



7.4.5 Power-on Conditions

7.4.5.1 Power-on Conditions

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|---|------------------|------------------|---|-------|-----|-----|-------|---------|
| | | | | Min | Typ | Max | | |
| Level detection voltage | - | V _{CC5} | - | 2.2 | 2.4 | 2.6 | V | |
| Level detection hysteresis width | - | V _{CC5} | - | - | 100 | - | mV | |
| Level detection time | - | - | - | - | - | 40 | μs | *1 |
| Power off time | t _{OFF} | V _{CC5} | - | 100 | - | - | μs | *2 |
| Power ramp rate | dV/dt | V _{CC5} | V _{CC5} : 1.5 V to 2.6 V | - | - | 1 | V/μs | *3 |
| Maximum ramp rate guaranteed to not generate power-on reset | dV/dt | V _{CC5} | V _{CC5} : Between 2.7 V and 4.5 V | - | - | 50 | mV/μs | *4 |

*1: This specification is at 1 V/μs of power ramp rate.

*2: V_{CC5} must be held below 1.5 V for a minimum period of t_{OFF}.

*3: Power ramp rate must be 1 V/μs or less from 1.5 V to 2.6 V.

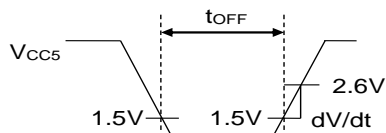
Power-on can detect by satisfying power ramp rate and power off time.

*4: The power ramp rate specification indicates power supply fluctuation after power-on detection. When V_{CC5} voltage is between 2.7 V and 4.5 V, the power supply fluctuation is below 50 mV/μs, the detection of power-on is suppressed. The power-on does not detect any power fluctuation between 4.5 V and 5.5 V.

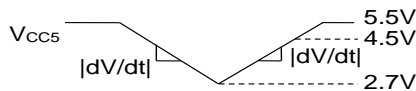
Notes:

When using the S6J3360/S6J3370 series, *2 and *3 must be satisfied. When neither *2 nor *3 can be satisfied, assert external reset (RSTX) at power-up and any brownout event.

• Power off time, Power ramp rate



• Maximum ramp rate guaranteed to not generate power-on reset



7.4.5.2 Power Supply Sequence

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|---|--------------------------|---------------------|-------|-----|-----|------|---|
| | | | Min | Typ | Max | | |
| AV _{CC5} power on delay from V _{CC5} | t _{d_avcc5} | AV _{CC5} | 0 | - | - | ms | AV _{CC5} power on should be simultaneous or after V _{CC5} power on. |
| DV _{CC} power on delay from V _{CC5} | t _{d_dvcc} | DV _{CC} | 0 | - | - | ms | DV _{CC} power on should be simultaneous or after V _{CC5} power on. ^{*1} |
| | | | - | - | - | ms | No requirement for power supply sequence. ^{*2} |
| V _{CC53_1} power on delay from V _{CC5} | t _{d_vcc531} | V _{CC53_1} | 0 | - | - | ms | V _{CC53_1} power on should be simultaneous or after V _{CC5} power on. |
| V _{CC53_2} power on delay from V _{CC5} | t _{d_vcc532} | V _{CC53_2} | 0 | - | - | ms | V _{CC53_2} power on should be simultaneous or after V _{CC5} power on. |
| V _{CC5} power off delay from AV _{CC5} | t _{doff_avcc5} | AV _{CC5} | 0 | - | - | ms | AV _{CC5} power off should be simultaneous or before V _{CC5} power off. |
| V _{CC5} power off delay from DV _{CC} | t _{doff_dvcc} | DV _{CC} | 0 | - | - | ms | DV _{CC} power off should be simultaneous or before V _{CC5} power off. ^{*1} |
| | | | - | - | - | ms | No requirement for power supply sequence. ^{*2} |
| V _{CC5} power off delay from V _{CC53_1} | t _{doff_vcc531} | V _{CC53_1} | 0 | - | - | ms | V _{CC53_1} power off should be simultaneous or before V _{CC5} power off. |
| V _{CC5} power off delay from V _{CC53_2} | t _{doff_vcc532} | V _{CC53_2} | 0 | - | - | ms | V _{CC53_2} power off should be simultaneous or before V _{CC5} power off. |

*1: For S6J33xxxS or S6J33xxxT or S6J33xxxU or S6J33xxxV part number

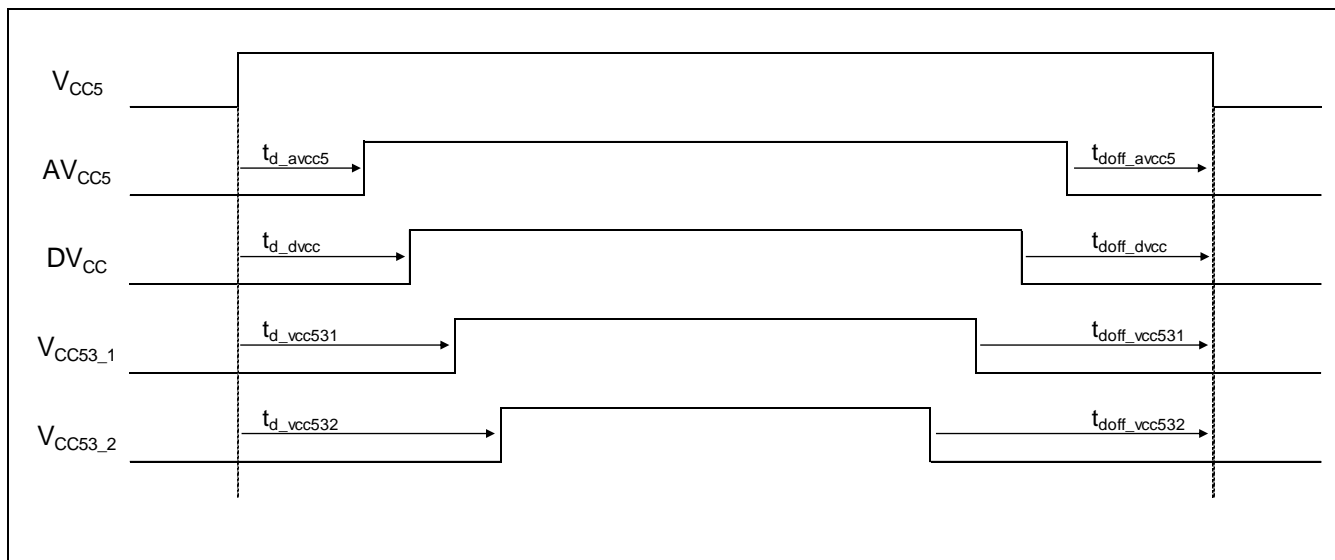
*2: For S6J33xxxA or S6J33xxxE or S6J33xxxC or S6J33xxxG part number

Notes:

Satisfy absolute maximum rating of power supply voltage on 7.1 Absolute Maximum Ratings.

This product series has five different power supply ports. The power supply sequence of them is specified with the power on delay time from V_{CC5}.

The power off sequence is reverse of the power on sequence.



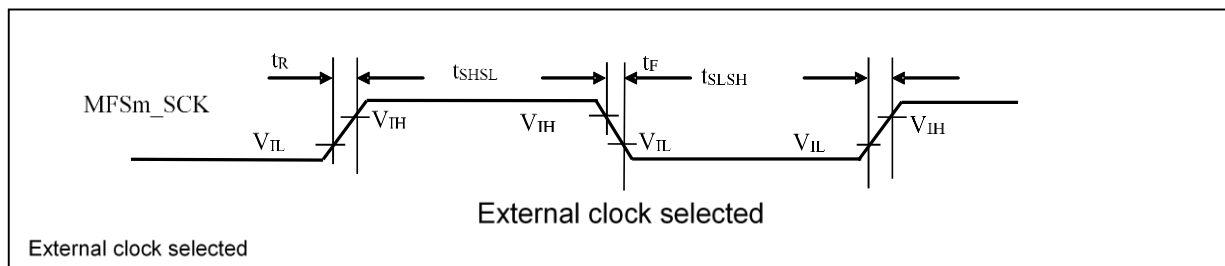
7.4.6 Multi-Function Serial
7.4.6.1 UART (Asynchronous Serial Interface) Timing (SMR:MD2-0 = 0b000, 0b001)
External Clock Selected (BGR:EXT = 1)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|------------|---|---|----------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | t_{SLSH} | MFSm_SCK_x ^{*2} (m = 0 to 11) | (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | $t_{CLK_LCPnA}^{*1} + 10$ | - | ns | |
| Serial clock "H" pulse width | t_{SHSL} | MFSm_SCK_x ^{*2} (m = 0 to 11) | | $t_{CLK_LCPnA}^{*1} + 10$ | - | ns | |
| SCK falling time | t_F | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |
| SCK rising time | t_R | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |

*1: n = 0: ch.0 to ch.7, n = 1: ch.8 to ch.11.

*2: For the details of x value, see section 5 Pin Descriptions.



7.4.6.2 CSIO Timing (SMR:MD2-0 = 0b010)

(1) Normal Synchronous Transfer (SCR:SPI = 0) and Mark Level "H" of Serial Clock Output (SMR:SCINV = 0)

(Condition: See section 7.2 Recommended Operating Conditions)

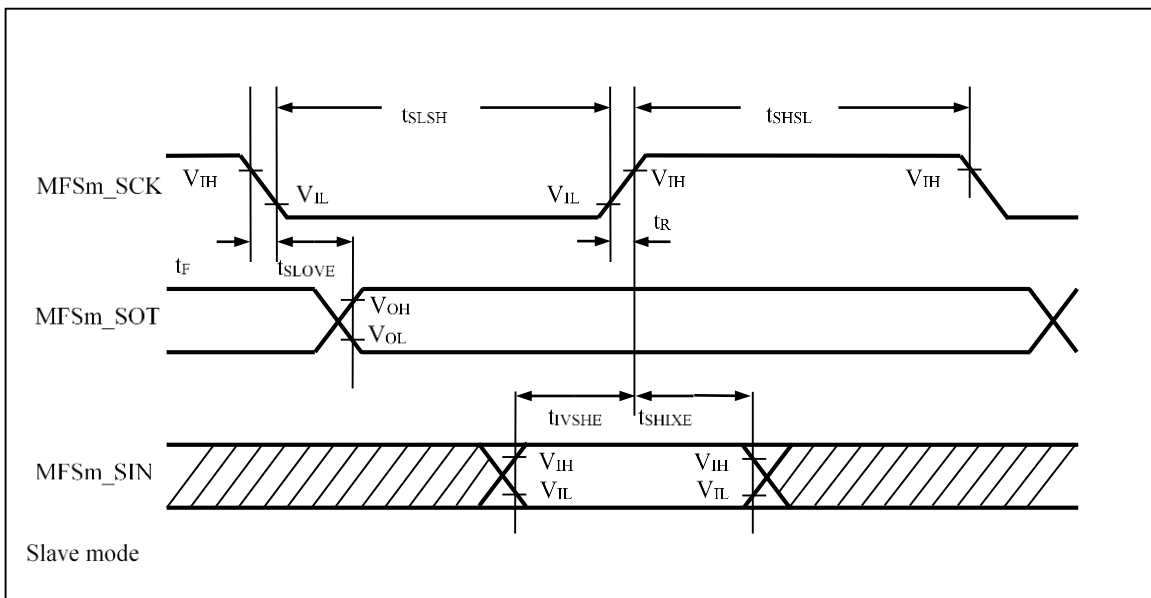
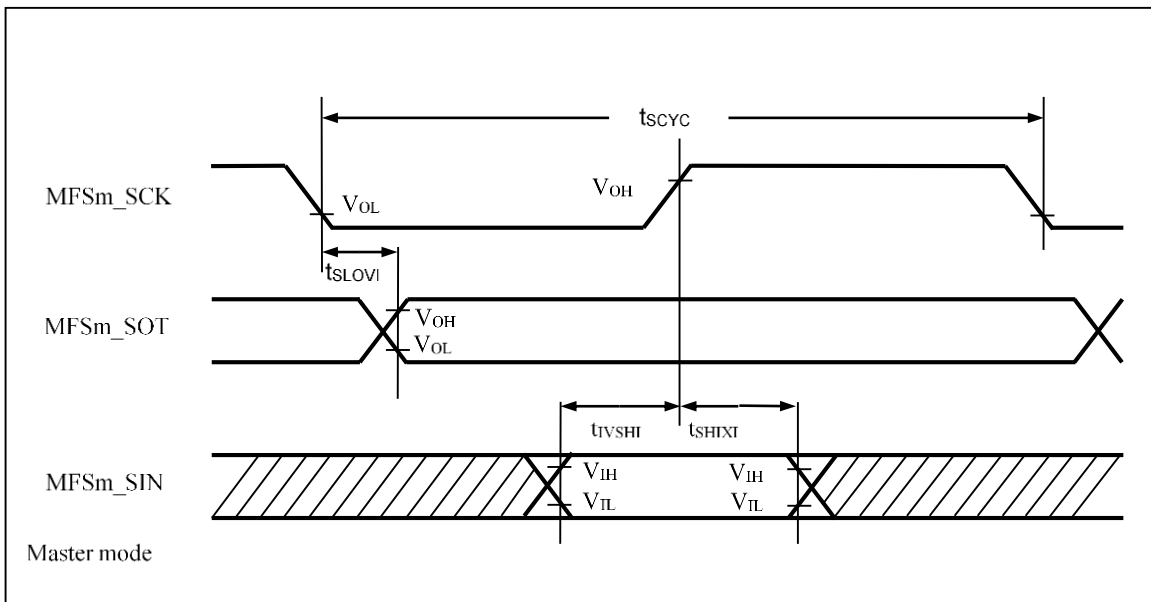
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|--------------------|---|--|---------------------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t _{SCYC} | MFSm_SCK_x ^{*2} (m = 0 to 11) | Master mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 4t _{CLK_LCPnA} ^{*1} | - | ns | |
| SCK ↓ → SOT delay time | t _{SLOVI} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | | -30 | 30 | ns | |
| Valid SIN → SCK ↑ setup time | t _{IVSHI} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 31 | - | ns | |
| SCK ↑ → Valid SIN hold time | t _{SHIXI} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 0 | - | ns | |
| Serial clock "H" pulse width | t _{SHSL} | MFSm_SCK_x ^{*2} (m = 0 to 11) | Slave mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 2t _{CLK_LCPnA} ^{*1} | - | ns | |
| Serial clock "L" pulse width | t _{SLSH} | MFSm_SCK_x ^{*2} (m = 0 to 11) | | 2t _{CLK_LCPnA} ^{*1} | - | ns | |
| SCK ↓ → SOT delay time | t _{SLOVE} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | | - | 30 | ns | |
| Valid SIN → SCK ↑ setup time | t _{IVSHE} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 10 | - | ns | |
| SCK ↑ → Valid SIN hold time | t _{SHIXE} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 20 | - | ns | |
| SCK falling time | t _F | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |
| SCK rising time | t _R | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |

*1: n = 0: ch.0 to ch.7, n = 1: ch.8 to ch.11.

*2: For the details of x value, see section 5 Pin Descriptions.

Notes:

- This table provides the alternate current standard for CLK synchronous mode.
- C_L is the load capability value connected to the pin during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(2) Normal Synchronous Transfer (SCR:SPI = 0) and Mark Level "L" of Serial Clock Output (SMR:SCINV = 1)

(Condition: See section 7.2 Recommended Operating Conditions)

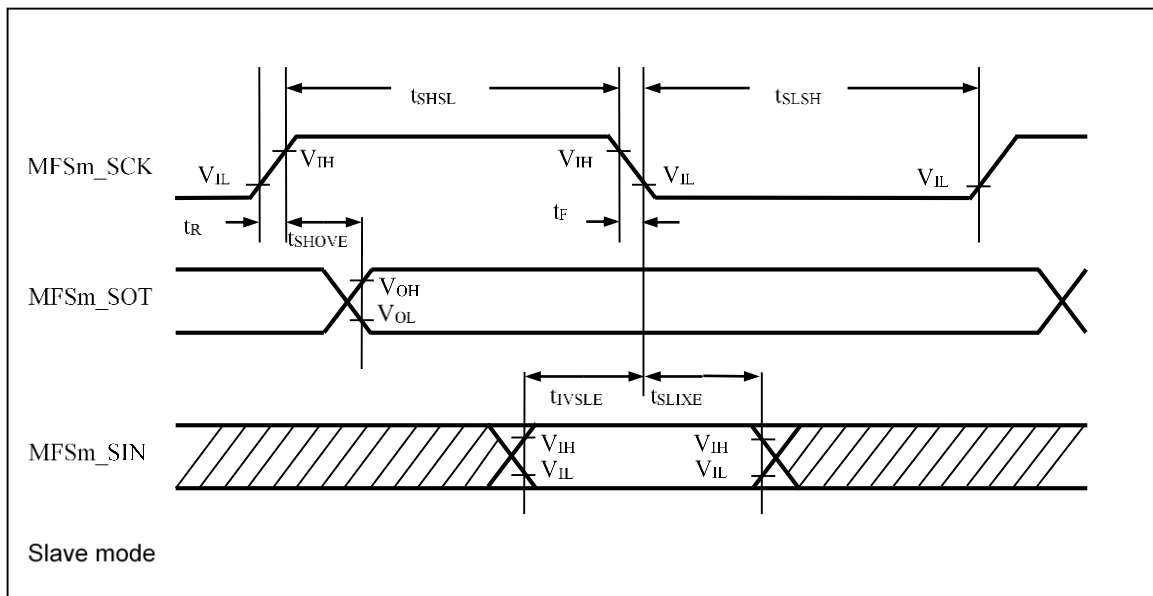
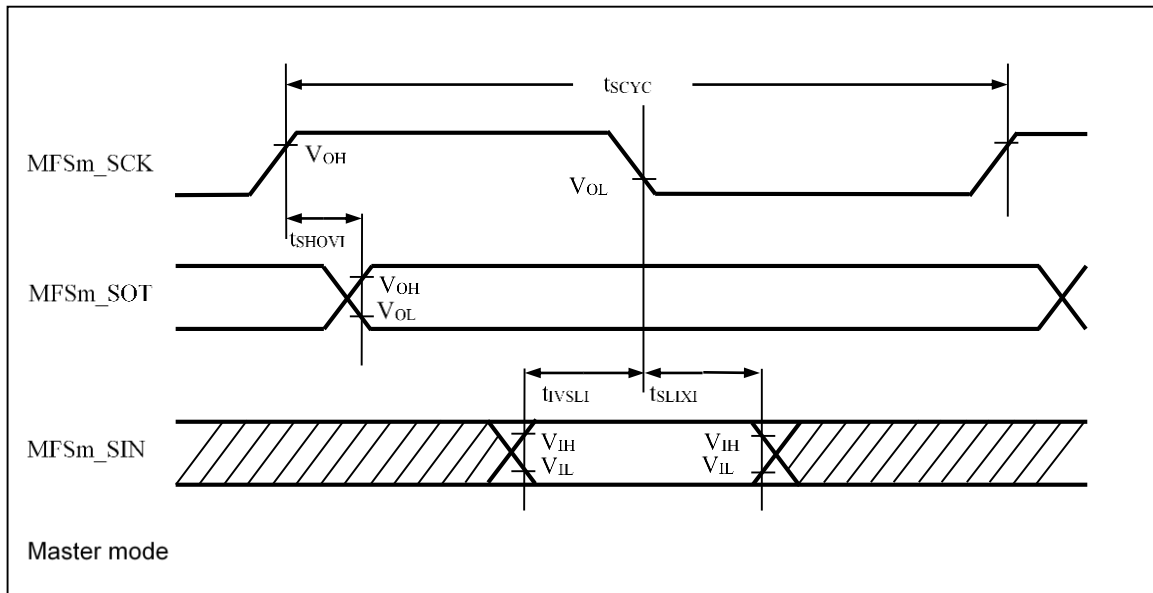
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|--------------------|---|--|---------------------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t _{SCYC} | MFSm_SCK_x ^{*2} (m = 0 to 11) | Master mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 4t _{CLK_LCPnA} ^{*1} | - | ns | |
| SCK ↑ → SOT delay time | t _{SHOVI} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | | -30 | 30 | ns | |
| Valid SIN → SCK ↓ setup time | t _{IVSLI} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 31 | - | ns | |
| SCK ↓ → Valid SIN hold time | t _{SLIXI} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 0 | - | ns | |
| Serial clock "H" pulse width | t _{SHSL} | MFSm_SCK_x ^{*2} (m = 0 to 11) | Slave mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 2t _{CLK_LCPnA} ^{*1} | - | ns | |
| Serial clock "L" pulse width | t _{SLSH} | MFSm_SCK_x ^{*2} (m = 0 to 11) | | 2t _{CLK_LCPnA} ^{*1} | - | ns | |
| SCK ↑ → SOT delay time | t _{SHOVE} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | | - | 30 | ns | |
| Valid SIN → SCK ↓ setup time | t _{IVSLE} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 10 | - | ns | |
| SCK ↓ → Valid SIN hold time | t _{SLIXE} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 20 | - | ns | |
| SCK falling time | t _F | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |
| SCK rising time | t _R | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |

*1: n = 0: ch.0 to ch.7, n = 1: ch.8 to ch.11

*2: For the details of x value, see section 5 Pin Descriptions.

Notes:

- This table provides the alternate current standard for CLK synchronous mode.
- C_L is the load capability value connected to the pin during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(3) SPI Supported (SCR:SPI = 1), and Mark Level "H" of Serial Clock Output (SMR:SCINV = 0)

(Condition: See section 7.2 Recommended Operating Conditions)

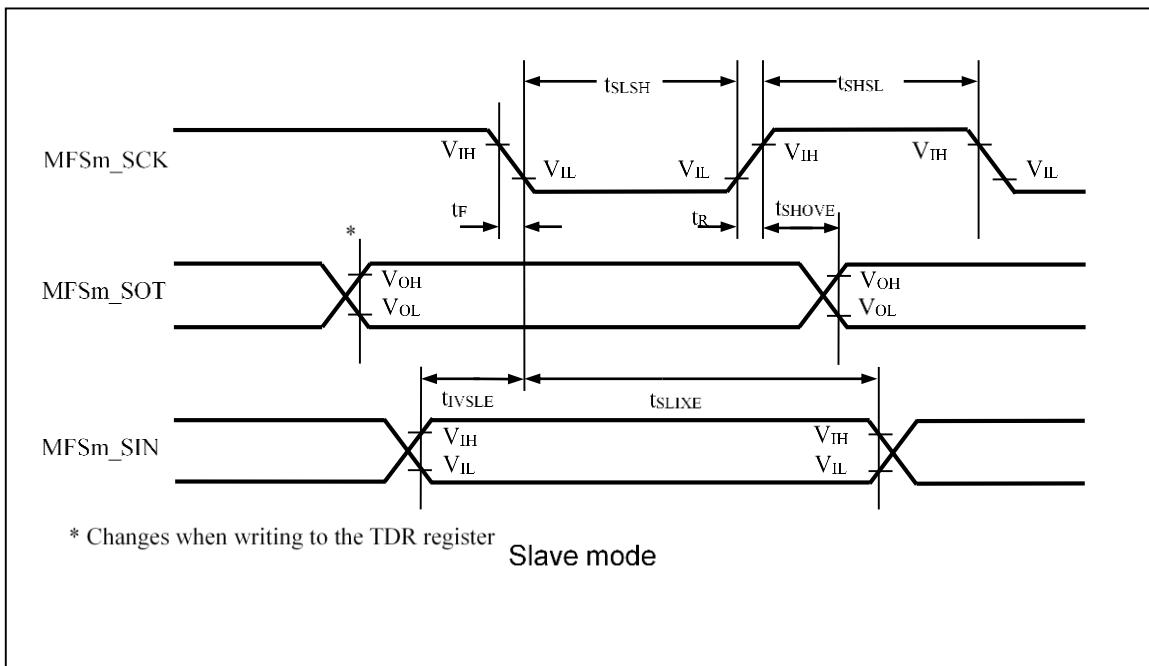
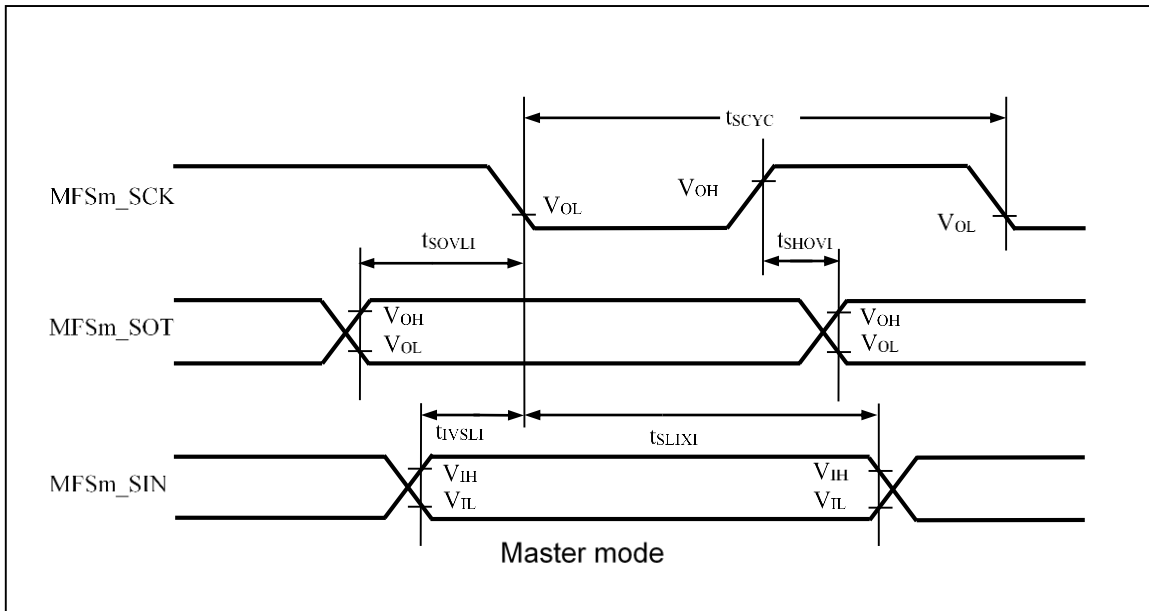
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|--------------------|---|--|---|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t _{SCYC} | MFSm_SCK_x ^{*2} (m = 0 to 11) | Master mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 4t _{CLK_LCPnA} ^{*1} | - | ns | |
| SCK ↑ → SOT delay time | t _{SHOVI} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | | -30 | 30 | ns | |
| Valid SIN → SCK ↓ setup time | t _{IVSLI} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 31 | - | ns | |
| SCK ↓ → Valid SIN hold time | t _{SLIXI} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 0 | - | ns | |
| SOT → SCK ↓ delay time | t _{SOVLI} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | | 2t _{CLK_LCPnA} ^{*1} - 30 | - | ns | |
| Serial clock "H" pulse width | t _{SHSL} | MFSm_SCK_x ^{*2} (m = 0 to 11) | | 2t _{CLK_LCPnA} ^{*1} | - | ns | |
| Serial clock "L" pulse width | t _{SLSH} | MFSm_SCK_x ^{*2} (m = 0 to 11) | 2t _{CLK_LCPnA} ^{*1} | - | ns | | |
| SCK ↑ → SOT delay time | t _{SHOVE} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | Slave mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | - | 30 | ns | |
| Valid SIN → SCK ↓ setup time | t _{IVSLE} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 10 | - | ns | |
| SCK ↓ → Valid SIN hold time | t _{SLIXE} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 20 | - | ns | |
| SCK falling time | t _F | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |
| SCK rising time | t _R | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |

*1: n = 0: ch.0 to ch.7, n = 1: ch.8 to ch.11

*2: For the details of x value, see section 5 Pin Descriptions.

Notes:

- This table provides the alternate current standard for CLK synchronous mode.
- C_L is the load capability value connected to the pin during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(4) SPI Supported (SCR:SPI = 1), and Mark Level "L" of Serial Clock Output (SMR:SCINV = 1)

(Condition: See section 7.2 Recommended Operating Conditions)

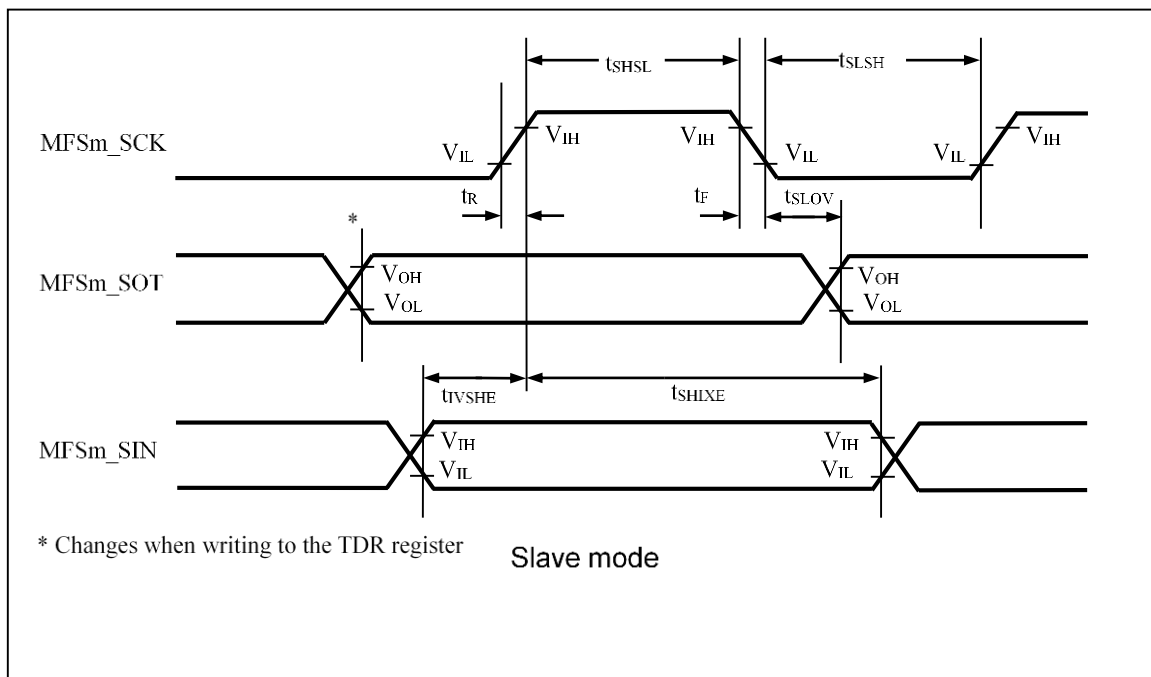
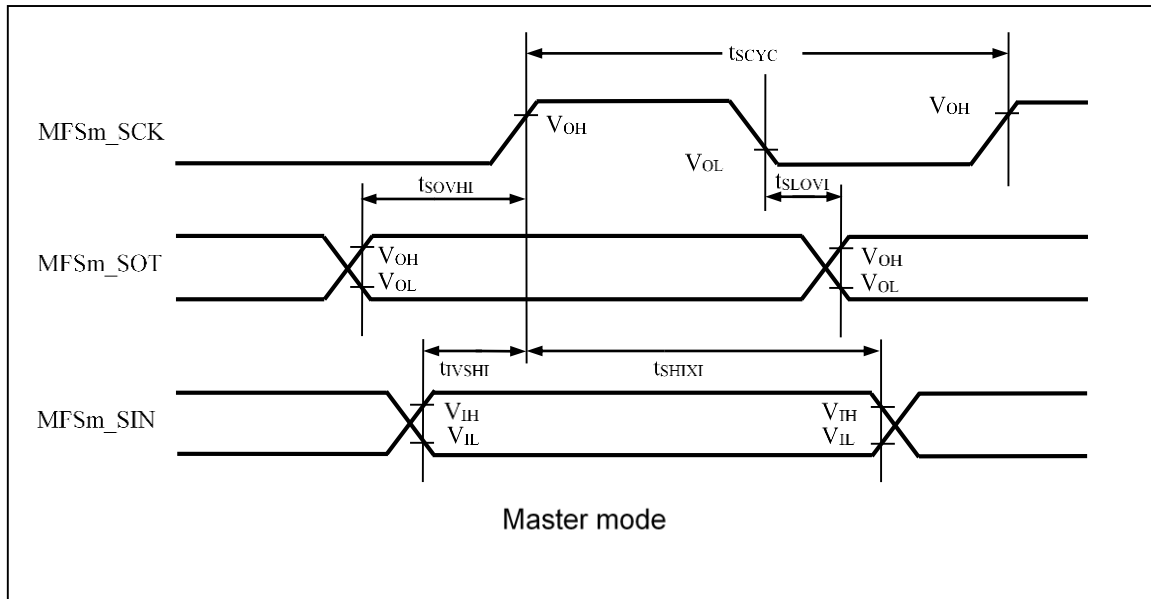
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------------------|--------------------|---|--|--|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t _{SCYC} | MFSm_SCK_x ^{*2} (m = 0 to 11) | Master mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 4t _{CLK_LCPnA} ^{*1} | - | ns | |
| SCK ↓ -> SOT delay time | t _{SLOVI} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | | -30 | 30 | ns | |
| Valid SIN -> SCK ↑ setup time | t _{IVSHI} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 31 | - | ns | |
| SCK ↑ -> Valid SIN hold time | t _{SHIXI} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 0 | - | ns | |
| SOT -> SCK ↑ delay time | t _{SOVHI} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | | 2t _{CLK_LCPnA} ^{*1} - 30 | - | ns | |
| Serial clock "H" pulse width | t _{SHSL} | MFSm_SCK_x ^{*2} (m = 0 to 11) | | 2t _{CLK_LCPnA} ^{*1} | - | ns | |
| Serial clock "L" pulse width | t _{SLSH} | MFSm_SCK_x ^{*2} (m = 0 to 11) | 2t _{CLK_LCPnA} ^{*1} | - | ns | | |
| SCK ↓ -> SOT delay time | t _{SLOVE} | MFSm_SCK_x ^{*2} MFSm_SOT_x ^{*2} (m = 0 to 11) | Slave mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | - | 30 | ns | |
| Valid SIN -> SCK ↑ setup time | t _{IVSHE} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 10 | - | ns | |
| SCK ↑ -> Valid SIN hold time | t _{SHIXE} | MFSm_SCK_x ^{*2} MFSm_SIN_x ^{*2} (m = 0 to 11) | | 20 | - | ns | |
| SCK falling time | t _F | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |
| SCK rising time | t _R | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |

*1: n = 0: ch.0 to ch.7, n = 1: ch.8 to ch.11.

*2: For the details of x value, see section 5 Pin Descriptions.

Notes:

- This table provides the alternate current standard for CLK synchronous mode.
- C_L is the load capability value connected to the pin during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(5) Serial Chip Select Used (SCSCR:CSEN = 1)

- Mark level "H" of serial clock output (SMR, SCSFR:SCINV = 0)
- Inactive level "H" of serial chip select (SCSCR, SCSFR:CSLVL = 1)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------------|-------------------|---|--|---|---|------|---------|
| | | | | Min | Max | | |
| SCS ↓ → SCK ↓ setup time | t _{CSSU} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Master mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | t _{CSSU} ^{*1} - 50 | - | ns | |
| SCK ↑ → SCS ↑ hold time | t _{CSDH} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | t _{CSDH} ^{*2} + 0 | - | ns | |
| SCS deselect time | t _{CSDI} | FSm_CSy_x ^{*5} (m = 0 to 11) | | t _{CSDS} ^{*3} - 50 + 5t _{CLK_LCPnA} ^{*4} | - | ns | |
| SCS ↓ → SCK ↓ setup time | t _{CSSS} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Slave mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 3t _{CLK_LCPnA} ^{*4} + 30 | - | ns | |
| SCK ↑ → SCS ↑ hold time | t _{CSDH} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | 0 | - | ns | |
| SCS deselect time | t _{CSDS} | MFSm_CSy_x ^{*5} (m = 0 to 11) | | 3t _{CLK_LCPnA} ^{*4} + 30 | - | ns | |
| SCS ↓ → SOT delay time | t _{DSE} | MFSm_CSy_x ^{*5} MFSm_SOT_x ^{*5} (m = 0 to 11) | | - | 40 | ns | |
| SCS ↑ → SOT delay time | t _{DEE} | MFSm_CSy_x ^{*5} MFSm_SOT_x ^{*5} (m = 0 to 11) | | 0 | - | ns | |
| SCK ↓ → SCS ↓ clock switching time | t _{SCC} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Master mode round operation (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 3t _{CLK_LCPnA} ^{*4} + 0 | 3t _{CLK_LCPnA} ^{*4} + 50 | ns | |

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSDH} = SCSTR:CSDH[7:0] x serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

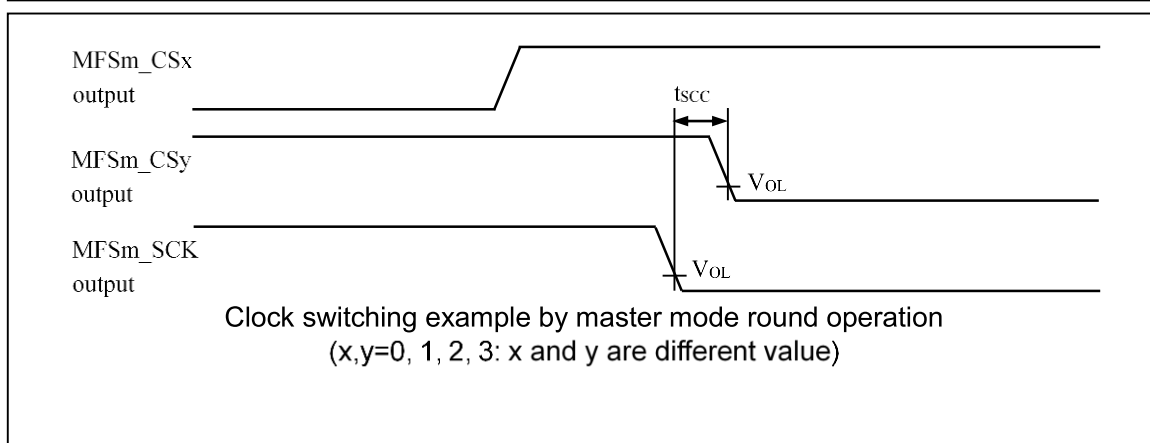
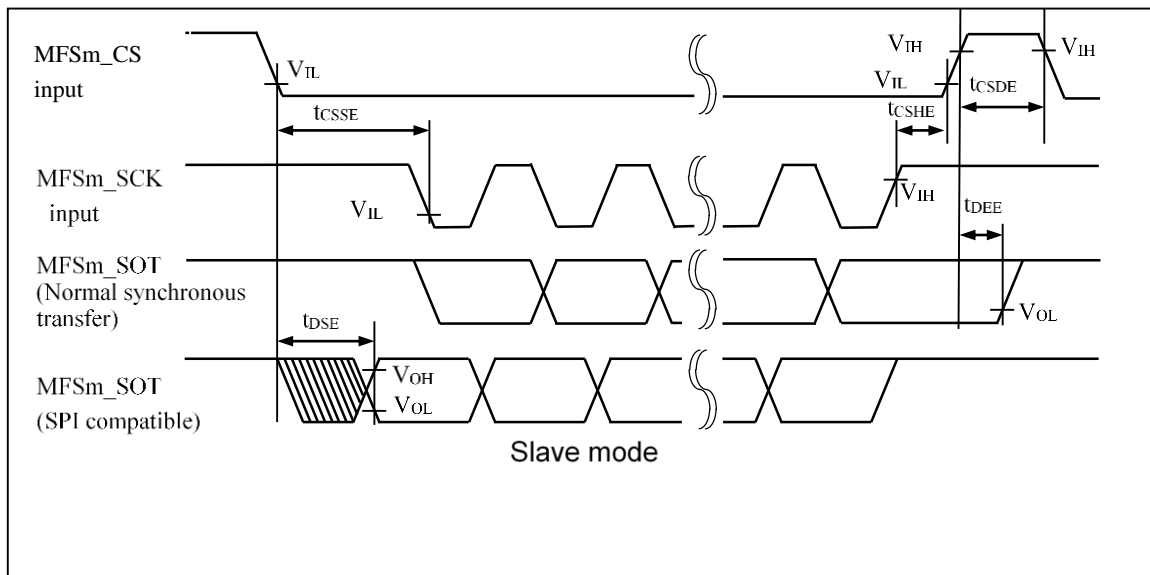
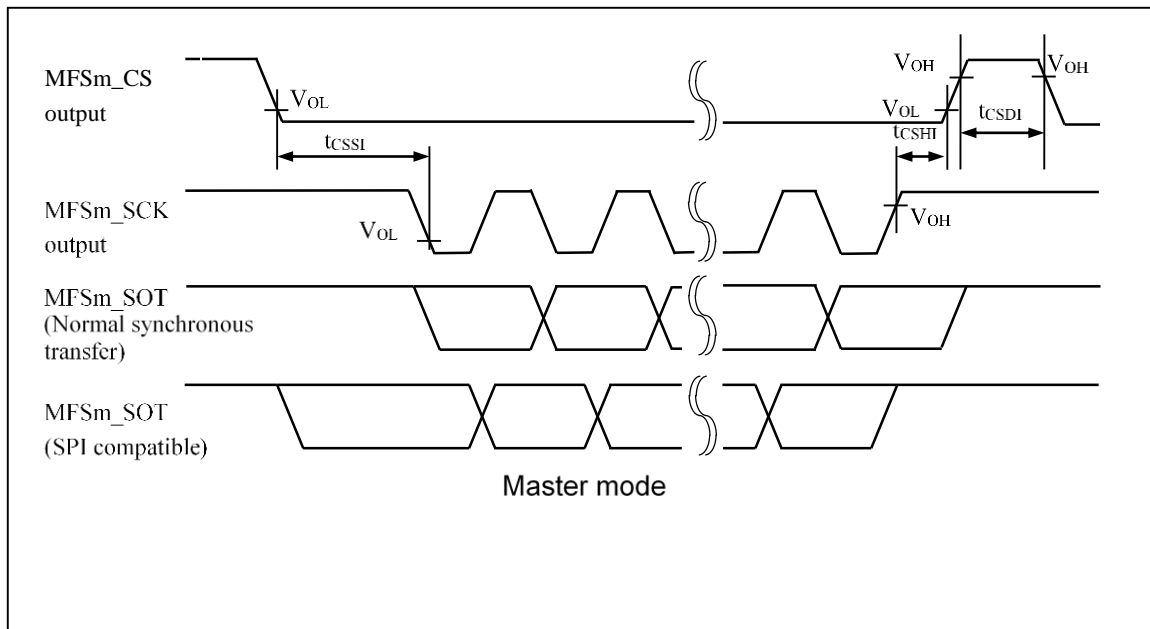
For details on *1, *2, and *3 above, see the hardware manual.

*4: n = 0:ch.0 to ch.7, n = 1:ch.8 to ch.11

*5: For the details of x or y value, see section 5 Pin Descriptions.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(6) Serial Chip Select Used (SCSCR:CSSEN = 1)

- Serial clock output signal detect level "L" (SMR, SCSFR:SCINV = 1)
- Serial chip select inactive level "H" (SCSCR, SCSFR:CSLVL = 1)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|--|-------------------|---|--|---|---|------|---------|
| | | | | Min | Max | | |
| SCS ↓ → SCK ↑ setup time | t _{CSSU} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Master mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | t _{CSSU} ^{*1} - 50 | - | ns | |
| SCK ↓ → SCS ↑ hold time | t _{CSDH} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | t _{CSDH} ^{*2} + 0 | - | ns | |
| SCS deselect time | t _{CSDI} | MFSm_CSy_x ^{*5} (m = 0 to 11) | | t _{CSDS} ^{*3} - 50 + 5t _{CLK_LCPnA} ^{*4} | - | ns | |
| SCS ↓ → SCK ↑ setup time | t _{CSSS} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Slave mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 3t _{CLK_LCPnA} ^{*4} + 30 | - | ns | |
| SCK ↓ → SCS ↑ hold time | t _{CSDH} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | 0 | - | ns | |
| SCS deselect time | t _{CSDI} | FMSm_CSy_x ^{*5} (m = 0 to 11) | | 3t _{CLK_LCPnA} ^{*4} + 30 | - | ns | |
| SCS ↓ → SOT delay time | t _{DSE} | FMSm_CSy_x ^{*5} MFSm_SOT_x ^{*5} (m = 0 to 11) | | - | 40 | ns | |
| SCS ↑ → SOT delay time | t _{DEE} | FMSm_CSy_x ^{*5} MFSm_SOT_x ^{*5} (m = 0 to 11) | | 0 | - | ns | |
| SCK ↑ → SCS ↓ clock switching time | t _{SCC} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Master mode round operation (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 3t _{CLK_LCPnA} ^{*4} + 0 | 3t _{CLK_LCPnA} ^{*4} + 50 | ns | |

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSDH} = SCSTR:CSDH[7:0] x serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

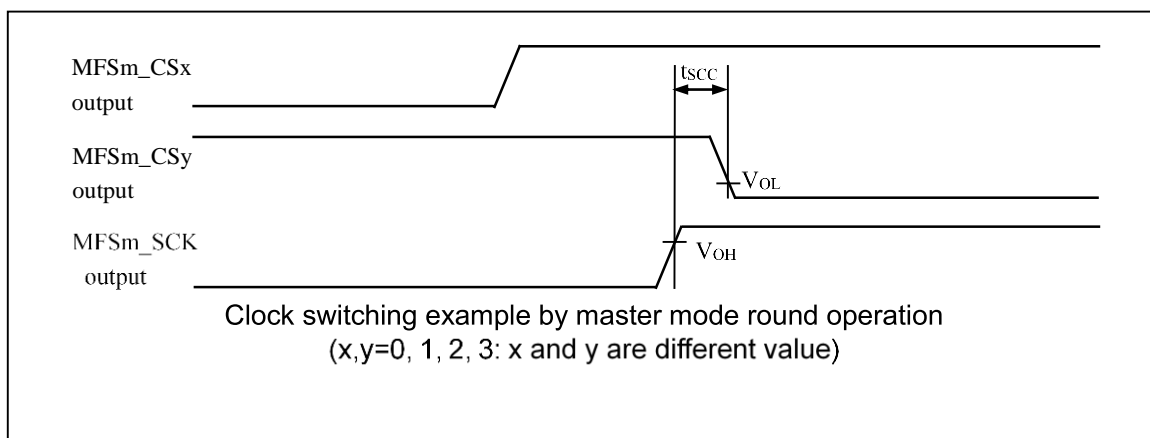
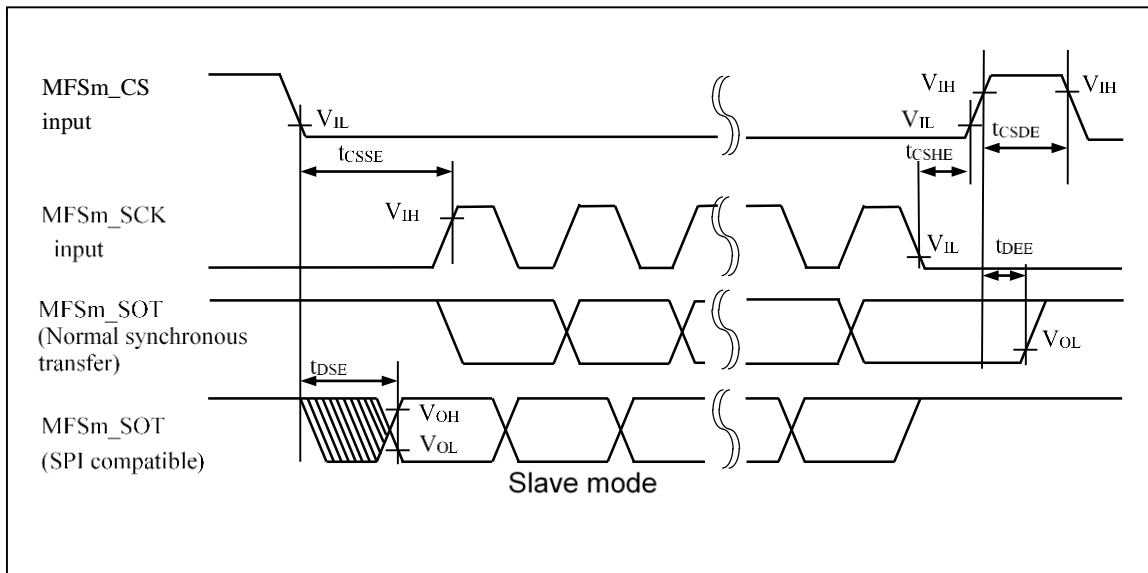
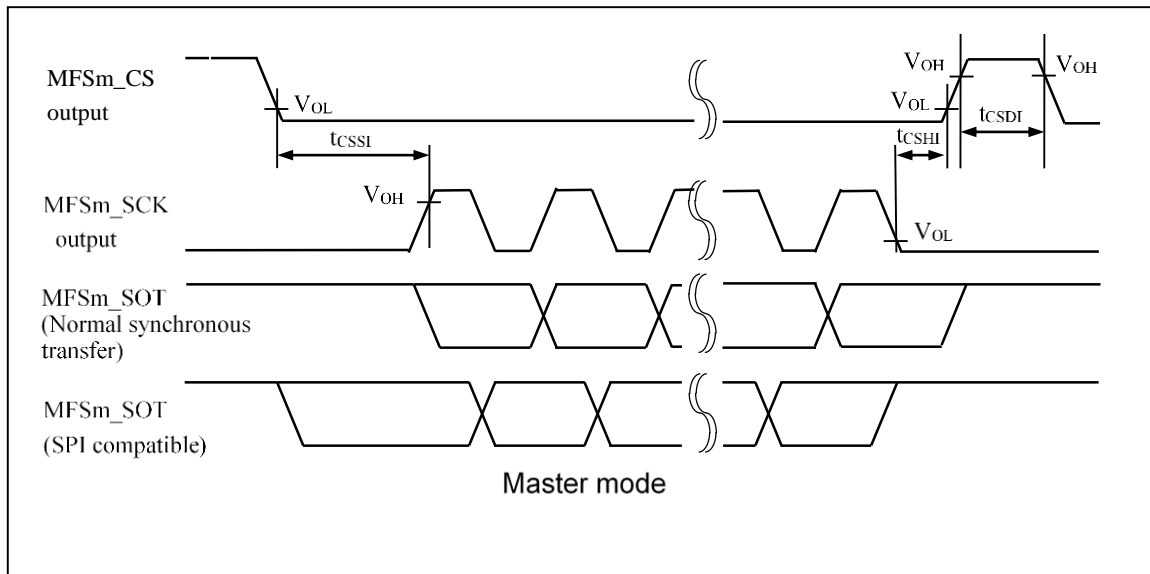
For details on *1, *2, and *3 above, see the hardware manual.

*4: n = 0:ch.0 to ch.7, n = 1:ch.8 to ch.11

*5: For the details of x or y value, see section 5 Pin Descriptions.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters. For details, see the hardware manual.



(7) Serial Chip Select Used (SCSCR:CSSEN = 1)

■ Serial clock output signal detect level "H" (SMR, SCSFR:SCINV = 0)

■ Serial chip select inactive level "L" (SCSCR, SCSFR:CSLVL = 0)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks | |
|--|-------------------|---|--|--|---|---|---------|--|
| | | | | Min | Max | | | |
| SCS ↑ → SCK ↓ setup time | t _{CSSU} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Master mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | t _{CSSU} ^{*1} - 50 | - | ns | | |
| SCK ↑ → SCS ↓ hold time | t _{CSDH} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | t _{CSDH} ^{*2} + 0 | - | ns | | |
| SCS deselect time | t _{CSDI} | MFSm_CSy_x ^{*5} (m = 0 to 11) | | t _{CSDS} ^{*3} - 50 + 5 t _{CLK_LCPnA} ^{*4} | - | ns | | |
| SCS ↑ → SCK ↓ setup time | t _{CSSS} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Slave mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 3t _{CLK_LCPnA} ^{*4} + 30 | - | ns | | |
| SCK ↑ → SCS ↓ hold time | t _{CSDH} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | 0 | - | ns | | |
| SCS deselect time | t _{CSDI} | MFSm_CSy_x ^{*5} (m = 0 to 11) | | 3t _{CLK_LCPnA} ^{*4} + 30 | - | ns | | |
| SCS ↑ → SOT delay time | t _{DSE} | MFSm_CSy_x ^{*5} MFSm_SOT_x ^{*5} (m = 0 to 11) | | - | 40 | ns | | |
| SCS ↓ → SOT delay time | t _{DEE} | MFSm_CSy_x ^{*5} MFSm_SOT_x ^{*5} (m = 0 to 11) | | 0 | - | ns | | |
| SCK ↓ → SCS ↑ clock switching time | t _{SCC} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | Master mode round operation (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 3t _{CLK_LCPnA} ^{*4} + 0 | 3t _{CLK_LCPnA} ^{*4} + 50 | ns | |

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSDH} = SCSTR:CSDH[7:0] x serial chip select timing operating clock

*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock

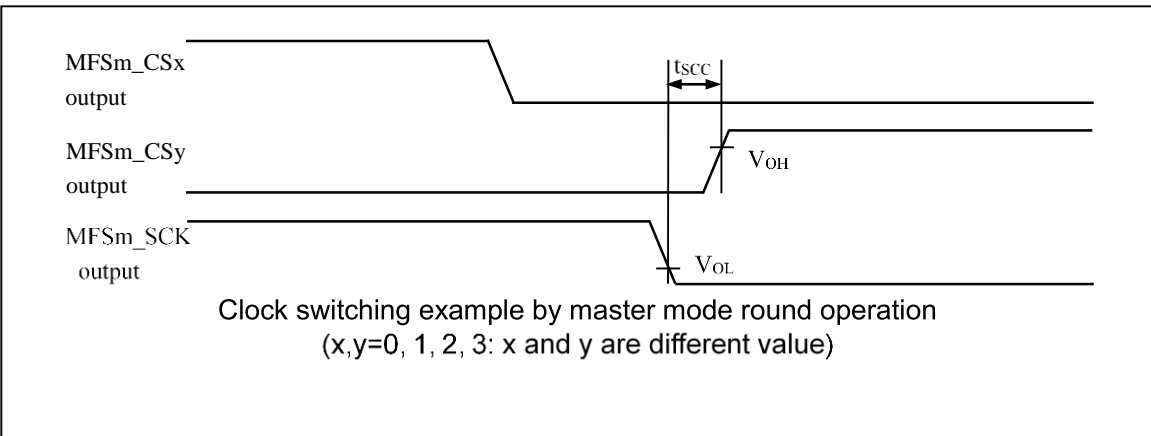
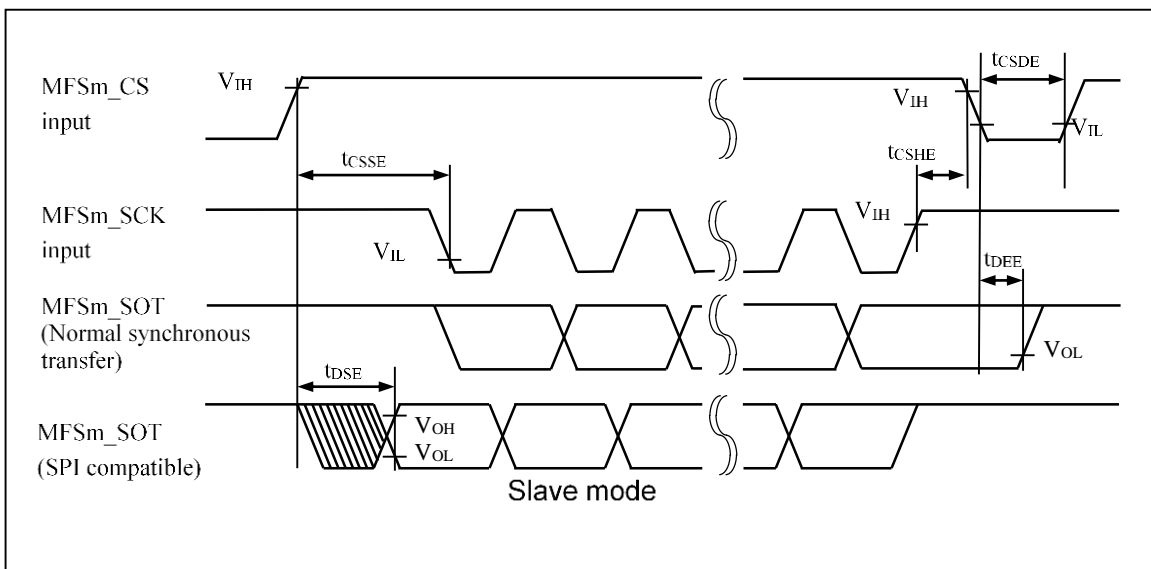
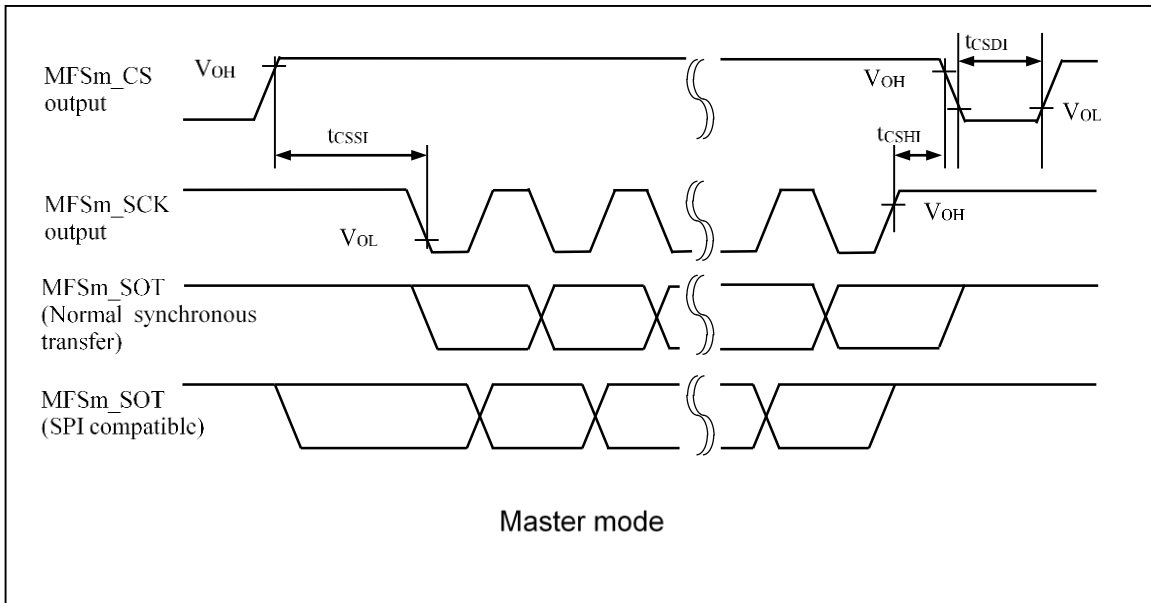
For details on *1, *2, and *3 above, see the hardware manual.

*4: n = 0:ch.0 to ch.7, n = 1:ch.8 to ch.11

*5: For the details of x or y value, see section 5 Pin Descriptions.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual



(8) Serial Chip Select Used (SCSCR:CSSEN = 1)

- Serial clock output signal detect level "L" (SMR, SCSFR:SCINV = 1)
- Serial chip select inactive level "L" (SCSCR, SCSFR:CSLVL = 0)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|--|-------------------|---|--|--|---|------|---------|
| | | | | Min | Max | | |
| SCS \uparrow \rightarrow SCK \uparrow setup time | t _{CSSU} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Master mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | t _{CSSU} ^{*1} - 50 | - | ns | |
| SCK \downarrow \rightarrow SCS \downarrow hold time | t _{CSDH} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | t _{CSDH} ^{*2} + 0 | - | ns | |
| SCS deselect time | t _{CSDI} | FSm_CSy_x ^{*5} (m = 0 to 11) | | t _{CSDS} ^{*3} - 50 + 5 t _{CLK_LCPnA} ^{*4} | - | ns | |
| SCS \uparrow \rightarrow SCK \uparrow setup time | t _{CSSS} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Slave mode (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2mA) | 3t _{CLK_LCPnA} ^{*4} + 30 | - | ns | |
| SCK \downarrow \rightarrow SCS \downarrow hold time | t _{CSDH} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | | 0 | - | ns | |
| SCS deselect time | t _{CSDI} | MFSm_CSy_x ^{*5} (m = 0 to 11) | | 3t _{CLK_LCPnA} ^{*4} + 30 | - | ns | |
| SCS \uparrow \rightarrow SOT delay time | t _{DSE} | MFSm_CSy_x ^{*5} MFSm_SOT_x ^{*5} (m = 0 to 11) | | - | 40 | ns | |
| SCS \downarrow \rightarrow SOT delay time | t _{DEE} | MFSm_CSy_x ^{*5} MFSm_SOT_x ^{*5} (m = 0 to 11) | | 0 | - | ns | |
| SCK \uparrow \rightarrow SCS \uparrow clock switching time | t _{SCC} | MFSm_SCK_x ^{*5} MFSm_CSy_x ^{*5} (m = 0 to 11) | Master mode round operation (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 3t _{CLK_LCPnA} ^{*4} + 0 | 3t _{CLK_LCPnA} ^{*4} + 50 | ns | |

*1: t_{CSSU} = SCSTR:CSSU[7:0] x serial chip select timing operating clock

*2: t_{CSDH} = SCSTR:CSDH[7:0] x serial chip select timing operating clock

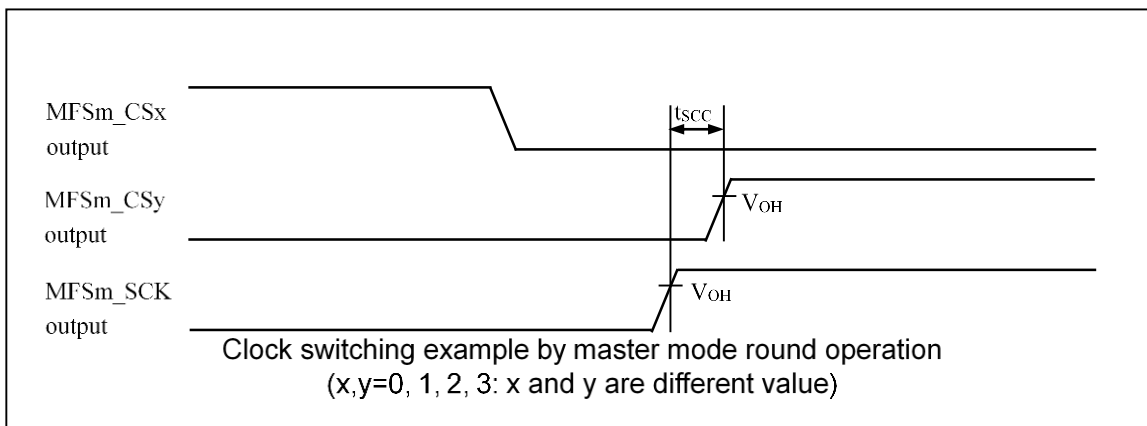
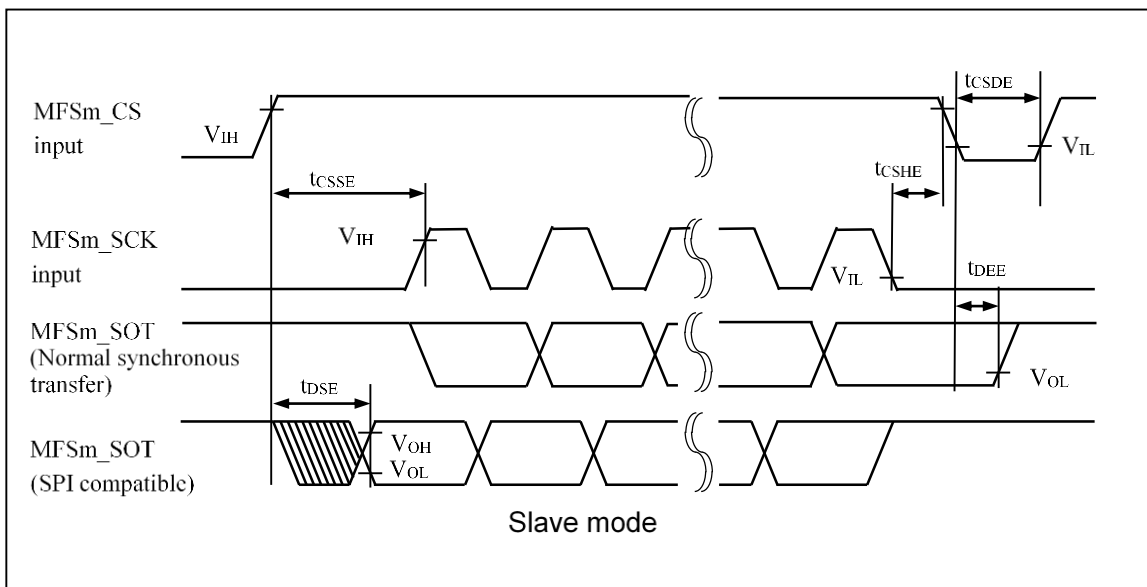
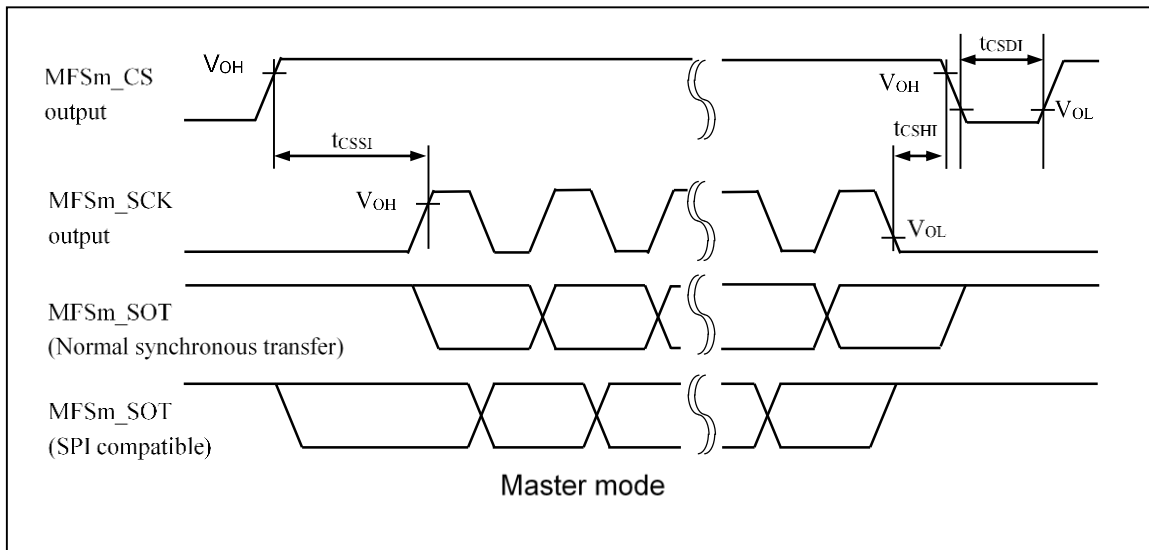
*3: t_{CSDS} = SCSTR:CSDS[15:0] x serial chip select timing operating clock
For details on *1, *2, and *3 above, see the hardware manual.

*4: n = 0:ch.0 to ch.7, n = 1:ch.8 to ch.11

*5: For the details of x or y value, see section 5 Pin Descriptions.

Notes:

- This is the AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by the internal operating clock used and other parameters.
For details, see the hardware manual.



7.4.6.3 LIN Interface (v2.1) (LIN Communication Control Interface (v2.1)) Timing (SMR:MD2-0 = 0b011)

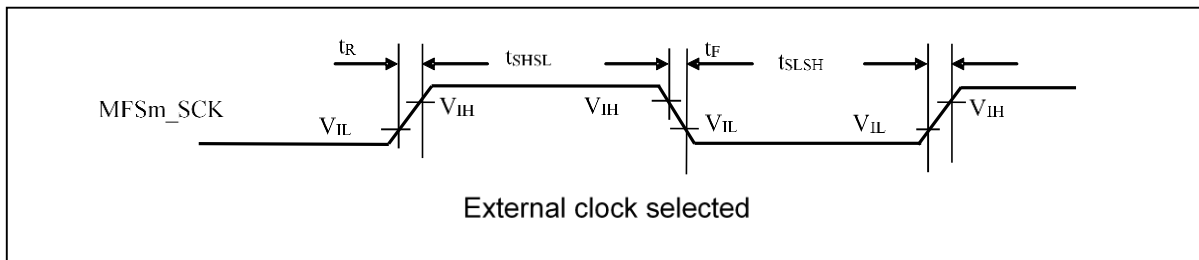
External Clock Selected (BGR:EXT = 1)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|------------|---|---|----------------------------|-----|------|---------|
| | | | | Min | Max | | |
| Serial clock "L" pulse width | t_{SLSH} | MFSm_SCK_x ^{*2} (m = 0 to 11) | (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | $t_{CLK_LCPnA}^{*1} + 10$ | - | ns | |
| Serial clock "H" pulse width | t_{SHSL} | MFSm_SCK_x ^{*2} (m = 0 to 11) | | $t_{CLK_LCPnA}^{*1} + 10$ | - | ns | |
| SCK falling time | t_F | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |
| SCK rising time | t_R | MFSm_SCK_x ^{*2} (m = 0 to 11) | | - | 5 | ns | |

*1: n = 0: ch.0 to ch.7, n = 1: ch.8 to ch.11

*2: For the details of x value, see section 5.1 Pin Descriptions.



7.4.6.4 I²C Timing (SMR:MD2-0 = 0b100)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Standard Mode | | Fast Mode | | Unit | Remarks |
|--|--------------------|--|---|--------------------------------|--------------------|--------------------------------|-------------------|------|---------|
| | | | | Min | Max | Min | Max | | |
| SCL clock frequency | f _{SCL} | MFSm_SCL (m = 0,1,4 to 11) | C _L = 50 pF, R = (V _p /I _{OL}) ^{*1} | 0 | 100 | 0 | 400 | kHz | |
| Repeat "start" condition hold time SDA↓ → SCL↓ | t _{HDSTA} | MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11) | | 4.0 | - | 0.6 | - | μs | |
| Period of "L" for SCL clock | t _{LOW} | MFSm_SCL (m = 0,1,4 to 11) | | 4.7 | - | 1.3 | - | μs | |
| Period of "H" for SCL clock | t _{HIGH} | MFSm_SCL (m = 0,1,4 to 11) | | 4.0 | - | 0.6 | - | μs | |
| Repeat "start" condition setup time SCL↑ → SDA↓ | t _{SUSTA} | MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11) | | 4.7 | - | 0.6 | - | μs | |
| Data hold time SCL↓ → SDA↓↑ | t _{HDDAT} | MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11) | | 0 | 3.45 ^{*2} | 0 | 0.9 ^{*3} | μs | |
| Data setup time SDA↓↑ → SCL↑ | t _{SUDAT} | MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11) | | 250 | - | 100 | - | ns | |
| Stop condition setup time SCL↑ → SDA↑ | t _{SUSTO} | MFSm_SDA, MFSm_SCL (m = 0,1,4 to 11) | | 4.0 | - | 0.6 | - | μs | |
| Bus-free time between "stop" condition and "start" condition | t _{BUF} | - | | 4.7 | - | 1.3 | - | μs | |
| Noise filter | t _{SP} | - | | t _{NFT} ^{*4} | - | t _{NFT} ^{*4} | - | ns | |

Notes: Only ch.6 and ch.7 are standard mode/ Fast mode correspondence. In other ch., only a standard mode is correspondence.

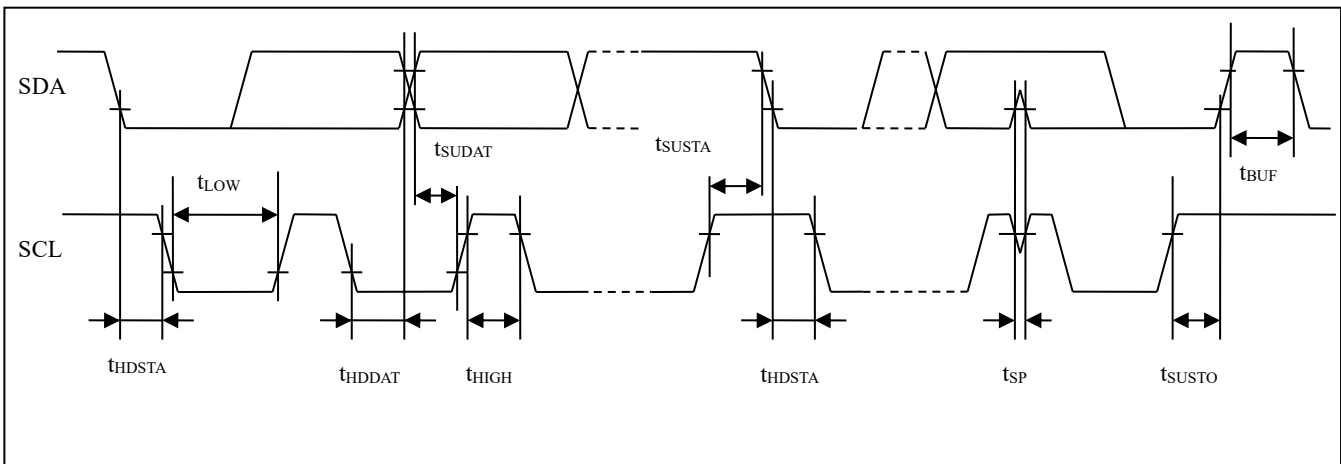
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively.
V_p shows the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} must only be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A fast mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{NFT} = (NFCR: NFT[4:0] + 1) × 2 × t_{CLK_LCP0A} (ch.0, ch.1, ch.4 to ch.7)

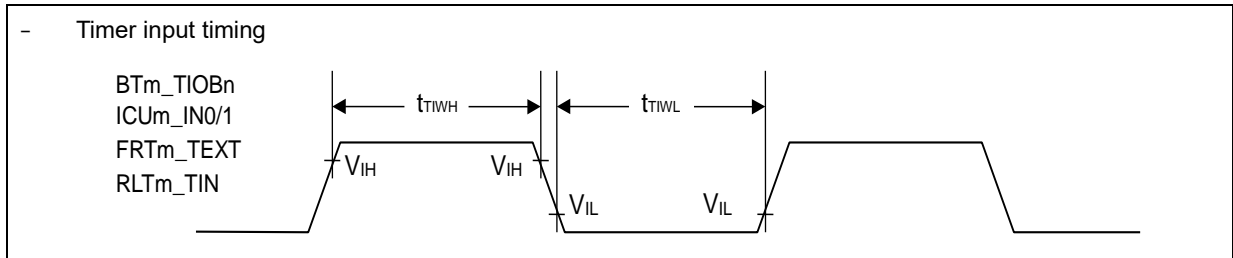
t_{NFT} = (NFCR: NFT[4:0] + 1) × 2 × t_{CLK_LCP1A} (ch.8 to ch.11)



7.4.7 Timer Input

(Condition: See section 7.2 Recommended Operating Conditions)

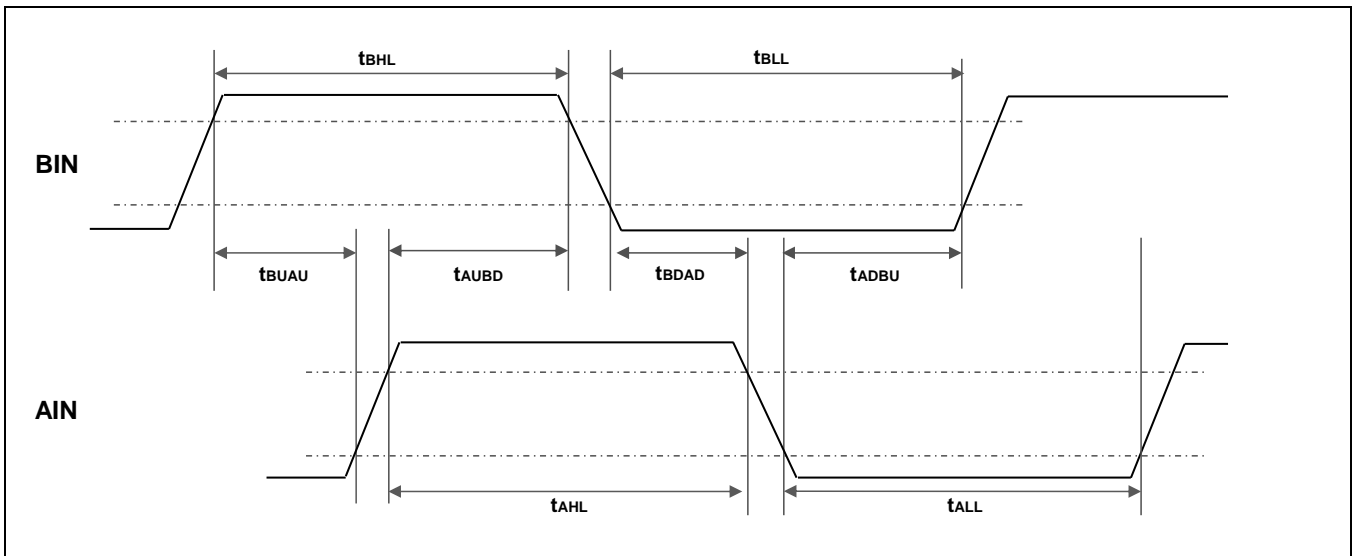
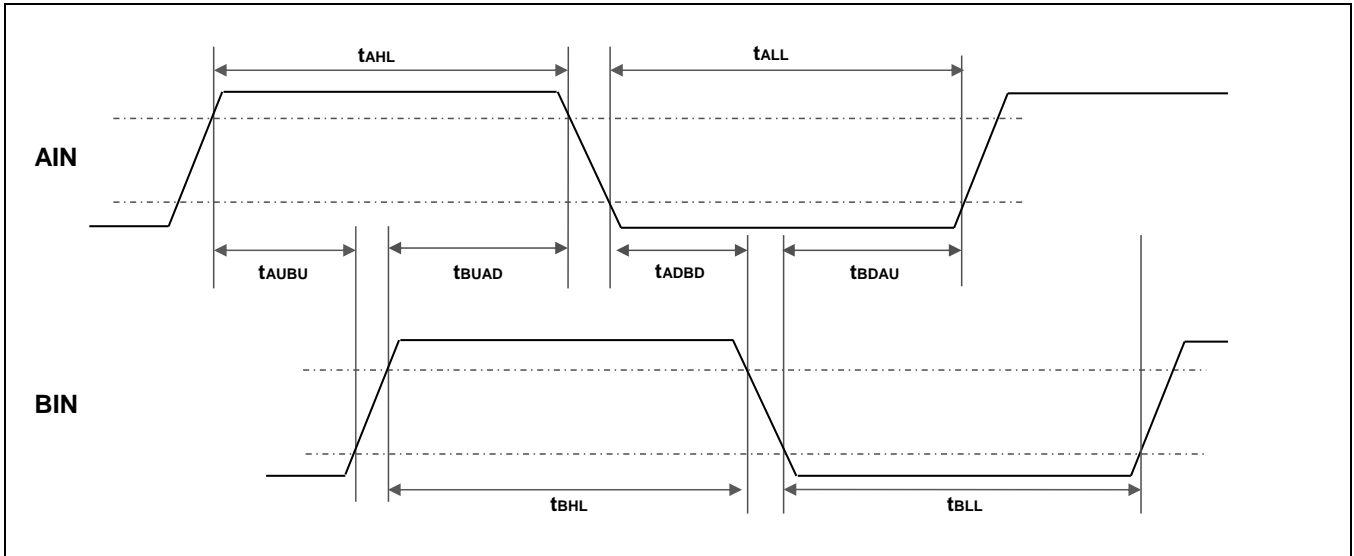
| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------|--------------------------|---|------------|-------------------|-----|------|-------------------------------|
| | | | | Min | Max | | |
| Input pulse width | t_{TWH} , t_{TWL} | BTm_TIOBn_0, BTm_TIOBn_1 (m = 0 to 15, n = 2m) | - | $4t_{CLK_LCP1A}$ | - | ns | $4t_{CLK_LCP1A} \geq 100$ ns |
| | | | | 100 | - | ns | $4t_{CLK_LCP1A} < 100$ ns |
| | | ICUm_IN0_0, ICUm_IN1_0, ICUm_IN0_1, ICUm_IN1_1 (m = 0,1, 2, 8, 9, 10) | - | $4t_{CLK_LCP0A}$ | - | ns | $4t_{CLK_LCP0A} \geq 100$ ns |
| | | | | 100 | - | ns | $4t_{CLK_LCP0A} < 100$ ns |
| | | FRTm_TEXT (m = 0, 1, 2, 3, 4, 8, 9, 10) | - | $4t_{CLK_LCP0A}$ | - | ns | $4t_{CLK_LCP0A} \geq 100$ ns |
| | | | | 100 | - | ns | $4t_{CLK_LCP0A} < 100$ ns |
| | | RLTm_TIN_0, RLTm_TIN_1 (m = 0 to 3) | - | $4t_{CLK_LCP0A}$ | - | ns | $4t_{CLK_LCP0A} \geq 100$ ns |
| | | | | 100 | - | ns | $4t_{CLK_LCP0A} < 100$ ns |
| | | RLTm_TIN_0, RLTm_TIN_1 (m = 16,17) | - | $4t_{CLK_LCP1A}$ | - | ns | $4t_{CLK_LCP1A} \geq 100$ ns |
| | | | | 100 | - | ns | $4t_{CLK_LCP1A} < 100$ ns |

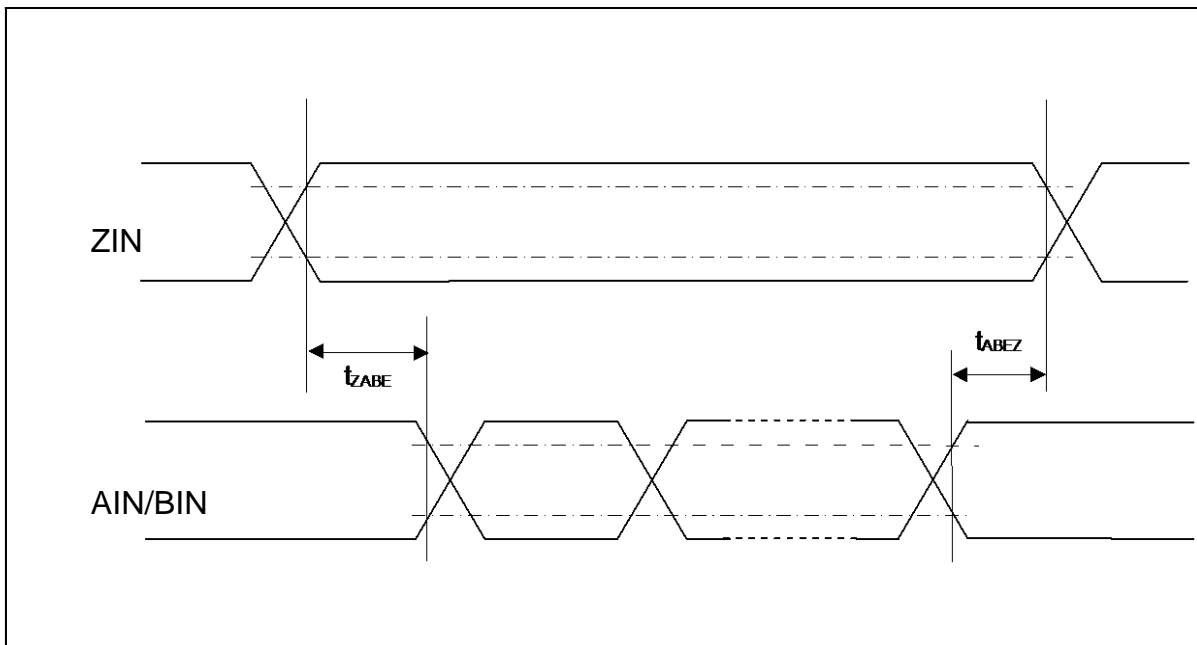
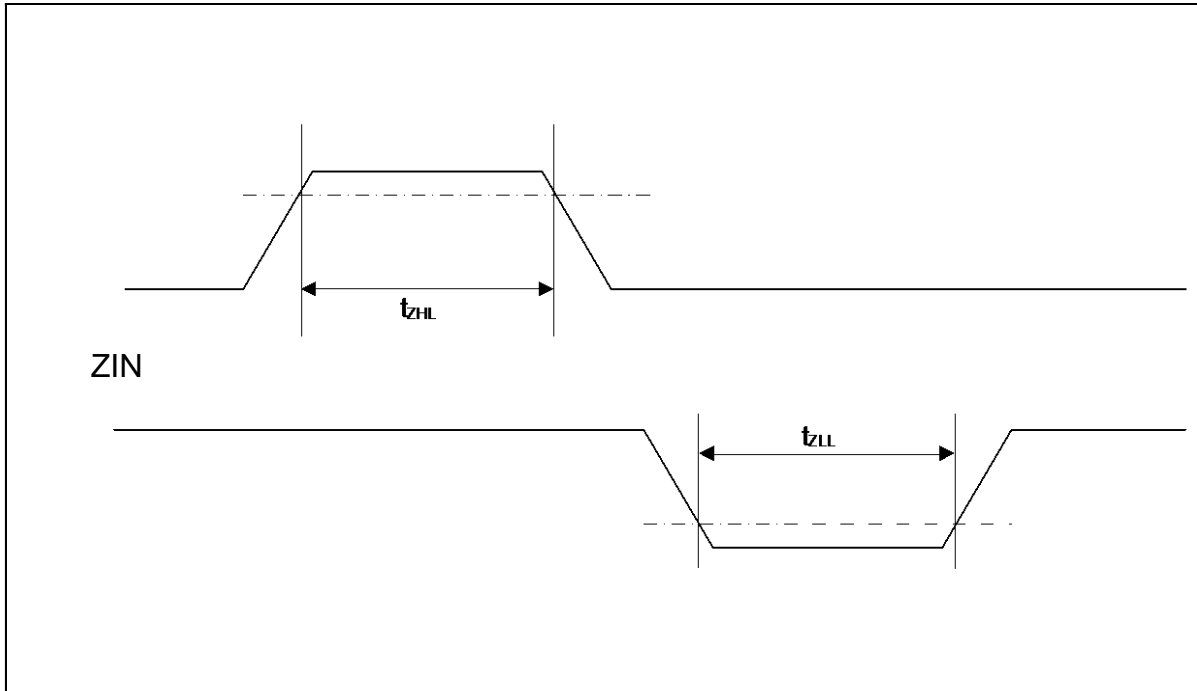


7.4.8 QPRC Timing

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|--|--------------------|--|-------------------------|-------------------------|-----|------|-------------------------------------|
| | | | | Min | Max | | |
| AIN pin "H" width | t _{AHL} | QPRCm_AIN (m = 8,9) | - | 4t _{CLK_LCP0A} | - | ns | 4t _{CLK_LCP0A} ≥ 100 ns |
| AIN pin "L" width | t _{ALL} | QPRCm_AIN (m = 8,9) | - | | | | |
| BIN pin "H" width | t _{BHL} | QPRCm_AIN (m = 8,9) | - | | | | |
| BIN pin "L" width | t _{BLL} | QPRCm_AIN (m = 8,9) | - | | | | |
| Time from AIN pin "H" level to BIN rise | t _{AUBU} | QPRCm_AIN, QPRCm_BIN (m = 8,9) | PC_Mode2 or PC_Mode3 | | | | |
| Time from BIN pin "H" level to AIN fall | t _{BUAD} | QPRCm_AIN, QPRCm_BIN (m = 8,9) | PC_Mode2 or PC_Mode3 | | | | |
| Time from AIN pin "L" level to BIN fall | t _{ADBD} | QPRCm_AIN, QPRCm_BIN (m = 8,9) | PC_Mode2 or PC_Mode3 | | | | |
| Time from BIN pin "L" level to AIN rise | t _{BDAU} | QPRCm_AIN, QPRCm_BIN (m = 8,9) | PC_Mode2 or PC_Mode3 | | | | |
| Time from BIN pin "H" level to AIN rise | t _{BUAU} | QPRCm_AIN, QPRCm_BIN (m = 8,9) | PC_Mode2 or PC_Mode3 | | | | |
| Time from AIN pin "H" level to BIN fall | t _{AUBD} | QPRCm_AIN, QPRCm_BIN (m = 8,9) | PC_Mode2 or PC_Mode3 | | | | |
| Time from BIN pin "L" level to AIN fall | t _{BDAD} | QPRCm_AIN, QPRCm_BIN (m = 8,9) | PC_Mode2 or PC_Mode3 | | | | |
| Time from AIN pin "L" level to BIN rise | t _{ADBU} | QPRCm_AIN, QPRCm_BIN (m = 8,9) | PC_Mode2 or PC_Mode3 | | | | |
| ZIN pin "H" width | t _{ZHL} | PRCm_ZIN (m = 8,9) | QCR:CGSC = "0" | | | | |
| ZIN pin "L" width | t _{ZLL} | PRCm_ZIN (m = 8,9) | QCR:CGSC = "0" | | | | |
| Time from determined ZIN level to AIN/BIN rise and fall | t _{ZABE} | QPRCm_AIN, QPRCm_BIN, QPRCm_ZIN (m = 8,9) | QCR:CGSC = "1" | | | | |
| Time from AIN/BIN rise and fall time to determined ZIN level | t _{ZABEZ} | QPRCm_AIN, QPRCm_BIN, QPRCm_ZIN (m = 8,9) | QCR:CGSC = "1" | | | | |



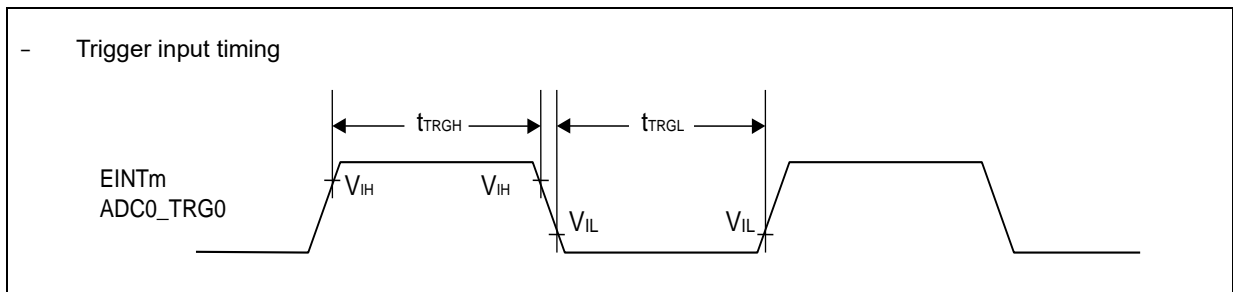


7.4.9 Trigger Input

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------|----------------------------|---------------------------------------|------------|-------------------|-----|---------|-------------------------------|
| | | | | Min | Max | | |
| Input pulse width | t_{TRGH} , t_{TRGL} | $EINTm_x^{*1}$ ($m = 0$ to 23) | - | 100 | - | ns | |
| | | ADC0_TRG0_0, ADC0_TRG0_1 | - | $5t_{CLK_LCP1A}$ | - | ns | $5t_{CLK_LCP1A} \geq 100$ ns |
| | | | | 100 | - | ns | $5t_{CLK_LCP1A} < 100$ ns |
| | | $EINTm_x^{*1}$ ($m = 0$ to 23) | - | 1 | - | μ s | Stop mode |

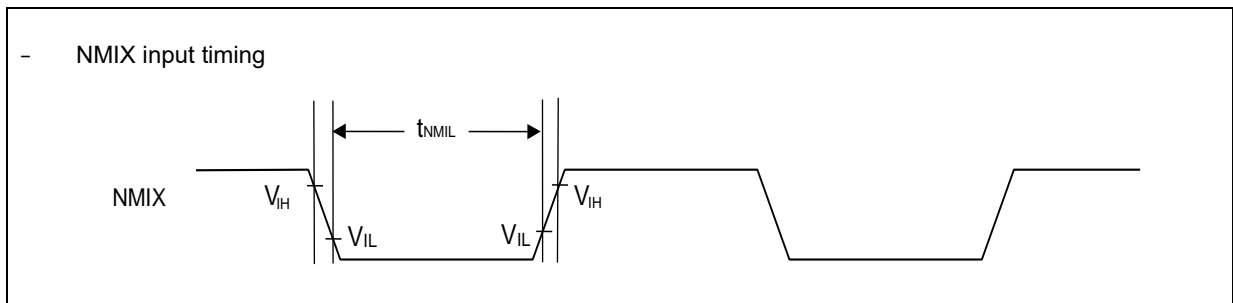
*1: For the details of x value, see section 5.1 “Pin Descriptions”.



7.4.10 NMI Input

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------|------------|----------|------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| Input pulse width | t_{NMIL} | NMIX | - | 300 | - | ns | |



7.4.11 Low Voltage Detection (External Voltage)
7.4.11.1 Low-voltage Detection (External Low-voltage Detection for LVDH1)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Guaranteed MCU Operation Range | Remarks | | |
|------------------------------------|-------------------|------------------|-----------------------------------|-------|-----|------|------|--------------------------------|---------|----|----|
| | | | | Min | Typ | Max | | | | | |
| Detection voltage | V _{DLAT} | V _{CC5} | LVDH1V = 0b000 | 2.61 | 2.7 | 2.79 | V | No | *1 | | |
| Release voltage | V _{DLAT} | V _{CC5} | | 2.7 | 2.8 | 2.9 | | | | | |
| Detection voltage | V _{DLAT} | V _{CC5} | LVDH1V = 0b001 | 2.7 | 2.8 | 2.9 | V | Yes | - | | |
| Release voltage | V _{DLAT} | V _{CC5} | | 2.8 | 2.9 | 3.0 | | | | | |
| Detection voltage | V _{DLAT} | V _{CC5} | LVDH1V = 0b010 | 3.47 | 3.6 | 3.73 | V | | | | |
| Release voltage | V _{DLAT} | V _{CC5} | | 3.57 | 3.7 | 3.83 | | | | | |
| Detection voltage | V _{DLAT} | V _{CC5} | LVDH1V = 0b011 | 3.67 | 3.8 | 3.93 | V | | | | |
| Release voltage | V _{DLAT} | V _{CC5} | | 3.76 | 3.9 | 4.04 | | | | | |
| Detection voltage | V _{DLAT} | V _{CC5} | LVDH1V = 0b100 | 3.86 | 4 | 4.14 | V | | | | |
| Release voltage | V _{DLAT} | V _{CC5} | | 3.96 | 4.1 | 4.24 | | | | | |
| Detection voltage | V _{DLAT} | V _{CC5} | LVDH1V = 0b101 | 4.05 | 4.2 | 4.35 | V | | | | |
| Release voltage | V _{DLAT} | V _{CC5} | | 4.15 | 4.3 | 4.45 | | | | | |
| Detection voltage | V _{DLAT} | V _{CC5} | LVDH1V = 0b110 | 2.41 | 2.5 | 2.59 | V | | | No | *1 |
| Release voltage | V _{DLAT} | V _{CC5} | | 2.51 | 2.6 | 2.69 | | | | | |
| Detection voltage | V _{DLAT} | V _{CC5} | LVDH1V = 0b111 (Initial value) | 2.51 | 2.6 | 2.69 | V | | | | |
| Release voltage | V _{DLAT} | V _{CC5} | | 2.61 | 2.7 | 2.79 | | | | | |
| Low-voltage detection/release time | T _d | - | - | - | - | 40 | μs | - | *2 | | |
| Power supply voltage regulation | - | V _{CC5} | - | -2 | - | 2 | V/ms | - | *3 | | |

Notes:

- *1: These LVD settings cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage (2.7 V).
- *2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.
- *3: Suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage.

7.4.11.2 Low-voltage Detection (External Low-voltage Detection for LVDH2)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Guaranteed MCU Operation Range | Remarks |
|------------------------------------|---------------------|---------------------|-----------------|-------|-----|------|------|--------------------------------|---------|
| | | | | Min | Typ | Max | | | |
| Detection voltage | V _{DLAT53} | V _{CC53_1} | LVDH2V = 0b0001 | 2.7 | 2.8 | 2.9 | V | Yes | - |
| Release voltage | V _{DLAT53} | V _{CC53_1} | (Initial value) | 2.8 | 2.9 | 3 | V | | |
| Detection voltage | V _{DLAT53} | V _{CC53_1} | LVDH2V = 0b0010 | 3.47 | 3.6 | 3.73 | V | | |
| Release voltage | V _{DLAT53} | V _{CC53_1} | | 3.57 | 3.7 | 3.83 | V | | |
| Detection voltage | V _{DLAT53} | V _{CC53_1} | LVDH2V = 0b0011 | 3.67 | 3.8 | 3.93 | V | | |
| Release voltage | V _{DLAT53} | V _{CC53_1} | | 3.76 | 3.9 | 4.04 | V | | |
| Detection voltage | V _{DLAT53} | V _{CC53_1} | LVDH2V = 0b0100 | 3.86 | 4.0 | 4.14 | V | | |
| Release voltage | V _{DLAT53} | V _{CC53_1} | | 3.96 | 4.1 | 4.24 | V | | |
| Detection voltage | V _{DLAT53} | V _{CC53_1} | LVDH2V = 0b0101 | 4.05 | 4.2 | 4.35 | V | | |
| Release voltage | V _{DLAT53} | V _{CC53_1} | | 4.15 | 4.3 | 4.45 | V | | |
| Low-voltage detection/release time | T _{d53} | - | - | - | - | 40 | μs | - | *1 |
| Power supply voltage regulation | - | V _{CC53_1} | - | -2 | - | 2 | V/ms | - | *2 |

Notes:

- *1: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.
- *2: Suppress the change of the power supply within the range of the power-supply voltage regulation to do a low-voltage detection by detecting voltage.

7.4.12 Low-Voltage Detection (Internal Voltage Specs)

7.4.12.1 Low-voltage Detection (Internal Low-voltage Detection for LVDL0)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|----------------------------|------------------|----------|------------|-------|-------|------|------|---------|
| | | | | Min | Typ | Max | | |
| Detection voltage | V _{RDL} | - | - | 0.82 | 0.85 | 0.88 | V | *1 |
| Release voltage | V _{RDL} | - | - | 0.89 | 0.925 | 0.96 | V | |
| Low-voltage detection time | T _{Rd} | - | - | - | - | 30 | μs | *2 |

Note:

- *1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as this detection level is below the minimum guaranteed MCU operation voltage.
- *2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.

7.4.12.2 Low-voltage Detection (Internal Low-voltage Detection for LVDL1)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Guaranteed MCU Operation Range | Remarks |
|----------------------------|--------------------|----------|-----------------------------------|-------|-------|------|------|--------------------------------|---------|
| | | | | Min | Typ | Max | | | |
| Detection voltage | V _{RDLAT} | - | LVDL1V = 0b000 (Initial value) | 0.84 | 0.875 | 0.91 | V | No | *1 |
| Release voltage | V _{RDLAT} | - | | 0.92 | 0.95 | 0.98 | V | | |
| Detection voltage | V _{RDLAT} | - | LVDL1V = 0b001 | 0.92 | 0.95 | 0.98 | V | | |
| Release voltage | V _{RDLAT} | - | | 0.98 | 1.025 | 1.06 | V | | |
| Low-voltage detection time | T _{Rd} | - | - | - | - | 30 | μs | - | *2 |

Notes:

- *1: This LVD cannot be used to reliably generate a reset before voltage dips below minimum guaranteed MCU operation voltage, as these detection levels are below the minimum guaranteed MCU operation voltage.
- *2: After the brown-out event where the voltage level dips below the detection threshold for less than this time, the detection may occur or be canceled.

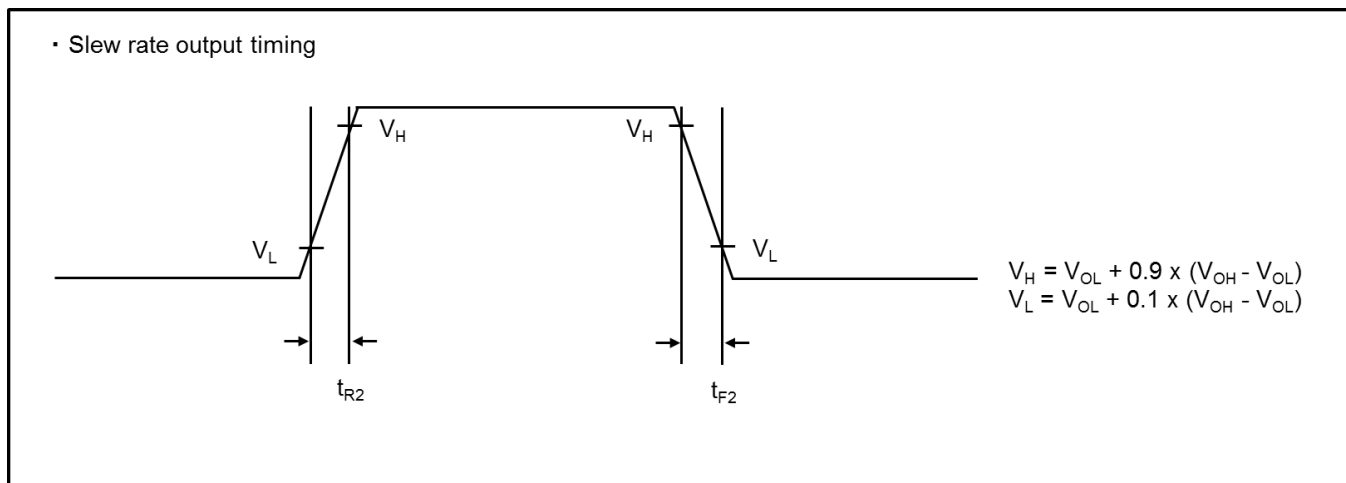
7.4.13 High Current Output Slew Rate

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | | Unit | Remarks |
|-------------------------|------------------------|-----------------------------|------------|-------|-----|-----|------|------------------------|
| | | | | Min | Typ | Max | | |
| Output rise / fall time | t_{R2} , t_{F2} | GPIO of DV _{CC} *1 | - | 15 | - | 100 | ns | Load capacitance 85 pF |

*1: For the details of GPIO group, see section 5.3 Input Level Setting/ Output Drive Capacity Setting.

When I/O output drive capacity setting is 30 mA.



7.4.14 External Bus Interface Timing

7.4.14.1 Clock Output Timing

(TA: Recommended operating conditions, $V_{cc53_1} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---------------------|------------|----------|---|-------------------|-------------------|------|---------|
| | | | | Min | Max | | |
| Cycle time | t_{CYC} | MCLK | $(C_L = 20\text{ pF}, I_{OH} = -5\text{ mA}, I_{OL} = 5\text{ mA})$ | 25 | - | ns | |
| Clock high width *1 | t_{CHCL} | MCLK | | $dH_{tCYC} - 4.5$ | $dH_{tCYC} + 4.5$ | ns | |
| Clock low width *2 | t_{CLCH} | MCLK | | $dL_{tCYC} - 4.5$ | $dL_{tCYC} + 4.5$ | ns | |

(TA: Recommended operating conditions, $V_{cc53_1} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---------------------|------------|----------|---|-------------------|-------------------|------|---------|
| | | | | Min | Max | | |
| Cycle time | t_{CYC} | MCLK | $(C_L = 20\text{ pF}, I_{OH} = -2\text{ mA}, I_{OL} = 2\text{ mA})$ | 31.25 | - | ns | |
| Clock high width *1 | t_{CHCL} | MCLK | | $dH_{tCYC} - 4.5$ | $dH_{tCYC} + 4.5$ | ns | |
| Clock low width *2 | t_{CLCH} | MCLK | | $dL_{tCYC} - 4.5$ | $dL_{tCYC} + 4.5$ | ns | |

*1: If division-ratio is even value, dH is equivalent to 0.5.

Otherwise, dH is calculated as the following.

$dH = \text{The number rounding "division-ratio} \times 0.5"$ down to the nearest integer / division-ratio

division-ratio is multiplication value among SYSDIV bit, HPMDIV bit, and EXTBUSDIV bit setting.

For example, setting SYSDIV to 1-division, HPMDIV to 7-division, EXTBUSDIV to 1-division, dH is calculated as 0.429.

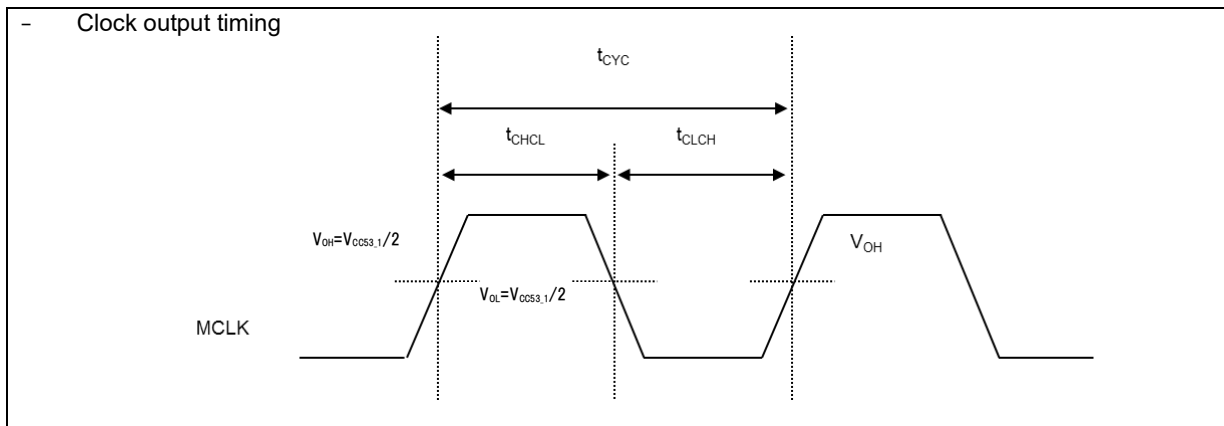
*2: If division-ratio is even value, dL is equivalent to 0.5.

Otherwise, dL is calculated as the following.

$dL = \text{The number rounding "division-ratio} \times 0.5"$ up to the nearest integer / division-ratio

division-ratio is multiplication value among SYSDIV bit, HPMDIV bit and EXTBUSDIV bit setting.

For example, setting SYSDIV to 1-division, HPMDIV to 7-division, EXTBUSDIV to 1-division, dL is calculated as 0.571.



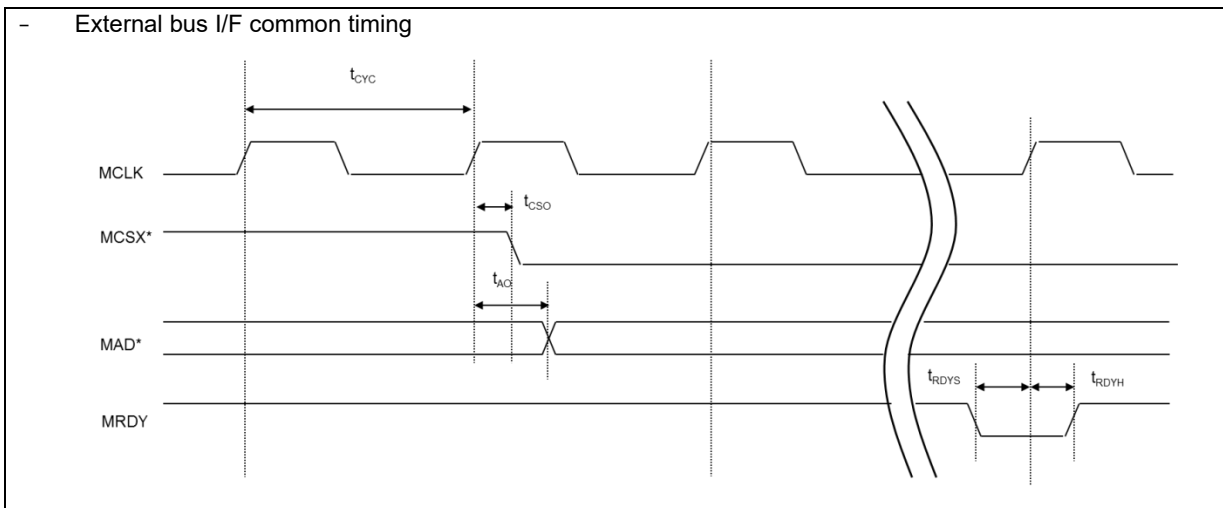
7.4.14.2 Common Timing between Read and Write

(TA: Recommended operating conditions, $V_{cc53_1} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---------------------------|------------|----------------------|---|-------|-------|------|--|
| | | | | Min | Max | | |
| Cycle time (without MRDY) | t_{CYC} | MCLK | $(C_L = 20\text{ pF}$, $I_{OH} = -5\text{ mA}$, $I_{OL} = 5\text{ mA})$ | 25 | - | ns | |
| Cycle time (with MRDY) | t_{CYC} | MCLK | | 40 | - | ns | If using MRDY, set MCLK to 25 MHz or less. |
| CS delay time | t_{CSO} | MCLK, MCSX0 to MCSX3 | | 0.5 | 11.25 | ns | |
| Address delay time | t_{AO} | MCLK, MAD0 to MAD21 | | 0.5 | 11.25 | ns | |
| RDY setup time | t_{RDYS} | MCLK, MRDY | "CMOS hysteresis input" and "Disable noise filter" are selected. | 21 | - | ns | |
| RDY hold time | t_{RDYH} | MCLK, MRDY | | 0 | - | ns | |

(TA: Recommended operating conditions, $V_{cc53_1} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|---------------------------|------------|----------------------|---|-------|-----|------|--|
| | | | | Min | Max | | |
| Cycle time (without MRDY) | t_{CYC} | MCLK | $(C_L = 20\text{ pF}$, $I_{OH} = -2\text{ mA}$, $I_{OL} = 2\text{ mA})$ | 31.25 | - | ns | |
| Cycle time (with MRDY) | t_{CYC} | MCLK | | 40 | - | ns | If using MRDY, set MCLK to 25 MHz or less. |
| CS delay time | t_{CSO} | MCLK, MCSX0 to MCSX3 | | 0.5 | 18 | ns | |
| Address delay time | t_{AO} | MCLK, MAD0 to MAD21 | | 0.5 | 18 | ns | |
| RDY setup time | t_{RDYS} | MCLK, MRDY | "CMOS hysteresis input" and "Disable noise filter" are selected. | 21 | - | ns | |
| RDY hold time | t_{RDYH} | MCLK, MRDY | | 0 | - | ns | |



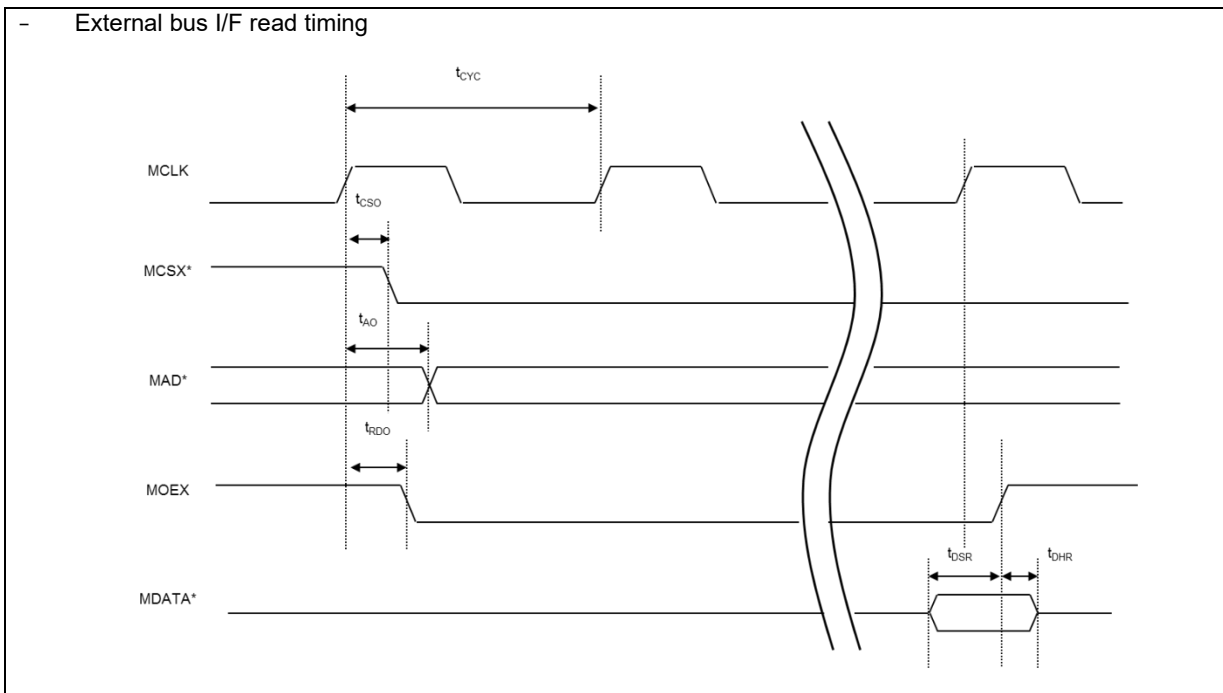
7.4.14.3 Read Timing

(TA: Recommended operating conditions, $V_{cc53_1} = 5.0\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-----------------|-----------|-------------------------|---|-------------------|-------|------|---------|
| | | | | Min | Max | | |
| Data setup time | t_{DSR} | MOEX, MDATA0 to MDATA15 | "CMOS hysteresis input" and "Disable noise filter" are selected. | $13.12 + t_{CYC}$ | - | ns | |
| Data hold time | t_{DHR} | MOEX, MDATA0 to MDATA15 | | 0 | - | ns | |
| MOEX delay time | t_{RDO} | MCLK, MOEX | ($C_L = 20\text{ pF}$, $I_{OH} = -5\text{ mA}$, $I_{OL} = 5\text{ mA}$) | 0.5 | 11.25 | ns | |

(TA: Recommended operating conditions, $V_{cc53_1} = 3.3\text{ V} \pm 10\%$, $V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-----------------|-----------|-------------------------|---|----------------|-----|------|---------|
| | | | | Min | Max | | |
| Data setup time | t_{DSR} | MOEX, MDATA0 to MDATA15 | "CMOS hysteresis input" and "Disable noise filter" are selected. | $21 + t_{CYC}$ | - | ns | |
| Data hold time | t_{DHR} | MOEX, MDATA0 to MDATA15 | | 0 | - | ns | |
| MOEX delay time | t_{RDO} | MCLK, MOEX | ($C_L = 20\text{ pF}$, $I_{OH} = -2\text{ mA}$, $I_{OL} = 2\text{ mA}$) | 0.5 | 18 | ns | |



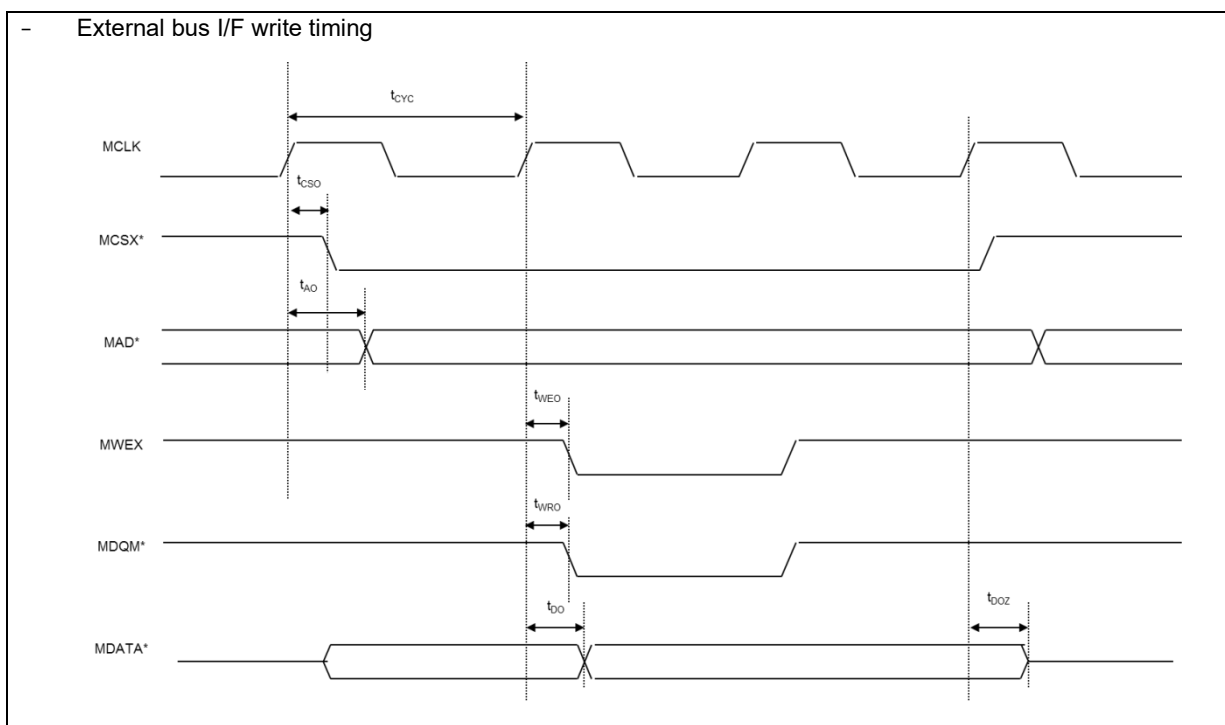
7.4.14.4 Write Timing

(T_A: Recommended operating conditions, V_{cc53_1} = 5.0 V ±10 %, V_{SS} = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------------------|------------------|------------------------|---|-------|-------|------|---------|
| | | | | Min | Max | | |
| MWEX delay time | t _{WEO} | MCLK, MWEX | (C _L = 20 pF, I _{OH} = -5 mA, I _{OL} = 5 mA) | 0.5 | 11.25 | ns | |
| Byte mask delay time | t _{WRO} | MCLK, MDQM0, MDQM1 | | 0.5 | 11.25 | ns | |
| Data delay time | t _{DO} | MCLK, MDATA0 to MDAT15 | | 0.5 | 11.25 | ns | |
| Data delay time (Hi-Z output) | t _{DOZ} | MCLK, MDATA0 to MDAT15 | | - | 11.25 | ns | |

(T_A: Recommended operating conditions, V_{cc53_1} = 3.3 V ±10 %, V_{SS} = 0.0 V)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------------------|------------------|------------------------|---|-------|-----|------|---------|
| | | | | Min | Max | | |
| MWEX delay time | t _{WEO} | MCLK, MWEX | (C _L = 20 pF, I _{OH} = -2 mA, I _{OL} = 2 mA) | 0.5 | 18 | ns | |
| Byte mask delay time | t _{WRO} | MCLK, MDQM0, MDQM1 | | 0.5 | 18 | ns | |
| Data delay time | t _{DO} | MCLK, MDATA0 to MDAT15 | | 0.5 | 18 | ns | |
| Data delay time (Hi-Z output) | t _{DOZ} | MCLK, MDATA0 to MDAT15 | | - | 18 | ns | |



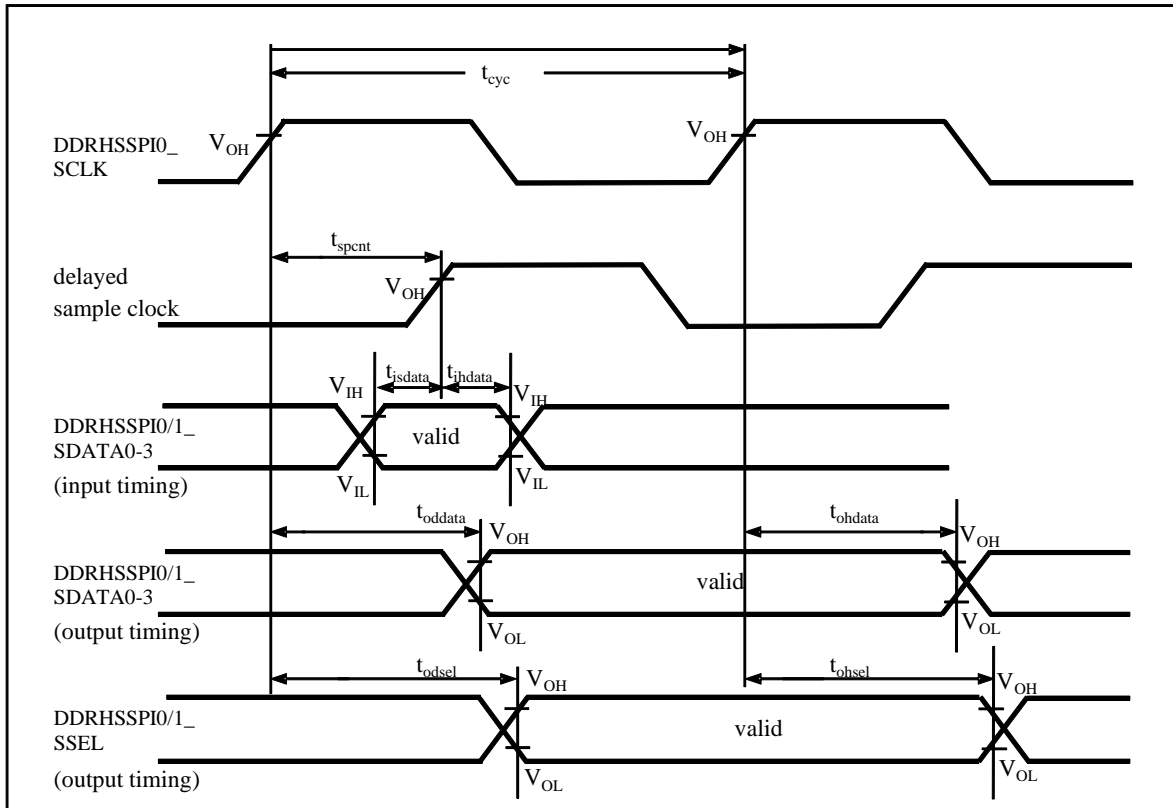
7.4.15 DDR-HSSPI

(1) DDR-HSSPI Interface Timing (SDR Mode)

(TA: Recommended operating conditions, $V_{CC53_2} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|--|--------------|--|---|------------------------------------|--------------------|------|---------|
| | | | | Min | Max | | |
| HSSPI clock cycle | t_{cyc} | DDRHSSPI0_SCLK | | 14.3 | - | ns | |
| DDRHSSPI_SCLK \uparrow → delayed sample clock \uparrow | t_{spcnt} | - | | 0 | 31.5 | ns | |
| DDRHSSPI_SDATA →DDRHSSPI_SCLK \uparrow input setup time | t_{isdata} | DDRHSSPI0_SDATA0-3 DDRHSSPI1_SDATA0-3 | | *1 | - | ns | |
| DDRHSSPI_SCLK \uparrow → DDRHSSPI_SDATA input hold time | t_{ihdata} | DDRHSSPI0_SDATA0-3 DDRHSSPI1_SDATA0-3 | ($C_L = 20\text{ pF}$, $I_{OH} = -15\text{ mA}$, $I_{OL} = 15\text{ mA}$) | *1 | - | ns | |
| DDRHSSPI_SCLK \uparrow → DDRHSSPI_SDATA output delay time | t_{oddata} | DDRHSSPI0_SDATA0-3 DDRHSSPI1_SDATA0-3 | or | - | $t_{cyc}/2 + 4.15$ | ns | |
| DDRHSSPI_SCLK \uparrow → DDRHSSPI_SDATA output hold time | t_{ohdata} | DDRHSSPI0_SDATA0-3 DDRHSSPI1_SDATA0-3 | ($C_L = 20\text{ pF}$, $I_{OH} = -5\text{ mA}$, $I_{OL} = 5\text{ mA}$) | $t_{cyc}/2 - 5.15$ | - | ns | |
| DDRHSSPI_SSEL \downarrow → DDRHSSPI_SCLK output delay time | t_{odsel} | DDRHSSPI0_SSEL DDRHSSPI1_SSEL | | $-18.45 + (SS2CD + 0.5) * t_{cyc}$ | - | ns | |
| DDRHSSPI_SCLK \uparrow → DDRHSSPI_SSEL output hold time | t_{ohsel} | DDRHSSPI0_SSEL DDRHSSPI1_SSEL | | $t_{cyc} - 4.15$ | - | ns | |

- SS2CD [1:0] should be configured as 11 (binary number).
- For *1, the delay of the delay sample clock can be configured (DLP function).

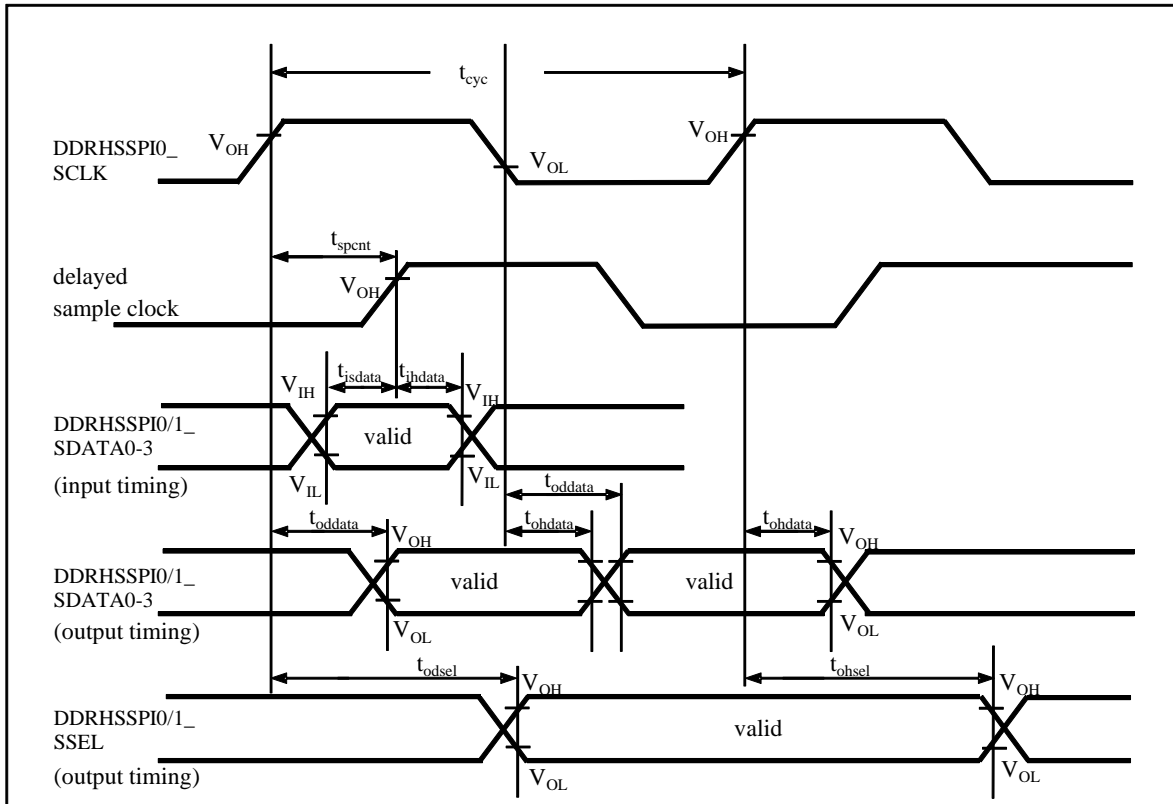


(2) DDR-HSSPI Interface Timing (DDR Mode)

 (TA: Recommended operating conditions, $V_{CC53_2} = 3.3\text{ V} \pm 0.3\text{ V}$, $V_{SS} = 0.0\text{ V}$)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|--|--------------|--|--|---|--------------------|------|---------|
| | | | | Min | Max | | |
| HSSPI clock cycle | t_{cyc} | DDRHSSPI0_SCLK | (C _L = 20 pF, I _{OH} = -15 mA, I _{OL} = 15 mA) or (C _L = 20 pF, I _{OH} = -5 mA, I _{OL} = 5 mA) | 14.3 | - | ns | |
| DDRHSSPI_SCLK↓ →delayed sample clock↑ | t_{spcnt} | - | | 0 | 31.5 | ns | |
| DDRHSSPI_SDATA→ DDRHSSPI_SCLK↓ input setup time | t_{isdata} | DDRHSSPI0_SDATA0-3 DDRHSSPI1_SDATA0-3 | | *1 | - | ns | |
| DDRHSSPI_SCLK↓ →DDRHSSPI_SDATA input hold time | t_{ihdata} | DDRHSSPI0_SDATA0-3 DDRHSSPI1_SDATA0-3 | | *1 | - | ns | |
| DDRHSSPI_SCLK↑ →DDRHSSPI_SDATA output delay time | t_{oddata} | DDRHSSPI0_SDATA0-3 DDRHSSPI1_SDATA0-3 | | - | $t_{cyc}/4 + 1.95$ | ns | |
| DDRHSSPI_SCLK↓ →DDRHSSPI_SDATA output hold time | t_{ohdata} | DDRHSSPI0_SDATA0-3 DDRHSSPI1_SDATA0-3 | | $t_{cyc}/4 - 2.0$ | - | ns | |
| DDRHSSPI_SSEL↓→ DDRHSSPI_SCLK output delay time | t_{odsel} | DDRHSSPI0_SSEL DDRHSSPI1_SSEL | | -18.45 + (SS2CD + 0.5) * t_{cyc} | - | ns | |
| DDRHSSPI_SCLK↑→ DDRHSSPI_SSEL output hold time | t_{ohsel} | DDRHSSPI0_SSEL DDRHSSPI1_SSEL | | 0.75 * $t_{cyc} - 2.45$ | - | ns | |

- SS2CD [1:0] should be configured as 11 (binary number).
- For *1, the delay of the delay sample clock can be configured (DLP function)



7.4.16 Port Noise Filter

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|----------------------|--------|----------|------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| Input pulse filtered | - | ALL GPIO | - | - | 17 | ns | *1 |

*1: Input pulse is filtered up to 17 ns when port noise filter is enabled. Filtering of input pulse more than 17 ns is not guaranteed.

7.4.17 Clock Monitor

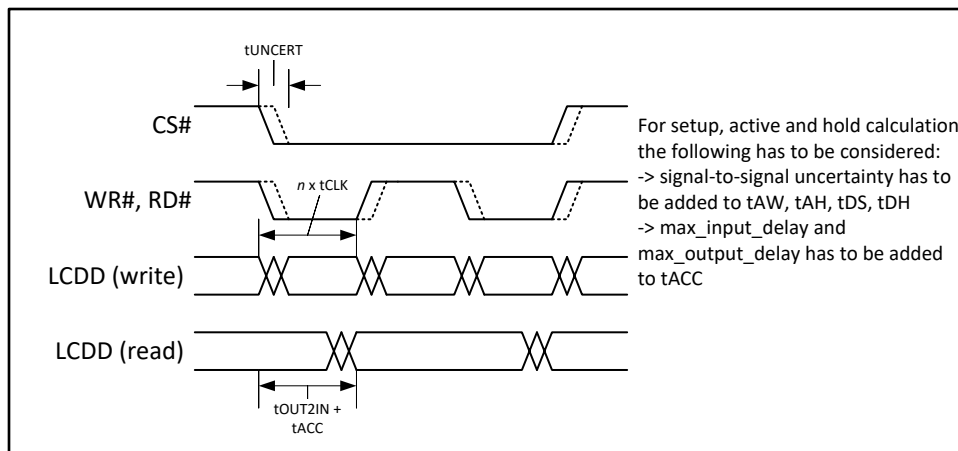
(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|-------------------------|--------|--------------------------|------------|-------|-----|------|---------|
| | | | | Min | Max | | |
| Clock monitor frequency | - | SYSC0_CLK_0, SYSC0_CLK_1 | - | - | 10 | MHz | |

7.4.18 LCD Bus I/F

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|------------------------------|--------------|-----------------|--|-------|------|------|---------|
| | | | | Min | Max | | |
| Clock cycle time | t_{CLK} | WR#, RD# | (C _L = 20 pF, I _{OH} = -5 mA, I _{OL} = 5 mA), | 25 | - | ns | |
| Signal-to-Signal uncertainty | t_{UNCERT} | CS# | | - | 5.0 | ns | |
| Output to input duration | t_{OUT2IN} | LCDD0 to LCDD17 | | - | 28.0 | ns | |



Note:

- To calculate interface timing, see the LCD controller specification of the external display for the required AC characteristics and S6J3360/S6J3370 Series hardware manual.

7.4.19 I2S

7.4.19.1 I2S Timing – Master Mode (MSMD = 1)

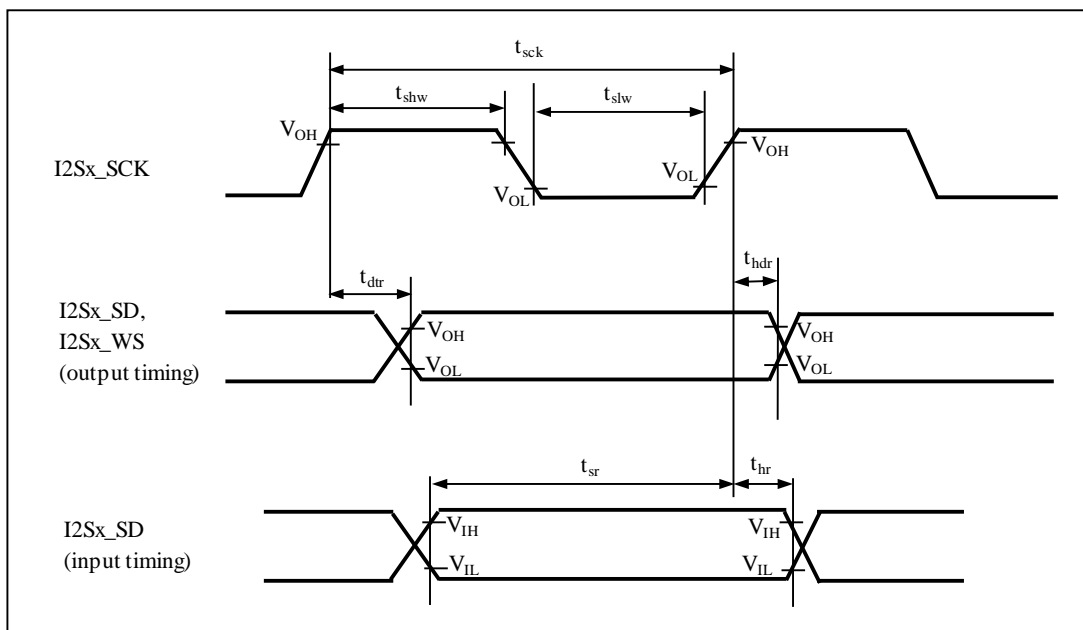
(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|--|-----------|---|---|-----------------------|--------------------|------|---|
| | | | | Min | Max | | |
| ECLK0/ECLK1 clock cycle | t_{eck} | | | 20 | - | ns | Only relevant if external ECLK input is selected. *1 |
| ECLK0/ECLK1 clock "H" pulse width | t_{ehw} | I2S0_ECLK_0/1 I2S1_ECLK_0 | | 0.40* t_{eck} | 0.60* t_{eck} | ns | |
| ECLK0/ECLK1 clock "L" pulse width | t_{elw} | | | 0.40* t_{eck} | 0.60* t_{eck} | ns | |
| I2S clock cycle (output SCK) | t_{sck} | | | 100 | - | ns | |
| I2S clock "H" pulse width | t_{shw} | I2S0_SCK_0/1, I2S1_SCK_0 | (C _L = 20 pF, I _{OH} = -5 mA, I _{OL} = 5 mA) | 0.35* t_{sck} | 0.65* t_{sck} | ns | |
| I2S clock "L" pulse width | t_{slw} | | | 0.35* t_{sck} | 0.65* t_{sck} | ns | |
| Sender delay time SCK↑ -> SD/WS valid | t_{dtr} | I2S0_SCK_0/1, I2S1_SCK_0, I2S0_SD_0/1, I2S1_SD_0, I2S0_WS_0/1, I2S1_WS_0 | | CPOL = 0, SMPL = 1 | - | 26 | ns |
| Sender hold time SCK↑ -> SD/WS invalid | t_{htr} | | | -10 | - | ns | *2 |
| Receiver setup time SD valid -> SCK↑ | t_{sr} | I2S0_SCK_0/1, I2S1_SCK_0, I2S0_SD_0/1, I2S1_SD_0 | | 40 | - | ns | *2 |
| Receiver hold time SCK↑ -> SD valid | t_{hr} | | | 10 | - | ns | *2 |

Notes:

*1: ECKM = 1. See the Resource Input Configuration chapter in TRM for required RESSEL register settings.

*2: See the I2S register description chapter in TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay values as per above table will remain the same.



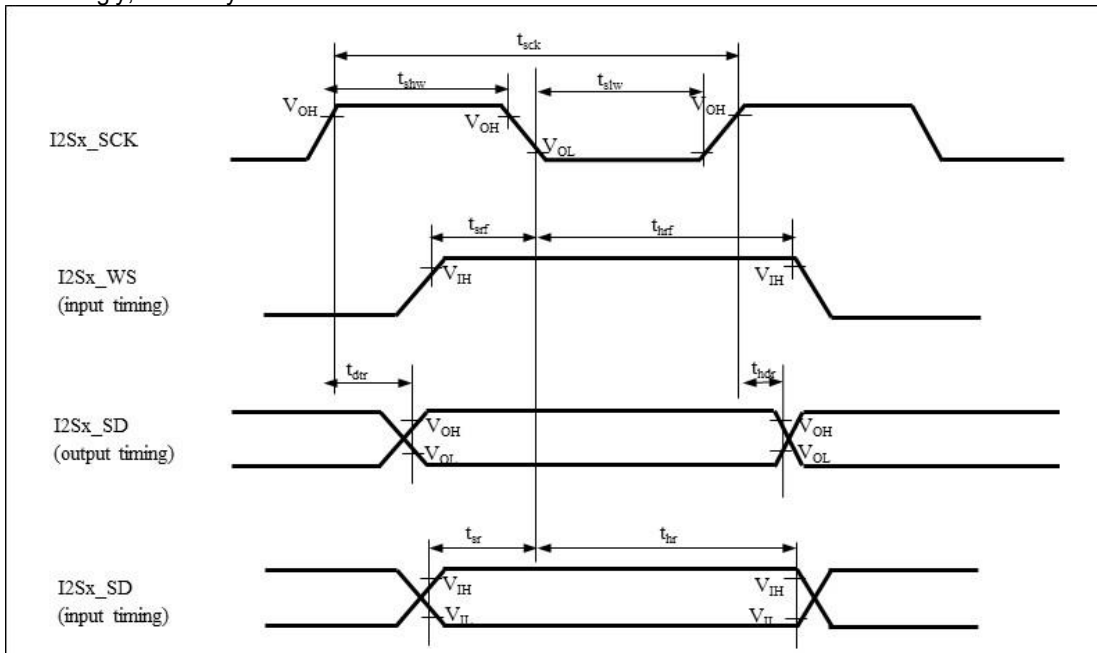
7.4.19.2 I2S Timing – Slave Mode (MSMD = 0)

(Condition: See section 7.2 Recommended Operating Conditions)

| Parameter | Symbol | Pin Name | Conditions | Value | | Unit | Remarks |
|--------------------------------------|-----------|---|--|----------------------|----------------------|------|---------|
| | | | | Min | Max | | |
| I2S clock cycle (input SCK) | t_{sck} | I2S0_SCK_0/1, I2S1_SCK_0 | (C _L = 20 pF, I _{OH} = -5 mA, I _{OL} = 5 mA) CPOL = 0, SMPL = 0 | 100 | - | ns | |
| I2S clock "H" pulse width | t_{shw} | I2S0_SCK_0/1, I2S1_SCK_0 | | $0.40 \cdot t_{sck}$ | $0.60 \cdot t_{sck}$ | ns | |
| I2S clock "L" pulse width | t_{slw} | | | $0.40 \cdot t_{sck}$ | $0.60 \cdot t_{sck}$ | ns | |
| Setup time WS transition -> SCK↓ | t_{srf} | I2S0_SCK_0/1, I2S1_SCK_0, I2S0_WS_0/1, I2S1_WS_0 | | 40 | - | ns | *1 |
| Hold time SCK↓ -> WS transition | t_{hrf} | | | 10 | - | ns | *1 |
| Sender delay time SCK↑ -> SD valid | t_{dtr} | I2S0_SCK_0/1, I2S1_SCK_0, I2S0_SD_0/1, I2S1_SD_0 | | - | 31 | ns | *1 |
| Sender hold time SCK↑ -> SD invalid | t_{htr} | | | -10 | - | ns | *1 |
| Receiver setup time SD valid -> SCK↓ | t_{sr} | I2S0_SCK_0/1, I2S1_SCK_0, I2S0_SD_0/1, I2S1_SD_0 | | 21 | - | ns | *1 |
| Receiver hold time SCK↓ -> SD valid | t_{hr} | | 10 | - | ns | *1 | |

Notes:

*1: See the I2S register description chapter in the TRM for different combinations of clock polarity (CPOL), sampling point position (SMPL), polarity/pulse_width/frame_sync phase of WS (FSPL, FSLN, FSPH). Actual waveforms and relevant clock edges will change accordingly; the delay values based on the table above will remain the same.



7.5 A/D Converter

7.5.1 Electrical Characteristics

(T_A: Recommended operating conditions, V_{CC} = AV_{CC5} = 5.0 V ± 0.5 V, V_{SS} = AV_{SS} = 0.0 V)

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|-------------------------------|------------------|--|----------------|-----|----------------|------|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 12 | bit | |
| Total error | - | - | - | - | ±6 | LSB | *3 |
| | - | - | - | - | ±12 | LSB | *4 |
| Integral Non linearity | - | - | - | - | ±4.0 | LSB | *5 |
| Differential Non linearity | - | - | - | - | ±1.9 | LSB | *5 |
| Zero transition voltage | V _{ZT} | ADC0_AN0 to ADC0_AN47 | AVRL - 11.5LSB | - | AVRL + 12.5LSB | V | *4 |
| Full-scale transition voltage | V _{FST} | ADC0_AN0 to ADC0_AN47 | AVRH - 13.5LSB | - | AVRH + 10.5LSB | V | *4 |
| Sampling time | t _{SMP} | - | 0.8 | - | - | µs | *1 |
| Compare time | t _{CMP} | - | 0.7 | - | 26 | µs | *1 |
| A/D conversion time | t _{CNV} | - | 1.5 | - | - | µs | *1 |
| Resumption time | - | - | - | - | 1 | µs | |
| Analog port input current | I _{AIN} | ADC0_AN0 to ADC0_AN2, ADC0_AN24 to ADC0_AN47 | -2 | - | 2 | µA | AV _{SS} ≤ V _{AIN} ≤ AV _{CC5} |
| | | ADC0_AN3 to ADC0_AN23 | -1 | - | 1 | | |
| Analog input voltage | V _{AIN} | ADC0_AN0 to ADC0_AN47 | AVRL | - | AVRH | V | |
| Analog input capacitance | C _{VIN} | ADC0_AN0 to ADC0_AN47 | - | - | 18 | pF | |
| Analog input resistance | R _{VIN} | ADC0_AN0 to ADC0_AN47 | - | - | 4.5 | kΩ | |
| Reference voltage | AVRH | AVRH5 | 4.5 | - | 5.5 | V | AV _{CC5} ≥ AVRH |
| | AVRL | AVRL5/AVSS | - | 0.0 | - | V | |
| Power supply current | I _A | AVCC5 | - | 600 | 700 | µA | |
| | I _{AH} | AVCC5 | - | 1.0 | 100 | µA | *2 |
| | I _R | AVRH5 | - | 0.7 | 1.95 | mA | |
| | I _{RH} | AVRH5 | - | - | 5.0 | µA | *2 |
| Variation between channels | - | ADC0_AN0 to ADC0_AN47 | - | - | 4.0 | LSB | |

*1: Time per channel

*2: Definition of the power supply current (when V_{CC5} = AV_{CC5} = 5.0 V) while the A/D converter is not operating and in stop mode.

*3: Total error is a comprehensive static error that includes the linearity after trimming by software. 1 LSB = (AVRH - AVRL)/4096

*4: 1 LSB = (AVRH - AVRL)/4096

*5: 1 LSB = (VFST - VZT)/4094

(T_A: Recommended operating conditions, V_{CC} = AV_{CC5} = 3.3 V ± 0.3 V, V_{SS} = AV_{SS} = 0.0 V)

| Parameter | Symbol | Pin Name | Value | | | Unit | Remarks |
|-------------------------------|------------------|---|-------------------|-----|-------------------|------|---|
| | | | Min | Typ | Max | | |
| Resolution | - | - | - | - | 12 | bit | |
| Total error | - | - | - | - | ±6 | LSB | *3 |
| Integral Non linearity | - | - | - | - | ±4.0 | LSB | *5 |
| Differential Non linearity | - | - | - | - | ±1.9 | LSB | *5 |
| Zero transition voltage | V _{ZT} | ADC0_AN0 to ADC0_AN47 | AVRL - 14.5LSB | - | AVRL + 15.5LSB | V | *4 |
| Full-scale transition voltage | V _{FST} | ADC0_AN0 to ADC0_AN47 | AVRH - 16.5LSB | - | AVRH + 13.5LSB | V | *4 |
| Sampling time | t _{SMP} | - | 1.0 | - | - | µs | *1 |
| Compare time | t _{CMP} | - | 1.4 | - | 26 | µs | *1 |
| A/D conversion time | t _{CNV} | - | 2.4 | - | - | µs | *1 |
| Resumption time | - | - | - | - | 1 | µs | |
| Analog port input current | I _{AIN} | ADC0_AN0 to ADC0_AN2, ADC0_AN24 to ADC0_AN47 | -2 | - | 2 | µA | AV _{SS} ≤ V _{AIN} ≤ AV _{CC5} |
| | | ADC0_AN3 to ADC0_AN23 | -1 | - | 1 | | |
| Analog input voltage | V _{AIN} | ADC0_AN0 to ADC0_AN47 | AVRL | - | AVRH | V | |
| Analog input capacitance | C _{VIN} | ADC0_AN0 to ADC0_AN47 | - | - | 18 | pF | |
| Analog input resistance | R _{VIN} | ADC0_AN0 to ADC0_AN47 | - | - | 6 | kΩ | |
| Reference voltage | AVRH | AVRH5 | 3 | - | 3.6 | V | AV _{CC5} ≥ AVRH |
| | AVRL | AVRL5/AVSS | - | 0.0 | - | V | |
| Power supply current | I _A | AVCC5 | - | 600 | 700 | µA | |
| | I _{AH} | AVCC5 | - | 1.0 | 100 | µA | *2 |
| | I _R | AVRH5 | - | 0.5 | 1.3 | mA | |
| | I _{RH} | AVRH5 | - | - | 7.0 | µA | *2 |
| Variation between channels | - | ADC0_AN0 to ADC0_AN47 | - | - | 4.0 | LSB | |

*1: Time per channel

*2: Definition of the power supply current (when V_{CC5} = AV_{CC5} = 3.3 V) while the A/D converter is not operating and in stop mode.

*3: Total error is a comprehensive static error that includes the linearity after trimming by software. 1 LSB = (AVRH - AVRL)/4096

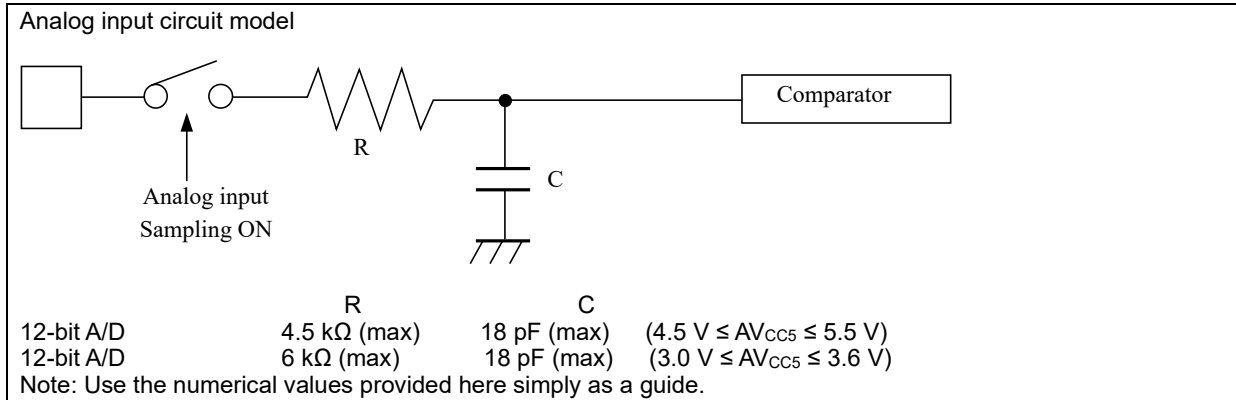
*4: 1 LSB = (AVRH - AVRL)/4096

*5: 1 LSB = (VFST - VZT)/4094

7.5.2 Notes on A/D Converters

Output Impedance of an External Circuit for Analog Input

When the external impedance is too high, the analog voltage sampling time may become insufficient. In this case, we recommend attaching a capacitor (about 0.1 μF) to an analog input pin.



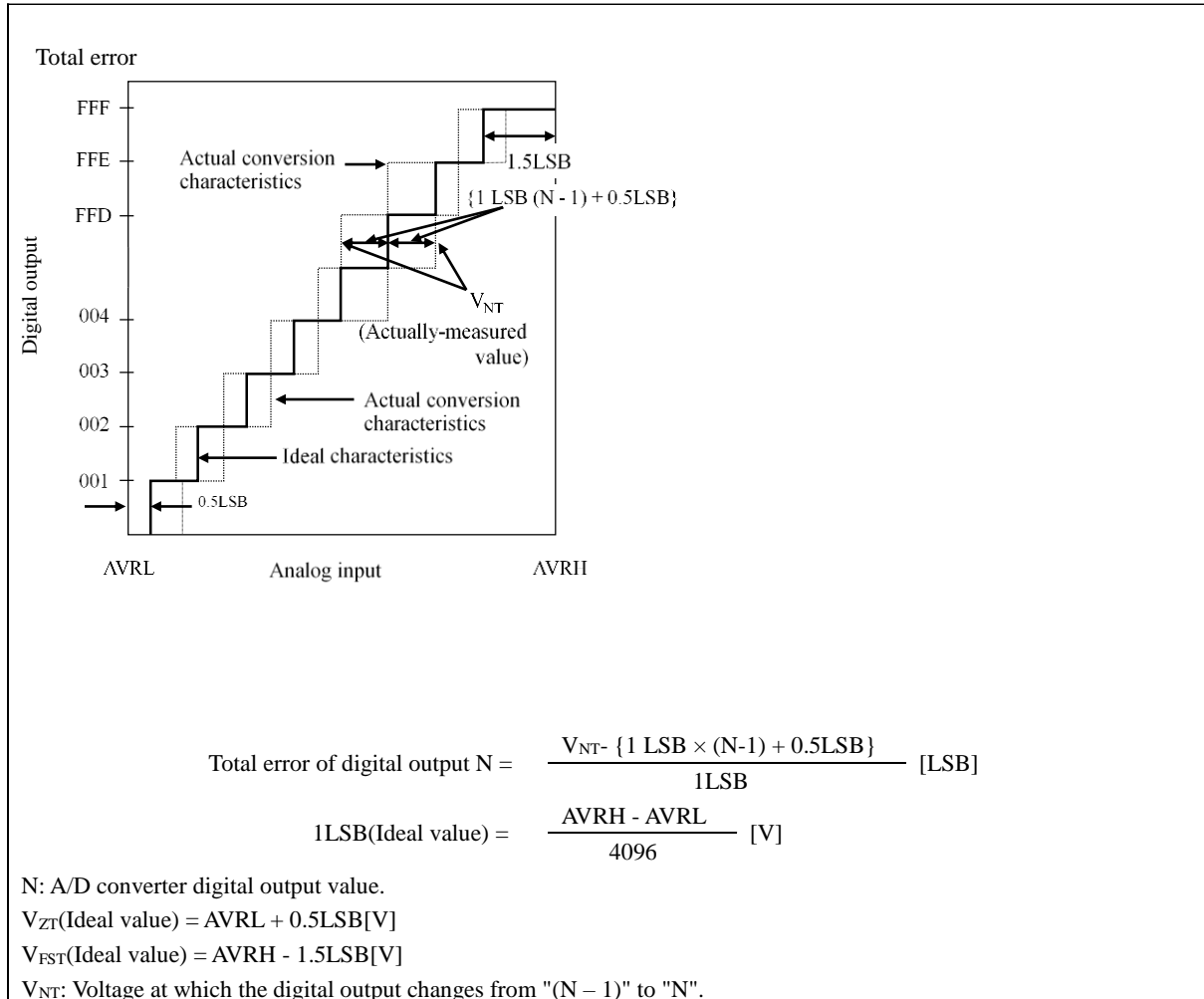
7.5.3 Glossary

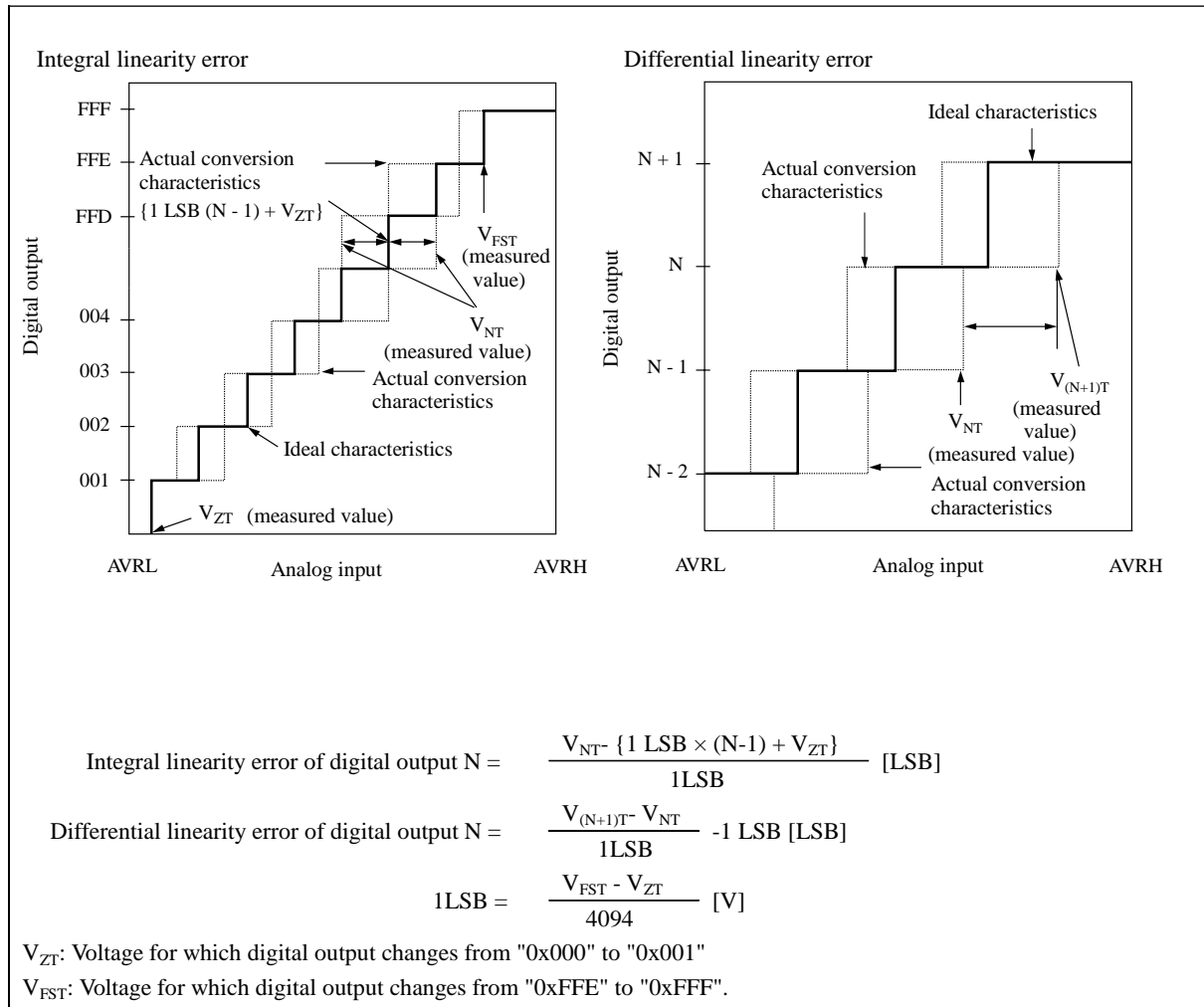
Resolution: Analog change that can be identified by an A/D converter.

Integral linearity error: Deviation of the straight line connecting the zero transition point ("0000 0000 0000" <--> "0000 0000 0001") and full-scale transition point ("1111 1111 1110" <--> "1111 1111 1111") from actual conversion characteristics includes zero transition error, full-scale transition error, and non-linearity error.

Differential linearity error: Deviation from the ideal value of the input voltage required for changing the output code by 1 LSB.

Total error: Difference between the actual value and the theoretical value.





7.6 Flash Memory

7.6.1 Electrical Characteristics

| Parameter | Value | | | Unit | Remarks |
|--|--|-----|-----|------|---|
| | Min | Typ | Max | | |
| Sector erase time | - | 120 | 180 | ms | Large sector ^{*1} Internal preprogramming time included |
| | - | 120 | 180 | ms | 8 kB sector ^{*1} Internal preprogramming time included |
| | - | 120 | 180 | ms | 4 kB sector ^{*2} Internal preprogramming time included |
| 32-bit write time (Program) | - | 30 | 60 | μs | System-level overhead time excluded ^{*1} |
| 64-bit write time (Program) | - | 30 | 60 | μs | System-level overhead time excluded ^{*1} |
| 256-bit write time (Program) | - | 40 | 70 | μs | System-level overhead time excluded ^{*1} |
| 32-bit write time (Work) | - | 30 | 60 | μs | System-level overhead time excluded ^{*2} |
| Erase count / Data retention time (Program) | 1,000/20 years | - | - | - | Temperature at write/erase time. Average temperature T _A = +85 °C |
| Erase count / Data retention time (Work) | 1,000/20 years 10,000/10 years 100,000/5 years | - | - | - | Temperature at write/erase time. Average temperature T _A = +85 °C |

*1: Guaranteed value for up to 1,000 erases

*2: Guaranteed value for up to 100,000 erases

7.6.2 Notes

While the flash memory is written or erased, shutdown of the external power (V_{CC5}) is prohibited.

In application systems, where V_{CC5} may be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.

In other words, after the external power supply voltage falls below the detection voltage (V_{DL}), hold V_{CC5} at 2.7 V or more within the duration calculated by the following expression:

$$T_d^{*1} [\mu s] + (1 / F_{CRF}^{*2} [MHz]) \times 1029 + 25 [\mu s]$$

*1: See [Low Voltage Detection \(External Voltage\)](#)

*2: See [Source Clock Timing](#)

8. Ordering Information

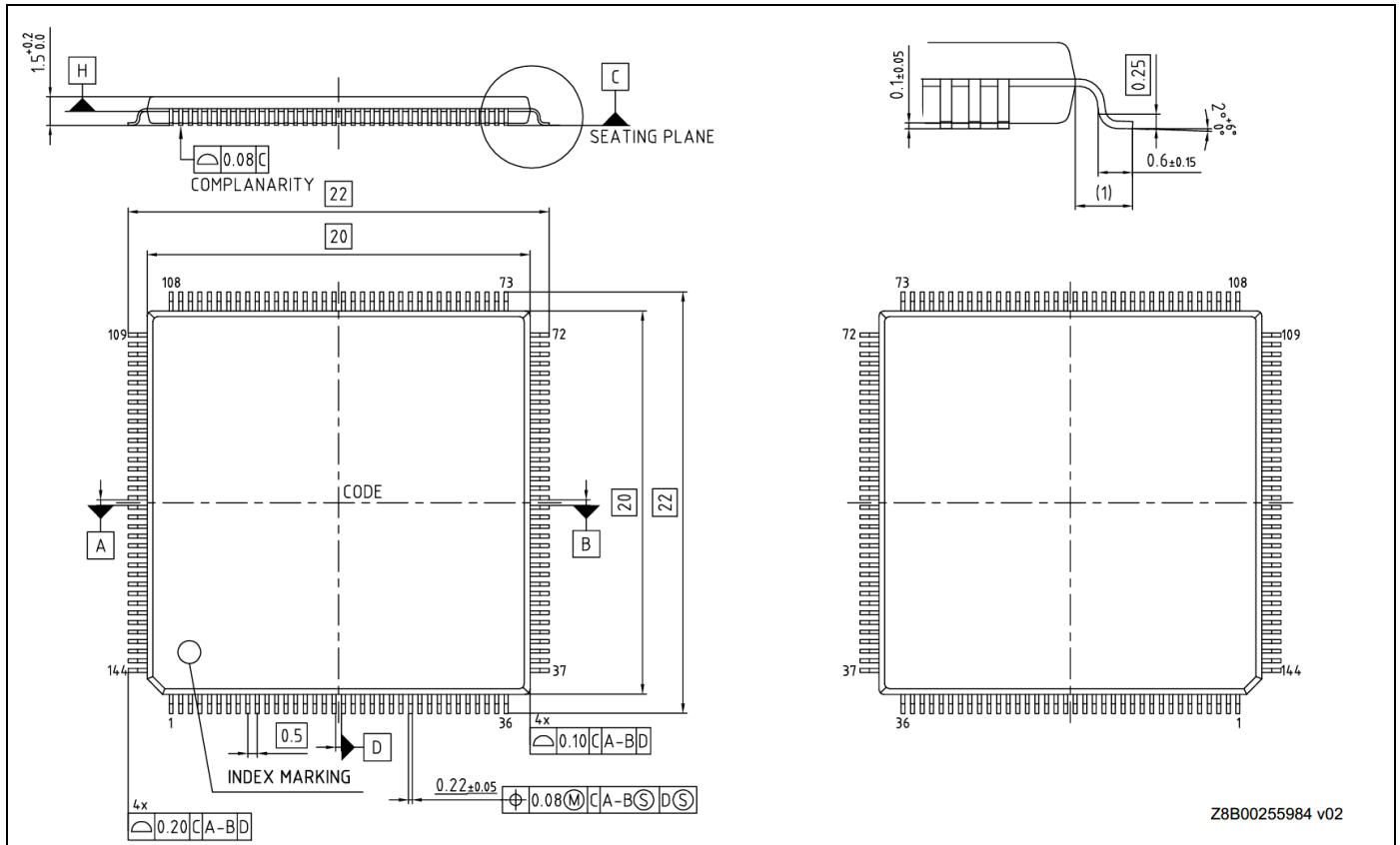
| Part Number | Package |
|-------------------|--|
| S6J336CHSBSV20000 | LQS144 (144-pin 0.5-mm pitch plastic LQFP) |
| S6J336AHSBSL20000 | LQN144 (144-pin 0.4-mm pitch plastic LQFP) |
| S6J336CHSBSL20000 | LQN144 (144-pin 0.4-mm pitch plastic LQFP) |
| S6J336AJABSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J336AJEBSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J336AJSBSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J336AJTBSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CJABSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CJEBSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CJSBSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CJTBSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J337BJSBSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J337CJSBSE20000 | LEF176 (176-pin 0.5-mm pitch plastic TEQFP) |
| S6J336AHABSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J336AHEBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J336AHSBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J336AHTBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CHABSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CHEBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CHSBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CHTBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J336CHTBSE2D000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J337AHTBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |
| S6J337AHUBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) |

| Part Number | Package |
|-------------------|--|
| S6J336AHABSC20000 | LEG144 (144-pin 0.4-mm pitch plastic TEQFP) |
| S6J336AHEBSC20000 | LEG144 (144-pin 0.4-mm pitch plastic TEQFP) |
| S6J336AHSBSC20000 | LEG144 (144-pin 0.4-mm pitch plastic TEQFP) |
| S6J336AHTBSC20000 | LEG144 (144-pin 0.4-mm pitch plastic TEQFP) |
| S6J336CHABSC20000 | LEG144 (144-pin 0.4-mm pitch plastic TEQFP) |
| S6J336CHEBSC20000 | LEG144 (144-pin 0.4-mm pitch plastic TEQFP) |
| S6J336CHSBSC20000 | LEG144 (144-pin 0.4-mm pitch plastic TEQFP) |
| S6J336CHTBSC20000 | LEG144 (144-pin 0.4-mm pitch plastic TEQFP) |

9. Package Dimensions

9.1 LQFP144 (0.5 mm)

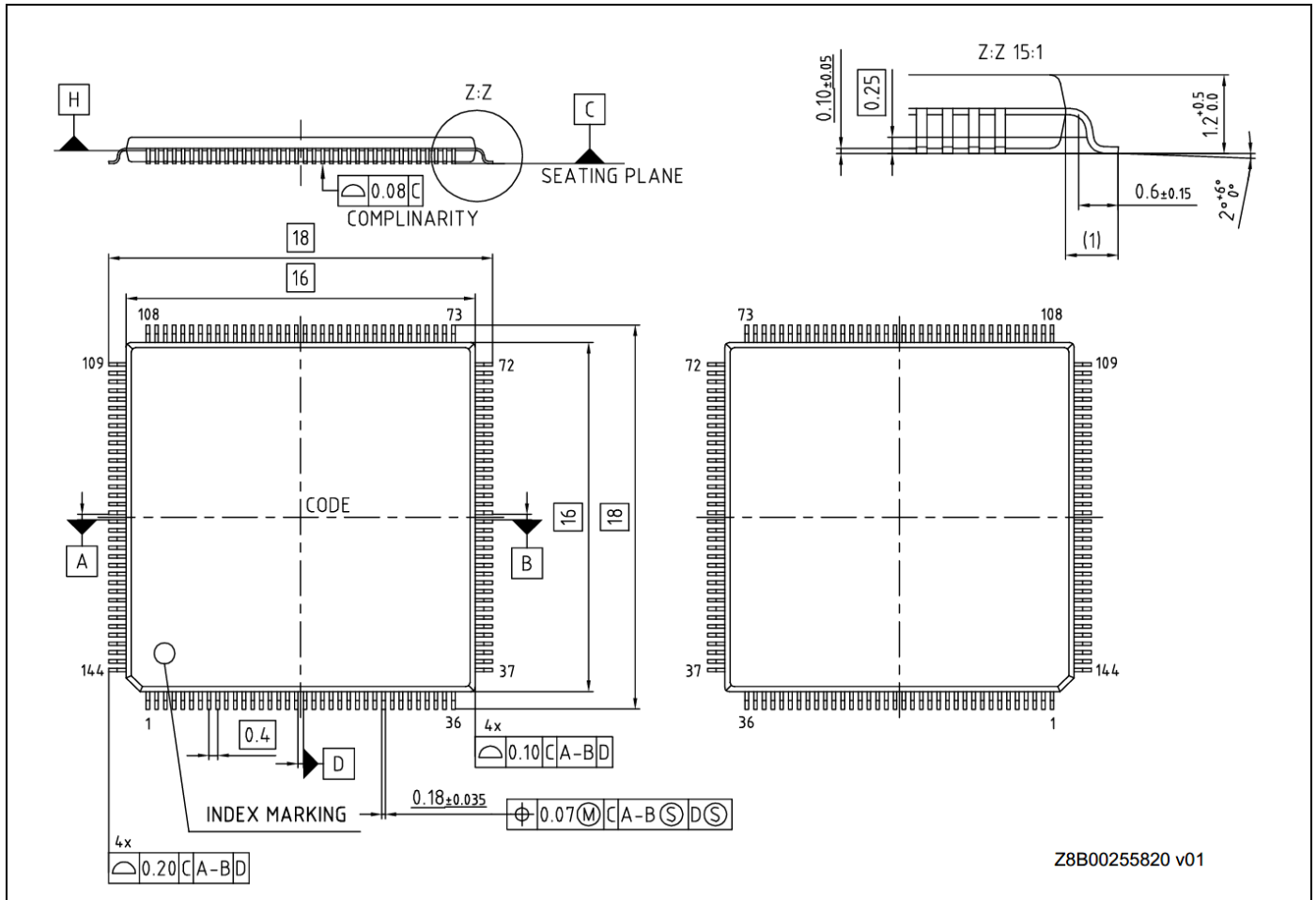
| Package Type | Package Code |
|--------------|--------------|
| LQFP 144 | LQS 144 |



Z8B00255984 v02

9.2 LQFP144 (0.4 mm)

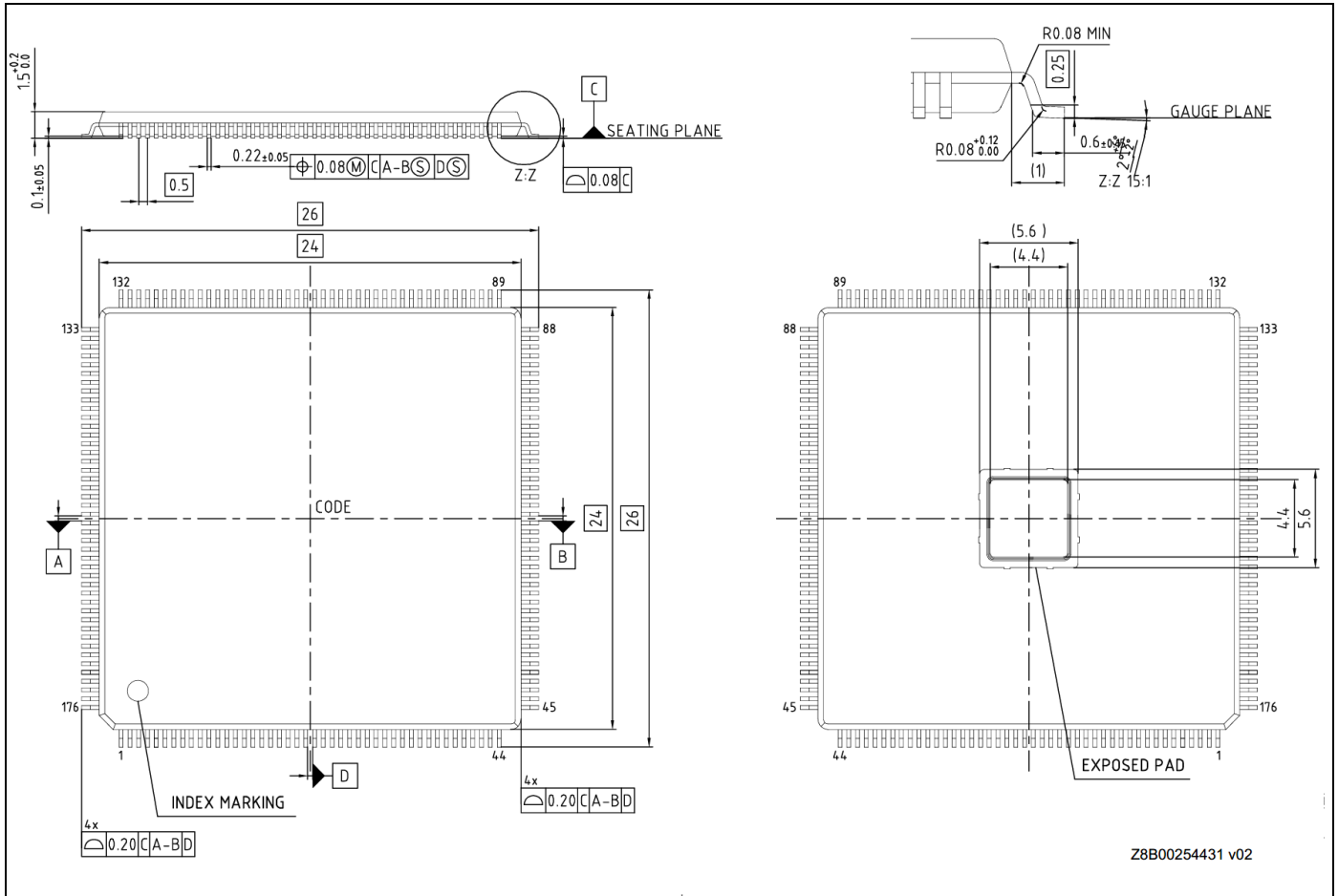
| Package Type | Package Code |
|--------------|--------------|
| LQFP 144 | LQN 144 |



Z8B00255820 v01

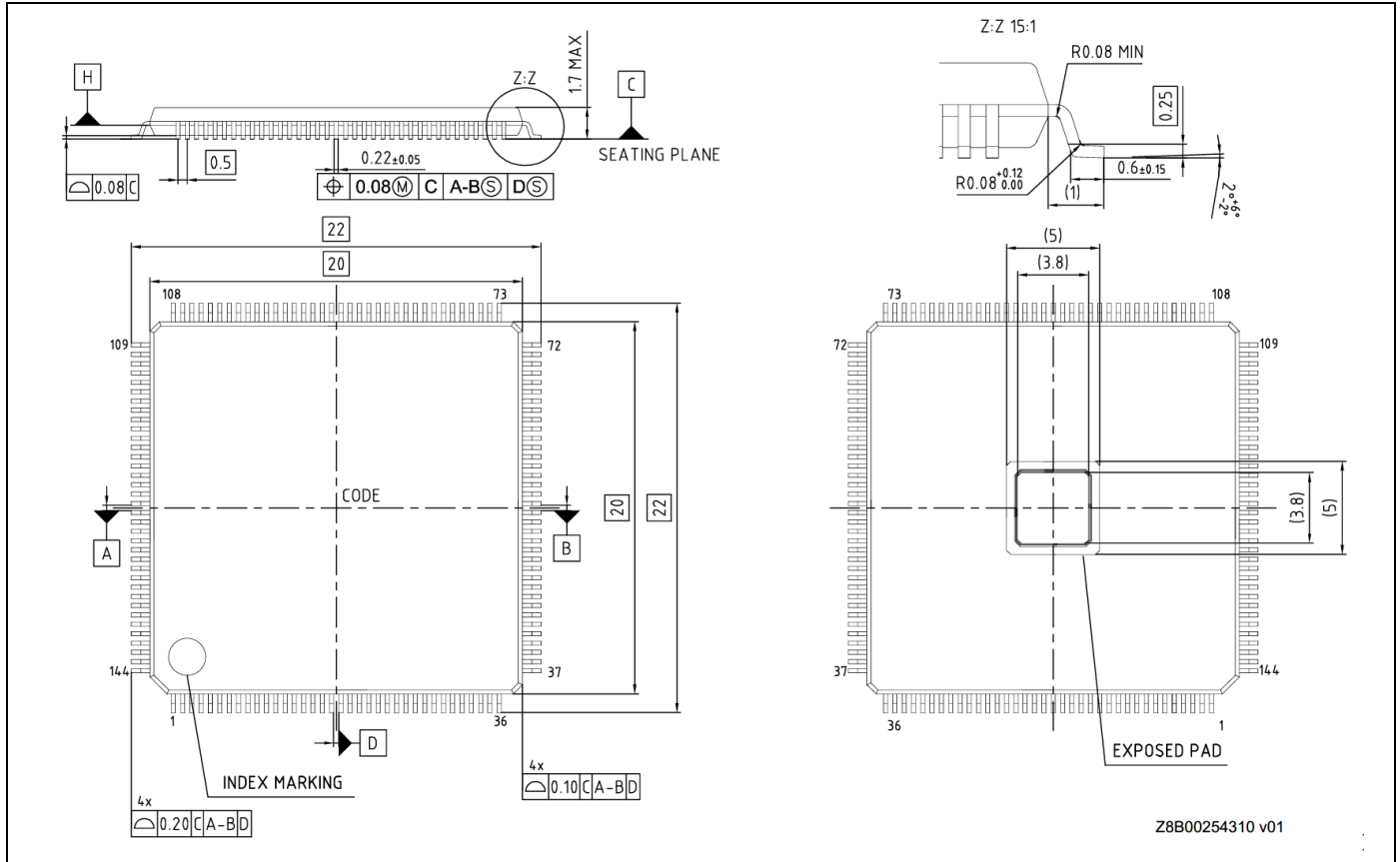
9.3 TEQFP176

| Package Type | Package Code |
|--------------|--------------|
| TEQFP 176 | LEF176 |



9.4 TEQFP144 (0.5 mm)

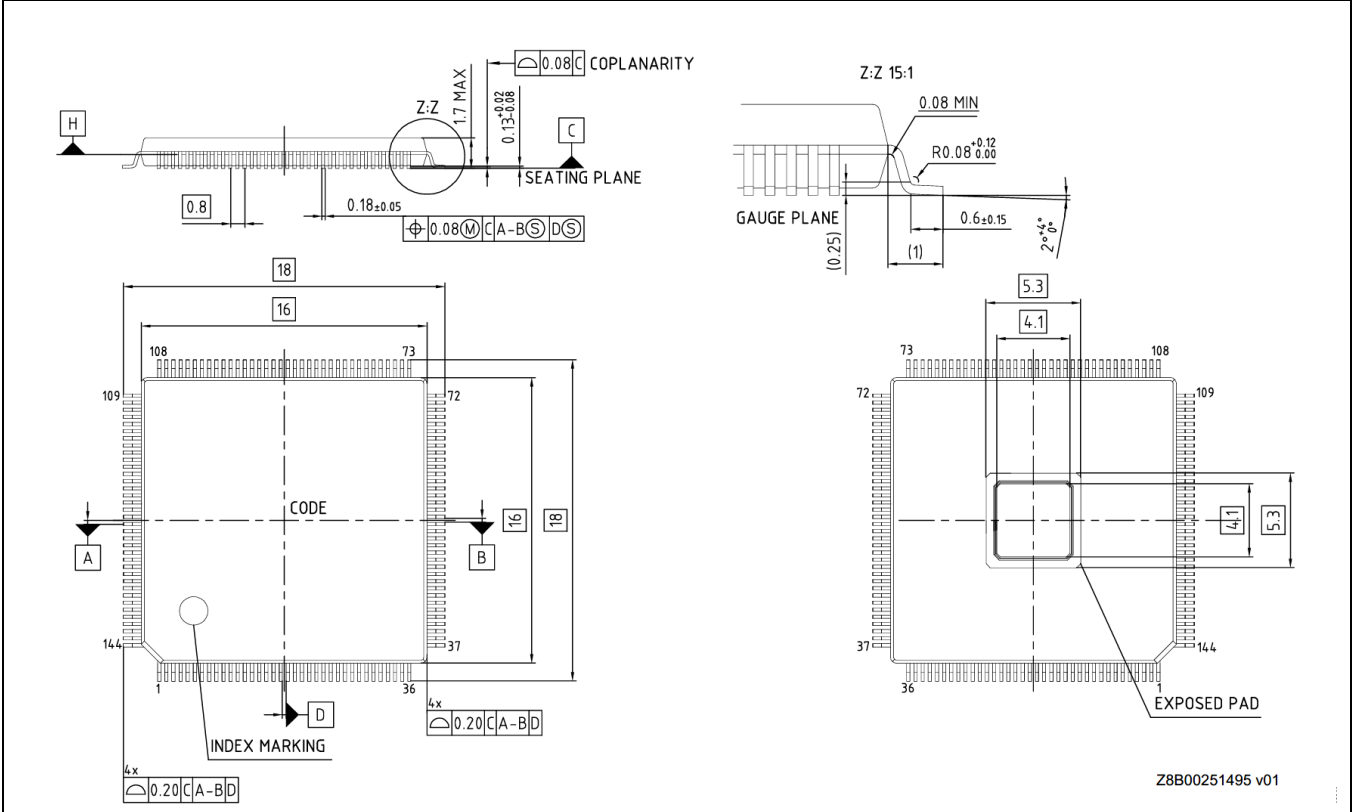
| Package Type | Package Code |
|--------------|--------------|
| TEQFP 144 | LEJ 144 |



Z8B00254310 v01

9.5 TEQFP144 (0.4 mm)

| Package Type | Package Code |
|--------------|--------------|
| TEQFP 144 | LEG 144 |



10. Acronyms

| Acronym | Definition |
|---------------|---|
| A/D converter | Analog digital converter |
| ADC | Analog-to-digital converter |
| AHB | Advanced high-performance bus |
| APB | Advanced peripheral bus |
| AXI | Advanced extensible interface |
| BT | Base timer |
| CAN | Controller area network |
| CAN FD | Controller area network with flexible data rate |
| CD | Clock domain |
| CPU | Central processing unit |
| CR | CR oscillator |
| CRC | Cyclic redundancy check |
| CSV | Clock supervisor |
| DDR | Double data rate |
| DDRHSSPI | DDR High Speed SPI |
| DMA | Direct memory access |
| DMAC | DMA controller |
| EBI | External bus interface |
| ECC | Error correction code |
| ETM | Embedded trace macro |
| EXT IRC | External interrupt controller |
| EXT IRQ | External interrupt request |
| FPU | Floating point unit |
| FRT | Free-run timer |
| GPIO | General-purpose I/O |
| GT | Global timer |
| HPM | High-performance matrix |
| HW-WDT | Hardware watchdog timer |
| I/O | Input or output |
| ICU | Input capture unit |
| IND PWM | Indicator pulse width modulation |
| IRC | Interrupt controller |
| IRQ | Interrupt request |
| I2S | Inter-IC sound |
| JTAG | Joint Test Action Group |
| LCD | Liquid crystal display |
| LCDC | LCD controller |
| LCD_IF | LCD bus interface |
| LIN | local interconnect network |
| LVD | Low-voltage detector |
| MCU | Microcontroller unit |

| Acronym | Definition |
|-----------|---|
| MFS | Multi-function serial interface |
| MPU | Memory protection unit |
| NF | Noise filter |
| NMI | Non-maskable interrupt |
| OCU | Output compare unit |
| OSC | Oscillator |
| PCM | Pulse code modulation |
| PD | Power domain |
| PLL | Phase-locked loop |
| PONR | Power-on reset |
| PPC | Port pin configuration |
| PPU | Peripheral protection unit |
| PRGCRC | Programmable CRC |
| PWM | Pulse width modulation |
| PWU | Partial wake up |
| QPRC | Quadrature Position/ Revolution Counter |
| RAM | Random access memory |
| RLT | Reload timer |
| ROM | Read-only memory |
| RTC | Real-time clock |
| SDR | Single data rate |
| SG | Sound generator |
| SHE | Secure Hardware Extension |
| SMC | Stepper motor control |
| SPI | Serial peripheral interface |
| SRAM | Static RAM |
| SSCG | Spread spectrum clock generator |
| SWFG | Sound waveform generator |
| SW-WDT | Software watchdog timer |
| SYSC | System controller |
| TCFLASH | Flash connected to TCM |
| TCM | Tightly coupled memory |
| TCRAM | RAM connected to TCM |
| TPU | Timing protection unit |
| WDR | Watchdog description record |
| WDT | Watchdog timer |
| WorkFLASH | Work Flash memory |

11. Errata

This section describes the errata for the S6J3360 and S6J3370 Series. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

| Part Number ^{*1} |
|---------------------------|
| S6J33xxHxxxL2xxxx |
| S6J33xxHxxxC2xxxx |
| S6J33xxHxxxV2xxxx |
| S6J33xxHxxxE2xxxx |
| S6J33xxJxxxE2xxxx |

*1: "x" is a part number option. For details, see section 1.2.1 Basic Option"

S6J3360 and S6J3370 Qualification Status

Product Status: Production

Errata Summary

The following table defines the errata applicability to available S6J3360 and S6J3370 Series devices.

| Items | Part Number ^{*1} | Fix Status |
|---|---|------------------------|
| 1. MCAN wrong message transmission | S6J33xxHxxxL2xxxx S6J33xxHxxxC2xxxx S6J33xxHxxxV2xxxx S6J33xxHxxxE2xxxx S6J33xxJxxxE2xxxx | No silicon fix planned |
| 2. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID | | |
| 3. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID | | |

*1: "x" is a part number option. For details, see section 1.2.1 Basic Option"

1. MCAN wrong message transmission

■ Problem Definition

There is a possibility a message with an ID (arbitration field) and a format and DLC (control field) is transmitted which was not configured by the application. The message itself is syntactically correct and can be received by other nodes.

The occurrence of the limitation requires a certain relationship in time between a transmission request for sending a message and the coincidence of noise in the 3rd bit of intermission field which is treated as the start of new message transmission (SoF).

■ Trigger Condition

Under the following conditions a message with wrong ID, format and DLC is transmitted:

- M_CAN is in state "Receiver" (PSR.ACT = "10"), no pending transmission.
- A new transmission is requested after sample point of 2nd bit of intermission but before the 3rd bit of Intermission is reached.
- The CAN bus is sampled dominant at the third bit of Intermission which is treated as SoF (see ISO11898-1:2015 section 10.4.2.2).

■ Scope of Impact

Under the conditions listed above it may happen, that:

- The shift register is not loaded with ID, format, and DLC of the requested message.

- The M_CAN will start arbitration with wrong ID, format, and DLC.
- In case the ID won arbitration, a CAN message with valid CRC is transmitted.
- In case this message is acknowledged, the ID stored in the Tx Event FIFO is the ID of the requested Tx message and not the ID of the message transmitted on the CAN bus
- Neither an error is detected by the transmitting node nor at the receiving node.

■ Workaround

Workaround 1:

This workaround avoids submitting a transmission request in the critical time window of about one bit time before the sample point of the 3rd bit of intermission field when on other pending transmission request exists:

- Requests a new transmission if another transmission is already pending or when the M_CAN / M_TTCAN is not in state "Receiver" (when PSR.ACT ≠ "10").
- If no pending transmission request exists, the application software needs to evaluate the Rx Interrupt flags IR.DRX, IR.RF0N, IR.RF1N which are set at the last bit of EoF when a received and accepted message gets valid.
- A new transmission may be requested by writing to TXBAR once the Rx interrupt occurred and the application waited another 3 bit times before submitting its Tx request. Note the Rx interrupt is generated at the last bit of EoF which is followed by three bits of Intermission.
- The application has to take care that the transmission request for the CAN Protocol Controller is activated before the critical window of the following reception is reached.

A supplemental action can be applied in order to detect messages which contain wrong ID and control field information:

- A checksum covering arbitration and control fields can be added to the data field of the message to be transmitted, to detect frames transmitted with wrong arbitration and control fields.

Workaround 2:

This workaround ensures that always at least one pending Tx request exists. If that is the case, the application may launch its Tx requests at any time without suffering from the limitation.

- Defines a low priority message with DLC = 0 that can be sent without harm. For example, loses arbitration against all other application messages, does not pass any acceptance filter of nodes in the same network. DLC = 0 shall reduce latency for other application messages.
- Configures sufficient Tx buffers – at least two - for this message type, therefore there is always another one waiting to be sent. E.g. an application that cannot react quickly enough with the time a single message of this type is sent, more than 2 Tx buffer may become necessary.
- The application uses the standard interfaces of the CAN / CAN FD stack to feed these messages.
- Whenever Tx confirmation is indicated for the second but last message of this type with pending Tx request, the application needs to submit at least one new Tx request. Note Tx confirmation is a standard feature in the AUTOSAR SW architecture.
- Before initially leaving INIT state of the M_CAN IP by clearing CCCR.INIT bit, make sure to activate a Tx request after having cleared CCCR.CCE. This will ensure that the conditions for the occurrence of the limitation when synchronizing to the CAN bus the first time after RESET are prevented.

■ Fix Status

No silicon fix planned.

2. CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID

■ Problem Definition

CAN FD controller message order inversion when multiple Tx Buffers that are configured with the same Message ID have pending Tx requests.

■ Configuration

Several Tx Buffers are configured with the same Message ID. Transmission of these Tx Buffers is requested sequentially with a delay between the individual Tx requests.

■ Expected behavior

When multiple Tx Buffers that are configured with the same Message ID have pending Tx requests, they shall be transmitted in ascending order of their Tx Buffer numbers. The Tx Buffer with lowest buffer number and pending Tx request is transmitted first.

■ Observed behavior

It may happen, depending on the delay between the individual Tx requests, that where multiple Tx Buffers are configured with the same Message ID the Tx Buffers are not transmitted in order of the Tx Buffer number (lowest number first).

■ Workaround

First, write the group of Tx messages with the same Message ID to the Message RAM and then request transmission of all these messages concurrently by a single write access to TXBAR. Before requesting a group of Tx messages with this Message ID, ensure that no message with this Message ID has a pending Tx request.

Applications not able to use the above workaround can implement a counter within the data section of their messages sent with same ID in order to allow the recipients to determine the correct sending sequence.

■ Fix Status

No silicon fix planned.

3. CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID**■ Problem Definition**

There was an incomplete description related to transmission from multiple buffers configured with the same Message ID in *Section 3.5.2 Dedicated Tx Buffers* and *Section 3.5.4 Tx Queue* of the Hardware Manual.

■ Detailed explanation

The following is the updated description in *Section 3.5.2 Dedicated Tx Buffers* and *Section 3.5.4 Tx Queue* of the Hardware Manual.

Section 3.5.2 Dedicated Tx Buffers:

- Original content in the Hardware Manual:

In case that multiple Tx Buffers are configured with the same Message ID, the Tx Buffer with the lowest buffer number is transmitted first.

- Enhancement:

These Tx buffers shall be requested in ascending order with the lowest buffer number first. Alternatively, all Tx buffers configured with the same Message ID can be requested simultaneously by a single write access to TXBAR.

Section 3.5.4 Tx Queue:

- Original content in the Hardware Manual:

In case that multiple Queue Buffers are configured with the same Message ID, the Queue Buffer with the lowest buffer number is transmitted first.

- Replacement:

In case that multiple Tx Queue buffers are configured with the same Message ID, the transmission order depends on numbers of the buffers where the messages were stored for transmission. As these buffer numbers depend on the then current states of the PUT index, a prediction of the transmission order is not possible.

- Original content in the Hardware Manual:

An Add Request cyclically increments the Put Index to the next free Tx Buffer.

- Replacement:

The Put Index always points to that free buffer of the Tx Queue with the lowest buffer number.

■ Workaround

In case a defined order of transmission is required, the Tx FIFO shall be used for transmission of messages with the same Message ID. Alternatively dedicated Tx buffers with same Message ID shall be requested in ascending order with the lowest buffer number first or by a single write access to TXBAR. Alternatively, a single Tx Buffer can be used to transmit those messages one after the other.

■ Fix Status

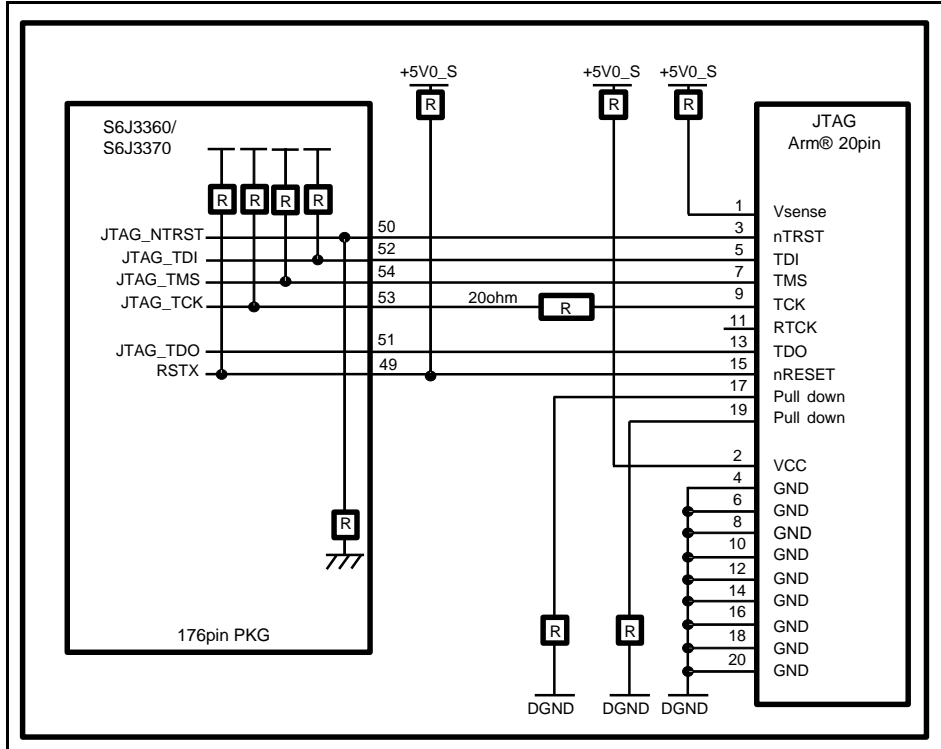
No silicon fix planned. Use workaround.

Hardware Manual will be updated accordingly.

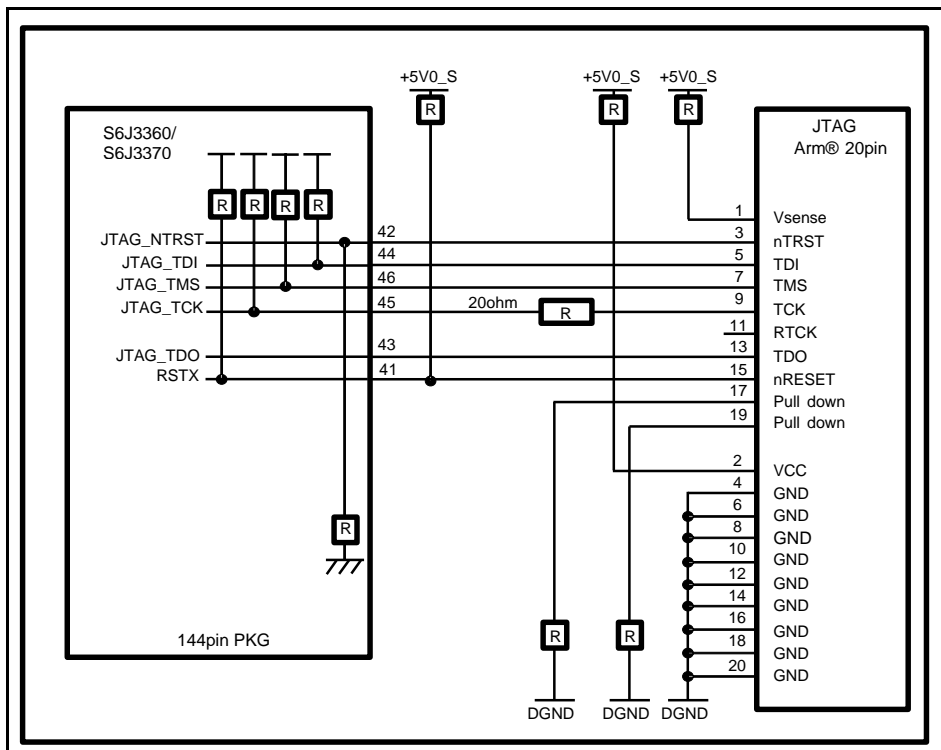
12. Appendix

12.1 Application 1: JTAG tool Connection

This is an application example of JTAG tool connection with 176-pin PKG.



This is an application example of JTAG tool connection with 144-pin PKG.



13. Major Changes

| Page | Section | Change Results | | | | | | | | | | | | |
|---------------------|-------------------------|---|---------------|-------------------|-------------------|-------------------|-------------------|-------------------|---------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Rev *H | | | | | | | | | | | | | | |
| 136, 137 | 8. Ordering Information | Updated all Part Numbers and Packages | | | | | | | | | | | | |
| 145 | 11. Errata | Revised the shading parts as below: Error) <table border="1"> <thead> <tr> <th>Part Number*1</th> </tr> </thead> <tbody> <tr><td>S6J337xHxxxL2xxxx</td></tr> <tr><td>S6J33xxHxxxC2xxxx</td></tr> <tr><td>S6J337xHxxxV2xxxx</td></tr> <tr><td>S6J33xxHxxxE2xxxx</td></tr> <tr><td>S6J33xxJxxxE2xxxx</td></tr> </tbody> </table> Correct) <table border="1"> <thead> <tr> <th>Part Number*1</th> </tr> </thead> <tbody> <tr><td>S6J33xxHxxxL2xxxx</td></tr> <tr><td>S6J33xxHxxxC2xxxx</td></tr> <tr><td>S6J33xxHxxxV2xxxx</td></tr> <tr><td>S6J33xxHxxxE2xxxx</td></tr> <tr><td>S6J33xxJxxxE2xxxx</td></tr> </tbody> </table> | Part Number*1 | S6J337xHxxxL2xxxx | S6J33xxHxxxC2xxxx | S6J337xHxxxV2xxxx | S6J33xxHxxxE2xxxx | S6J33xxJxxxE2xxxx | Part Number*1 | S6J33xxHxxxL2xxxx | S6J33xxHxxxC2xxxx | S6J33xxHxxxV2xxxx | S6J33xxHxxxE2xxxx | S6J33xxJxxxE2xxxx |
| Part Number*1 | | | | | | | | | | | | | | |
| S6J337xHxxxL2xxxx | | | | | | | | | | | | | | |
| S6J33xxHxxxC2xxxx | | | | | | | | | | | | | | |
| S6J337xHxxxV2xxxx | | | | | | | | | | | | | | |
| S6J33xxHxxxE2xxxx | | | | | | | | | | | | | | |
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| S6J33xxHxxxE2xxxx | | | | | | | | | | | | | | |
| S6J33xxJxxxE2xxxx | | | | | | | | | | | | | | |
| 145, 146, 147 | 11. Errata | Added about CAN FD controller message order inversion when transmitting from dedicated Tx Buffers configured with same Message ID | | | | | | | | | | | | |
| 149 | 13. Major Changes | Added Major changes section. | | | | | | | | | | | | |
| Rev *I | | | | | | | | | | | | | | |
| 145, 147 | 11. Errata | Added about CAN FD incomplete description of Dedicated Tx Buffers and Tx Queue related to transmission from multiple buffers configured with the same Message ID | | | | | | | | | | | | |
| 138 139 | 9. Package Dimensions | Updated package drawing spec from 002-13015 *A to *B Updated package drawing spec from 002-14045 ** to *A | | | | | | | | | | | | |
| Rev *J | | | | | | | | | | | | | | |

| 136 | 8. Ordering Information | <p>Revised the shading parts as below:</p> <p>Error)</p> <table border="1"> <thead> <tr> <th>Part Number</th> <th>Package</th> </tr> </thead> <tbody> <tr> <td>S6J336CHSBSV20000</td> <td>LQS144 (144-pin 0.4-mm pitch plastic LQFP)</td> </tr> <tr> <td>S6J336AHSBSL20000</td> <td>LQN144 144-pin 0.4-mm pitch plastic LQFP)</td> </tr> <tr> <td>S6J336CHSBSL20000</td> <td>LQN144 144-pin 0.4-mm pitch plastic LQFP)</td> </tr> <tr> <td>:</td> <td>:</td> </tr> </tbody> </table> <p>Correct)</p> <table border="1"> <thead> <tr> <th>Part Number</th> <th>Package</th> </tr> </thead> <tbody> <tr> <td>S6J336CHSBSV20000</td> <td>LQS144 (144-pin 0.5-mm pitch plastic LQFP)</td> </tr> <tr> <td>S6J336AHSBSL20000</td> <td>LQN144 (144-pin 0.4-mm pitch plastic LQFP)</td> </tr> <tr> <td>S6J336CHSBSL20000</td> <td>LQN144 (144-pin 0.4-mm pitch plastic LQFP)</td> </tr> <tr> <td>:</td> <td>:</td> </tr> </tbody> </table> | Part Number | Package | S6J336CHSBSV20000 | LQS144 (144-pin 0.4-mm pitch plastic LQFP) | S6J336AHSBSL20000 | LQN144 144-pin 0.4-mm pitch plastic LQFP) | S6J336CHSBSL20000 | LQN144 144-pin 0.4-mm pitch plastic LQFP) | : | : | Part Number | Package | S6J336CHSBSV20000 | LQS144 (144-pin 0.5-mm pitch plastic LQFP) | S6J336AHSBSL20000 | LQN144 (144-pin 0.4-mm pitch plastic LQFP) | S6J336CHSBSL20000 | LQN144 (144-pin 0.4-mm pitch plastic LQFP) | : | : |
|-------------------|--|--|-------------|--------------|-------------------|---|-------------------|--|-------------------|--|-------------------|--|-------------|---------|-------------------|---|-------------------|---|-------------------|---|---|---|
| Part Number | Package | | | | | | | | | | | | | | | | | | | | | |
| S6J336CHSBSV20000 | LQS144 (144-pin 0.4-mm pitch plastic LQFP) | | | | | | | | | | | | | | | | | | | | | |
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| : | : | | | | | | | | | | | | | | | | | | | | | |
| Rev *K | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 1.2.1 Basic Option | <p>Added the shading parts as below:</p> <p>Packing</p> <table border="1"> <thead> <tr> <th>Digit</th> <th>Packing type</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Tray</td> </tr> <tr> <td>D</td> <td>Tape and Reel</td> </tr> </tbody> </table> | Digit | Packing type | 0 | Tray | D | Tape and Reel | | | | | | | | | | | | | | |
| Digit | Packing type | | | | | | | | | | | | | | | | | | | | | |
| 0 | Tray | | | | | | | | | | | | | | | | | | | | | |
| D | Tape and Reel | | | | | | | | | | | | | | | | | | | | | |
| 136 | 8. Ordering Information | <p>Added the shading parts as below:</p> <table border="1"> <thead> <tr> <th>Part Number</th> <th>Package</th> </tr> </thead> <tbody> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>S6J336CHTBSE20000</td> <td>LEJ144 (144-pin 0.5-mm pitch plastic TEQFP)</td> </tr> <tr> <td>S6J336CHTBSE2D000</td> <td>LEJ144 (144-pin 0.5-mm pitch plastic TEQFP)</td> </tr> <tr> <td>S6J337AHTBSE20000</td> <td>LEJ144 (144-pin 0.5-mm pitch plastic TEQFP)</td> </tr> <tr> <td>:</td> <td>:</td> </tr> </tbody> </table> | Part Number | Package | : | : | S6J336CHTBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) | S6J336CHTBSE2D000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) | S6J337AHTBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) | : | : | | | | | | | | |
| Part Number | Package | | | | | | | | | | | | | | | | | | | | | |
| : | : | | | | | | | | | | | | | | | | | | | | | |
| S6J336CHTBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) | | | | | | | | | | | | | | | | | | | | | |
| S6J336CHTBSE2D000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) | | | | | | | | | | | | | | | | | | | | | |
| S6J337AHTBSE20000 | LEJ144 (144-pin 0.5-mm pitch plastic TEQFP) | | | | | | | | | | | | | | | | | | | | | |
| : | : | | | | | | | | | | | | | | | | | | | | | |

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: S6J3360 Series, S6J3370 Series 32-bit Arm® Cortex®-R5F TRAVEO™ T1G Microcontroller
Document Number: 002-03359

| Revision | ECN | Submission Date | Description of Change |
|----------|---------|-----------------|--|
| ** | 5017504 | 01/19/2016 | New Spec. |
| *A | 5247224 | 04/28/2016 | Removed HyperBUS from Function List and Pin Descriptions, Removed Spanion. Added 2.Precautions and Handling Devices and 3. Handling Devices |
| *B | 5461846 | 10/05/2016 | 208-pin was reduced for feasibility study and customer demand. Updated 1.2.1 Basic Option MFS1_CS0_1 144 pin: Added 8 pin MFS1_CS1_0 120 pin: Deleted 8 pin MFS3_CS0_1 100 pin: Added 91 pin MFS3_CS1_1 100 pin: Added 92 pin MFS3_CS2_1 100 pin: Added 93 pin MFS3_CS3_1 100 pin: Added 94 pin MFS9_CS1_0 100 pin: Added 64 pin MFS10_SIN_0 176 pin: Added 119 pin MFS11_CS0_0 176 pin: Added 121 pin MFS11_CS0_1 176 pin: Deleted 121 pin MFS11_CS0_1 144 pin: Deleted 100 pin MFS11_CS1_0 144 pin: Added 100 pin MFS6_SCL 176 pin: Added 77 pin ICU0_IN0_0 120 pin: Added 44 pin OCU1_OUT1_0 120 pin: Added 54 pin OCU10_OUT0_0 100 pin: Deleted 54 pin OCU10_OUT1_0 100 pin: Added 54 pin BT0_TIOB0_0 100 pin: Added 54 pin BT1_TIOA2_0 120 pin: Added 46 pin BT1_TIOA2_1 100 pin: Deleted 54 pin BT1_TIOA3_0 100 pin: Deleted 46 pin BT1_TIOA3_0 120 pin: Added 47 pin BT9_TIOB18_0 100 pin: Deleted 63 pin BT9_TIOB18_0 100 pin: Added 71 pin BT10_TIOA20_0 100 pin: Deleted 64 pin BT10_TIOA20_0 100 pin: Added 67 pin P1_12 100 pin: Deleted 112 pin P1_12 100 pin: Added 58 pin P2_30 208 pin: Deleted 202 pin P2_30 208 pin: Added 207 pin P2_31 208 pin: Deleted 203 pin I2S1_SD_0 Corrected I2S Communication Port 1 SD_0 I2S1_WS_0 |

| Revision | ECN | Submission Date | Description of Change |
|----------|-----|-----------------|--|
| | | | Corrected I2S Communication Port 1 WS_0 I2S1_SCK_0 Corrected I2S Communication Port 1 SCK_0 MAD16 Corrected Extension BUS Interface address 16 MAD17 Corrected Extension BUS Interface address 17 MAD18 Corrected Extension BUS Interface address 18 MAD19 Corrected Extension BUS Interface address 19 MAD20 Corrected Extension BUS Interface address 20 MAD21 Corrected Extension BUS Interface address 21 MWEX Corrected Extension BUS Interface Write to WE CS# Corrected LCD BUS interface data 0 to CS# WR# Corrected LCD BUS interface data 0 to WR# RD# Corrected LCD BUS interface data 0 to RD# RS Corrected LCD BUS interface data 0 to RS RES# wrong LCD BUS interface data 0, corrected LCD BUS interface RES# TE Corrected LCD BUS interface data 0 to TE C 100pin: Deleted 41 pin C 100pin: Added 36 pin Updated VCC 100 pin Updated VCC 208 pin Updated VSS 100 pin Updated VSS 120 pin Updated VSS 176 pin Updated VSS 208 pin Updated Block Diagram Updated pin name in 7.4.6 Multi Function serial, 7.4.7 Timer Input, 7.4.8 QPRC timing, and 7.4.9 Trigger Input Added 7.4.13 High Current Output Slew Rate and 7.4.14 Clock output timing, 7.4.15/7.4.16/7.4.17 External bus I/F timing and 7.4.18 DDR-HSSPI Updated Ordering information Updated Package Dimensions Updated Acronyms |

| Revision | ECN | Submission Date | Description of Change |
|----------|---------|-----------------|--|
| *C | 5626913 | 02/14/2017 | Updated following contents. -1.Features -4.Pin Assignment -5.Pin descriptions -6.Block Diagram -7.Electrical characteristics -8.Ordering Information -9.Package Dimensions Added 11.Appendix |
| *D | 5731385 | 05/09/2017 | Update PKG information -9.Package Dimensions |
| *E | 5919824 | 10/17/2017 | Updated following contents. -1.Features -3.Handling Devices -7.Electrical characteristics |
| *F | 6006783 | 12/27/2017 | Updated following contents. -1.Features -4.Pin Assignment -5.Pin descriptions -7.Electrical characteristics -8.Ordering Information -9.Package Dimensions |
| *G | 6286821 | 08/21/2018 | Updated following contents. - Updated package line up - Added the feedback resistor value of oscillation I/O - Added the recommendation mounting condition - Added the value of IO hysteresis voltage - Updated the value of Power Supply Current - Updated the value of DDR-HSSPI - Added the contents of Errata |
| *H | 7101781 | 04/05/2021 | Updated 8. Ordering Information Updated 11. Errata Added 13. Major Changes For details, see 13. Major Changes |
| *I | 7398097 | 10/25/2021 | Updated 11. Errata Updated package drawing spec from 002-13015 *A to *B Updated package drawing spec from 002-14045 ** to *A For details, see 13. Major Changes |
| *J | 7436521 | 11/10/2021 | Updated 8. Ordering Information |
| *K | 7761661 | 05/13/2022 | Updated 1.2.1 Basic Option Updated 8. Ordering Information |
| *L | 8108197 | 02/13/2025 | Updated package diagrams in 9.Package Dimensions |

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