



**64-Mbit/32-Mbit S Models, 3 V,
Flash Memory with Page Mode, featuring
110 nm MirrorBit[®] Process Technology**

1. Introduction

This supplementary document provides information on a device designed for limited distribution. It describes how the features, operation, and ordering options of this device have been enhanced or changed from the standard device on which it is based. The information contained in this document modifies any information on the same topics established by the data sheets listed in the Affected Documents/Related Documents table and should be used in conjunction with those documents. This document may also contain information that was not previously covered by the S29GL-N data sheet. It is intended for hardware system designers and software developers of applications, operating systems, or tools.

1.1 Affected Documents/Related Documents

Title	Publication Number
S29GL-N MirrorBit [®] Flash Family Data Sheet (64 Mb/32 Mb)	S29GL-N_01

Contents

1. Introduction	1	4. Connection Diagrams & Physical Dimensions	9
1.1 Affected Documents/Related Documents	1	4.1 64-Ball BGA 10 mm x 13 mm Package Option	9
2. Device Description	3	4.2 FAA064 Connection Diagram	
2.1 Permanent Sector Lock Algorithm		64-Ball BGA 10 mm x 13 mm	9
Feature Description	3	4.3 FAA064 Physical Dimensions	10
2.2 Ordering Options Changed	3	4.4 LAA064 Connection Diagram	
2.3 Device Bus Operation Changed	4	64-Ball Fortified BGA, 13 mm x 11 mm	11
2.4 Device ID Changed	4	4.5 LAA064 Physical Dimensions	12
2.5 WP# Hardware Protection	4	4.6 LAE064 Connection Diagram	
3. Advance Sector Protection Clarification	5	64-Ball Fortified BGA, 9 mm x 9 mm	13
3.1 Persistent Protection Bit (PPB) Operation Changed	7	4.7 LAE064 Physical Dimensions	14
3.2 Distinguishing Between Permanent Sector Protection		5. Revision History	15
from Standard			
(Non-Permanent Sector Protection) Devices	7		
3.3 Global Volatile Sector Protection Freeze			
Command Set Changed	8		

2. Device Description

2.1 Permanent Sector Lock Algorithm Feature Description

The device offers a unique Permanent Sector Lock Algorithm that allows the host system to permanently secure the data in any desired sectors of the memory array via a software command at V_{CC} supply levels. There is no need for high voltage ($> V_{CC}$) on any pin during this operation. Initiating this software command sequence permanently disables both program and erase operations in any desired sectors. This feature protects the data in these areas from being changed or erased in any way after this command has been activated. Sectors can be incrementally locked at any time and in any sequence.

2.2 Ordering Options Changed

The ordering numbers (Valid Combination) for Permanent Sector Lock Products are formed by a combination of the following:

S29GL-N	90	D	F	I	S1	0	
							PACKING TYPE
							0 =Tray (standard)(See Note)
							2 =7" Tape and Reel
							3 =13" Tape and Reel
							MODEL NUMBER
							S1=Uniform 64 KB sector device, WP#/ACC= V_{IL} protect high addresses sector, LAA064 or LAE064
							S2=Uniform 64 KB sector device, WP#/ACC= V_{IL} protect low addresses sector, LAA064 or LAE064
							S3=Uniform 64 KB sector device, WP#/ACC= V_{IL} protect high addresses sector, FAA064
							S4=Uniform 64 KB sector device, WP#/ACC= V_{IL} protect low addresses sector, FAA064
							TEMPERATURE RANGE
							I = Industrial (-40°C to $+85^{\circ}\text{C}$)
							PACKAGE MATERIALS SET
							A = Standard
							F = Pb-free
							PACKAGE TYPE
							F = Fortified Ball Grid Array package, LAA064 or FAA064
							D = Fortified Ball Grid Array package, LAE064
							SPEED OPTION
							90 = 90 ns random access time ($V_{IO} = V_{CC} = 2.7\text{V} - 3.6\text{V}$)
							11 = 110 ns random access time ($V_{IO} = 1.65\text{V} - 3.6\text{V}$)
							DEVICE NUMBER/DESCRIPTION
							3.0 Volt-only, Page-Mode Flash Memory Manufactured on 110 nm MirrorBit process technology
							S29GL064N = 64 Mb (4 M x 16-Bit/8 M x 8-Bit)
							S29GL032N = 32 Mb (2 M x 16-Bit/4 M x 8-Bit)

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S29GL032N and S29GL064N Valid Combinations						
Device Number	Speed Option (ns)	Package, Material & Temperature Range	Model Number	Packaging Type		
S29GL032N S29GL064N	90, 110	DFI	S1, S2	0, 2, 3 (See Note)	LAE064	Fortified BGA
		FFI			LAA064	
					S3, S4	

Note

Type 0 is standard. Specify other options as required.

2.3 Device Bus Operation Changed

Permanent Sector Lock devices are in word (x16) configuration only, which is different from standard devices, where are both byte and word configurable.

2.4 Device ID Changed

Permanent Sector Lock devices have three byte Device IDs. These Device IDs are different from those found in standard S29GL-N devices. Customers can distinguish Standard and Permanent Sector Lock devices by reading the status of a Lock Register (See [Advance Sector Protection Clarification](#) for more details).

Table 2.1 S29GL-N (64 Mb/32 Mb S Models) Device Identification

Device	Cycle	CE#	OE#	WE#	A _{max} to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ15 to DQ8		DQ7 to DQ0
													BYTE# = V _{IH}	BYTE# = V _{IL}	
S29GL064N	Cycle 1	L	L	H	X	V _{ID}	X	L	X	L	L	H	22h	X	7Eh
	Cycle 2	L	L	H	X	V _{ID}	X	L	X	H	H	L	22h	X	09h
	Cycle 3	L	L	H	X	V _{ID}	X	L	X	H	H	H	22h	X	03h
S29GL032N	Cycle 1	L	L	H	X	V _{ID}	X	L	X	L	L	H	22h	X	7Eh
	Cycle 2	L	L	H	X	V _{ID}	X	L	X	H	H	L	22h	X	09h
	Cycle 3	L	L	H	X	V _{ID}	X	L	X	H	H	H	22h	X	04h

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, X = Don't care.

2.5 WP# Hardware Protection

The WP# Hardware Protection feature is always available, independent of the software managed protection method chosen.

The Write Protect function provides a hardware method of protecting certain boot sectors without using V_{ID}. This function is one of two provided by the WP#/ACC pin. For details on the ACC (Accelerated program) function, refer to the Accelerated Program Operation section of the S29GL032N/064N data sheet. If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the outermost 64 Kbyte boot sector independently of whether this sector were protected or unprotected using the method described in the Sector Protection section of the S29GL032N/064N data sheet. The outermost 64 KB is one sector containing the lowest addresses for S2/S4 model number devices, and the outermost 64 KB is one sector containing the highest addresses for S1/S3 model number device.

Note that the WP#/ACC contains an internal pull up; when connected, WP#/ACC is at V_{IH}.

3. Advance Sector Protection Clarification

The Advance Sector Protection feature can disable programming or erase operations in any or all sectors, and can be implemented via software and/or hardware methods. [Figure 3.1](#) and [Figure 3.2](#) illustrate a high level logic diagram between the Persistent Protection Mode and Password Protection Mode.

Figure 3.1 Persistent Protection Mode

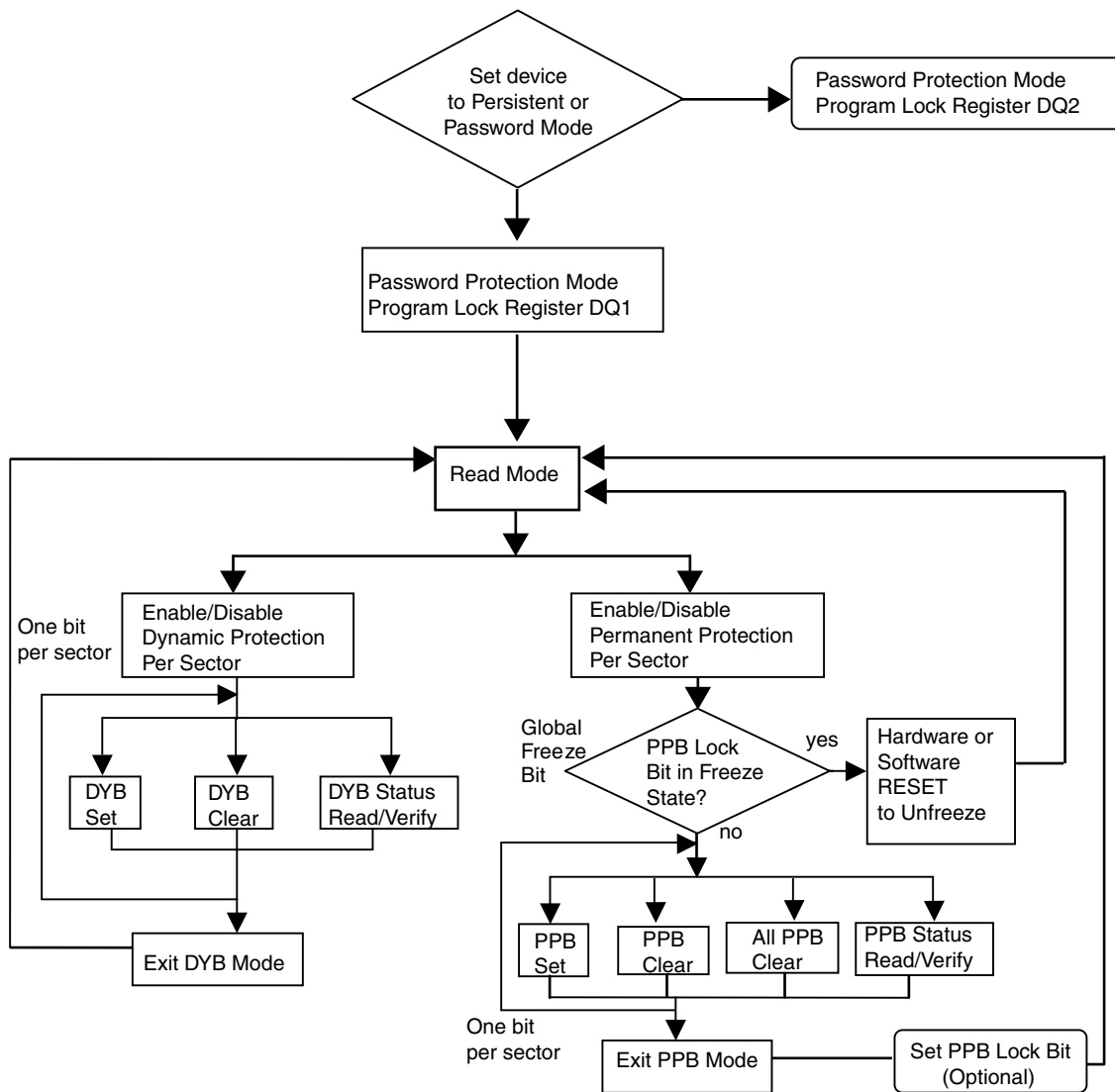
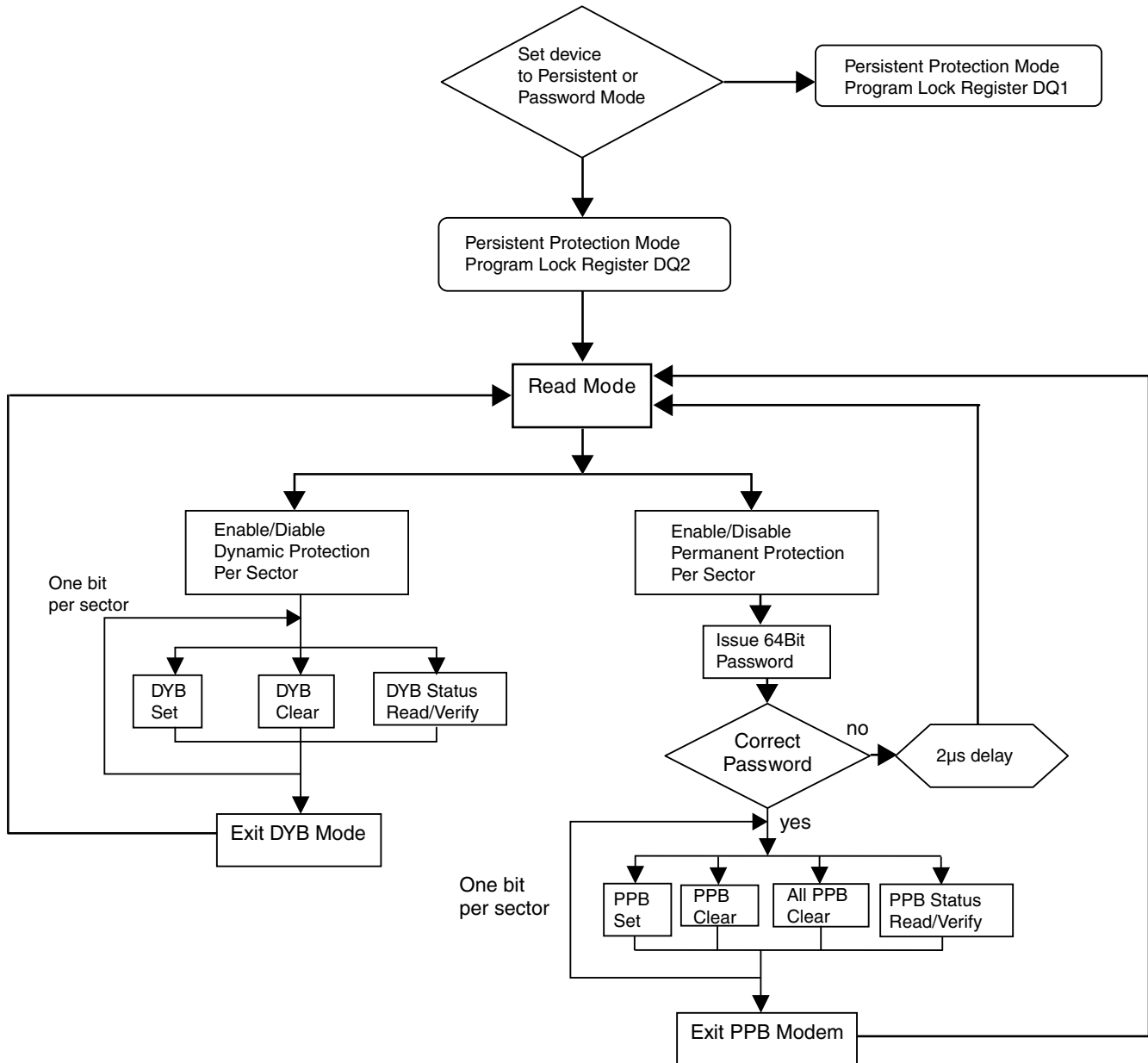


Figure 3.2 Password Protection Mode


3.1 Persistent Protection Bit (PPB) Operation Changed

Specifically the PPB (Persistent Protection Bit) feature has changed to only one time programmable (OTP).

A single Persistent (non-volatile) Protection Bit is assigned to each sector. If a PPB is programmed to the protected state through the “PPB Program” command, that sector will be protected from program or erase operations and will be read-only. Programming the PPB bit requires the typical word programming time without utilizing the Write Buffer.

Non-Volatile Sector Protection command sequence (see [Table 3.1](#)) must be issued for any of the following operations:

- Non-Volatile Sector Protection Command Set Entry
- PPB Program Command
- PPB Status Read Command
- Non-Volatile Sector Protection Command Set Exit

Notes

1. Non-Volatile Sector Protection Command Set Entry command, disables reads and writes from the main memory.
2. There are no means by which to individually erase or group erase a PPB, once it is programmed.

Table 3.1 Non-Volatile Sector Protection Command Set

Non-Volatile Sector Protection Command Set Definitions											
Command Sequence			Cycles	Bus Cycles (Notes 2-3)							
				First		Second		Third			
				Addr	Data	Addr	Data	Addr	Data		
PPB	Non-Volatile Sector Protection Command Set Entry	Word	3	555	AA	2AA	55	555	C0		
		Byte		AAA		555		AAA			
	PPB Program (Note 1), (Note 2)	Word	2	XXX	A0	SA	00				
		Byte		XXX							
	PPB Status Read (Note 2)	Word	1	SA	RD (0)						
		Byte									
	Non-Volatile Sector Protection Command Set Exit (Note 3)		Word	2	XXX	90	XXX	00			

Notes

1. When the ACC pin = V_{IH} , the protection status of (PPB or DYB) is checked: If protected, program and erase are ignored per sector basis; if not protected, program and erase are allowed on a per sector basis.
2. Protected State = “00h”, Unprotected State = “01h”.
3. The Exit command returns the device to reading the array.

3.2 Distinguishing Between Permanent Sector Protection from Standard (Non-Permanent Sector Protection) Devices

The Lock Register consists of 4 bits, (DQ3, DQ2, DQ1, and DQ0). The DQ2, DQ1, DQ0 bits of the Lock Register are programmable by the user. DQ3 of the Lock Register is available only as a special option for these devices, via Factory programming. Users are not allowed to program both DQ2 and DQ1 bits of the Lock Register to the 00 state. If the user tries to program DQ2 and DQ1 bits of the Lock Register to the 00 state, the device aborts the Lock Register programming operation and resets the DQ2 and DQ1 bits of the Lock Register back to the default 11 state. The programming time of the Lock Register is the same as the typical word programming time without utilizing the Write Buffer of the device. During a Lock Register programming sequence execution, the DQ6 Toggle Bit I toggles until the programming of the Lock Register has completed to indicate programming status. All Lock Register bits are readable to allow users to verify Lock Register statuses. Initial access time is required to read the Lock Register.

Table 3.2 Lock Register

DQ3	DQ2	DQ1	DQ0
Persistent Sector Protection OTP Bit	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	SecSi Sector Protection Bit

- SecSi Sector Protection Bit allows the user to lock the SecSi Sector area.
- Persistent Protection Mode Lock Bit allows the user to set the device permanently to operate in the Persistent Protection Mode.
- Password Protection Mode Lock Bit allows the user to set the device permanently to operate in the Password Protection Mode.
- Persistent Sector Protection OTP Bit is set at factory through Factory Set option to disable the “All PPB Erase” command.

Lock Register Command Set sequence (Table 3.3) is needed to program and read Lock Register Bits.

Table 3.3 Lock Register Command Set

Non-Volatile Sector Protection Command Set Definitions									
Command Sequence			Cycles	Bus Cycles					
				First		Second		Third	
				Addr	Data	Addr	Data	Addr	Data
Lock Register	Lock Register Command Set Entry (Note 1), (Note 2)	Word	3	555	AA	2AA	55	555	40
		Byte		AAA		555		AAA	
	Lock Register Bits Program (Note 3), (Note 4)	Word	2	XXX	A0	XXX	Data		
		Byte		XXX		XXX			
	Lock Register Bits Read (Note 3)	Word	1	00	Data				
		Byte							
	Lock Register Command Set Exit (Note 1), (Note 2)	Word	2	XXX	90	XXX	00		
		Byte		XXX		XXX			

Notes

1. The Exit command returns the device to reading the array.
2. If any of the Entry command was initiated, an Exit command must be issued to reset the device into read mode. Otherwise the device hangs.
3. All Lock Register bits are one-time programmable. Note that the program state = “0” and the erase state = “1”. Also note that of both the Persistent Protection Mode Lock Bit and the Password Protection Mode Lock Bit cannot be programmed at the same time or the Lock Register Bits Program operation aborts and returns the device to read mode. Lock Register bits that are reserved for future use default to “1’s”. The Lock Register is shipped out as “FFFF’s” before Lock Register Bit program execution.
4. Only DQ0, DQ1 and DQ2 are programmable by customer.

Table 3.4 Lock Register Bit Read-out Sequence

		DQ15 – DQ4 (Factory Default)	DQ3 Persistent Sector Protection OTP Bit	DQ2 Password Protection Mode Lock Bit	DQ1 Persistent Protection Mode Lock Bit	DQ0 SecSi Sector Protection Bit
New Device		1’s	1	1	1	1
Standard (non-Permanent Sector Protection Device)	Persistent Mode	1’s	1	1	0	X
	Password Mode	1’s	1	0	1	X
Permanent Sector Protection Device	Persistent Mode	1’s	0	1	0	X
	Password Mode	1’s	0	0	1	X

3.3 Global Volatile Sector Protection Freeze Command Set Changed

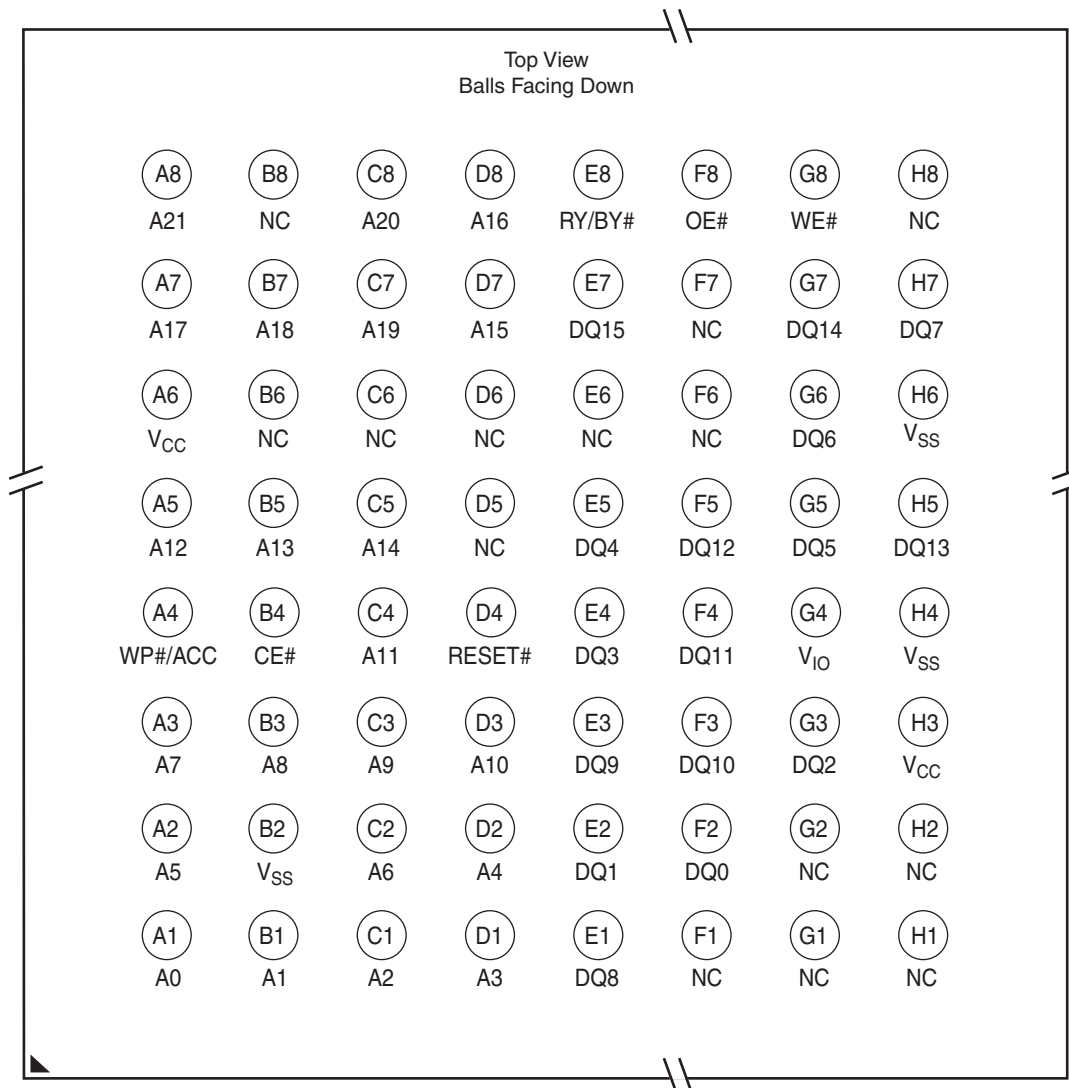
Due to the fact that PPB feature has changed to OTP, Global Volatile Sector Protection Freeze Command Set is not required.

4. Connection Diagrams & Physical Dimensions

4.1 64-Ball BGA 10 mm x 13 mm Package Option

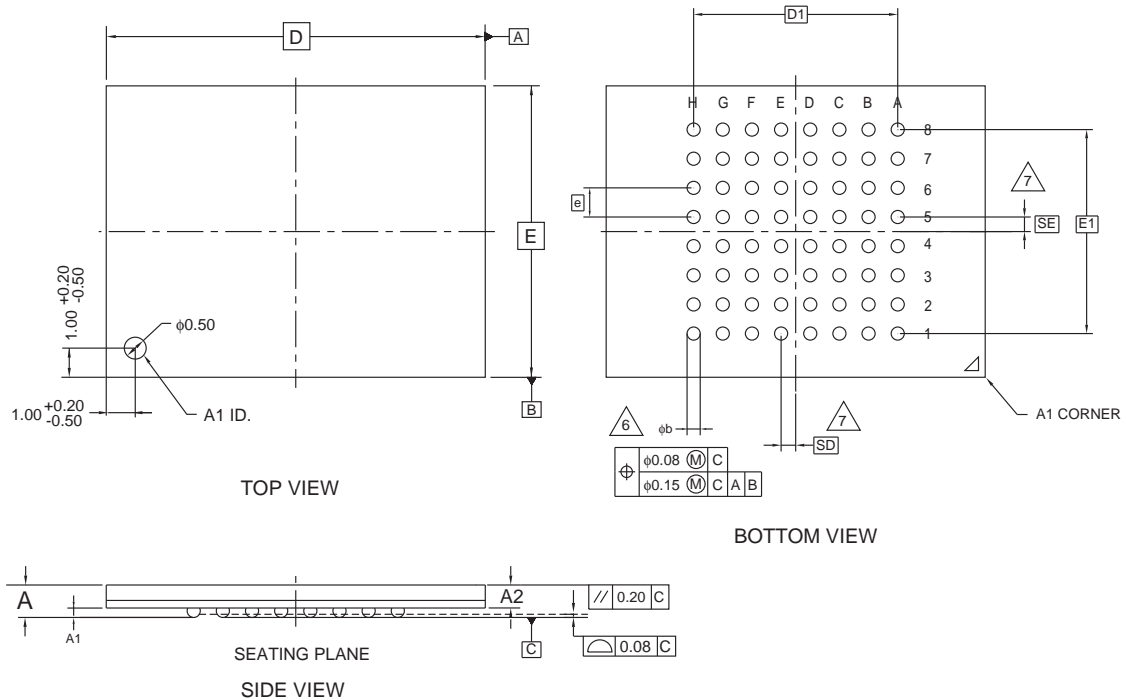
An additional package option is available for Permanent Sector Lock devices. This package option is a 64-Ball Grid Array (BGA) package with dimensions of 10 mm x 13 mm and a 1 mm ball pitch. Standard package option 64-Ball Fortified BGA are also available for Permanent Sector Lock devices.

4.2 FAA064 Connection Diagram 64-Ball BGA 10 mm x 13 mm


Note

1. Ball A8 is NC on S29GL032N.

4.3 FAA064 Physical Dimensions



NOTES:

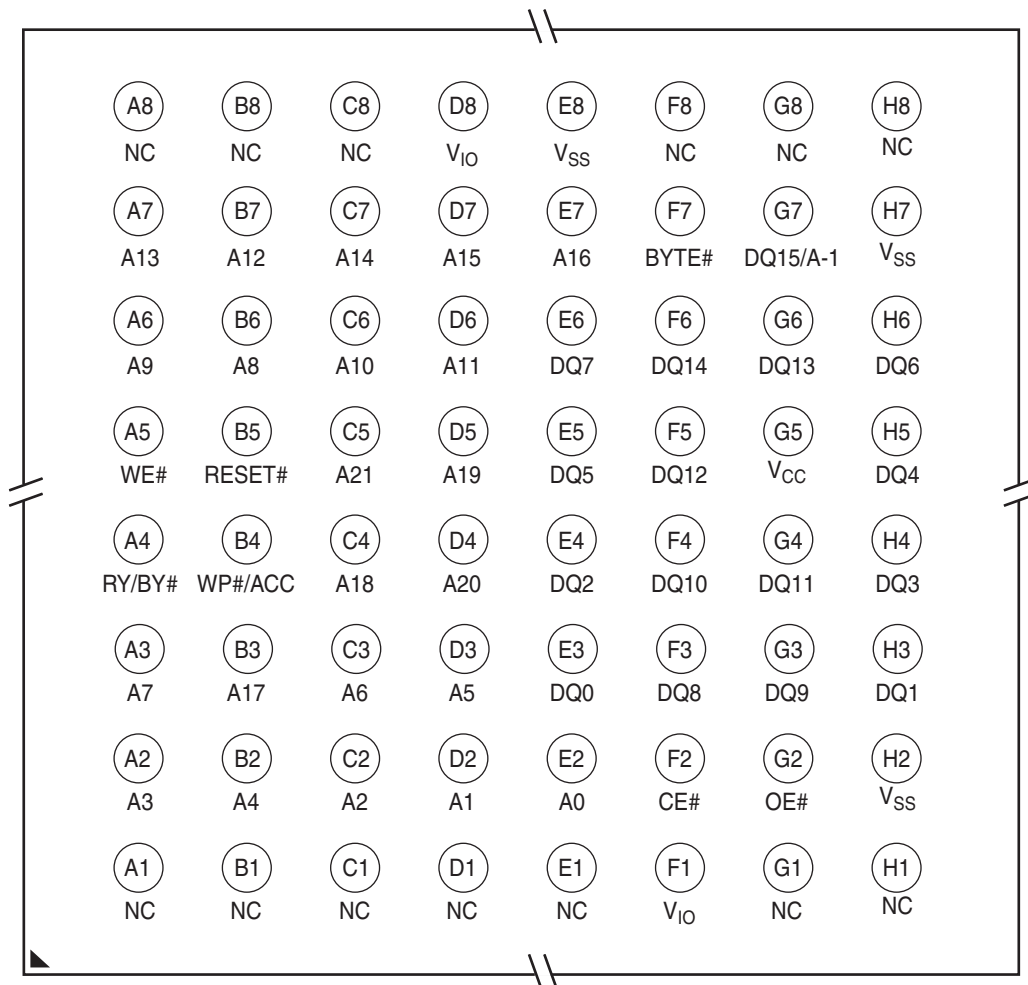
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
N IS THE TOTAL NUMBER OF SOLDER BALLS.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM Z.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = $\frac{e}{2}$
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- FOR PACKAGE THICKNESS, "A" IS THE CONTROLLING DIMENSION.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKINGS INDENTATION OR OTHER MEANS.

3174/38.9G

PACKAGE	FAA 064			NOTE
JEDEC	N/A			
	10.00 mm x 13.00 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	---	---	1.20	OVERALL THICKNESS
A1	0.30	---	---	BALL HEIGHT
A2	0.64	---	0.78	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	10.00 BSC.			BODY SIZE
D1	7.00 BSC.			BALL FOOTPRINT
E1	7.00 BSC.			BALL FOOTPRINT
MD	8			ROW MATRIX SIZE D DIRECTION
ME	8			ROW MATRIX SIZE E DIRECTION
N	64			TOTAL BALL COUNT
b	0.40	0.45	0.50	BALL DIAMETER
e	1.00 BSC			BALL PITCH
SD / SE	0.50 BSC			SOLDER BALL PLACEMENT

4.4 LAA064 Connection Diagram 64-Ball Fortified BGA, 13 mm x 11 mm

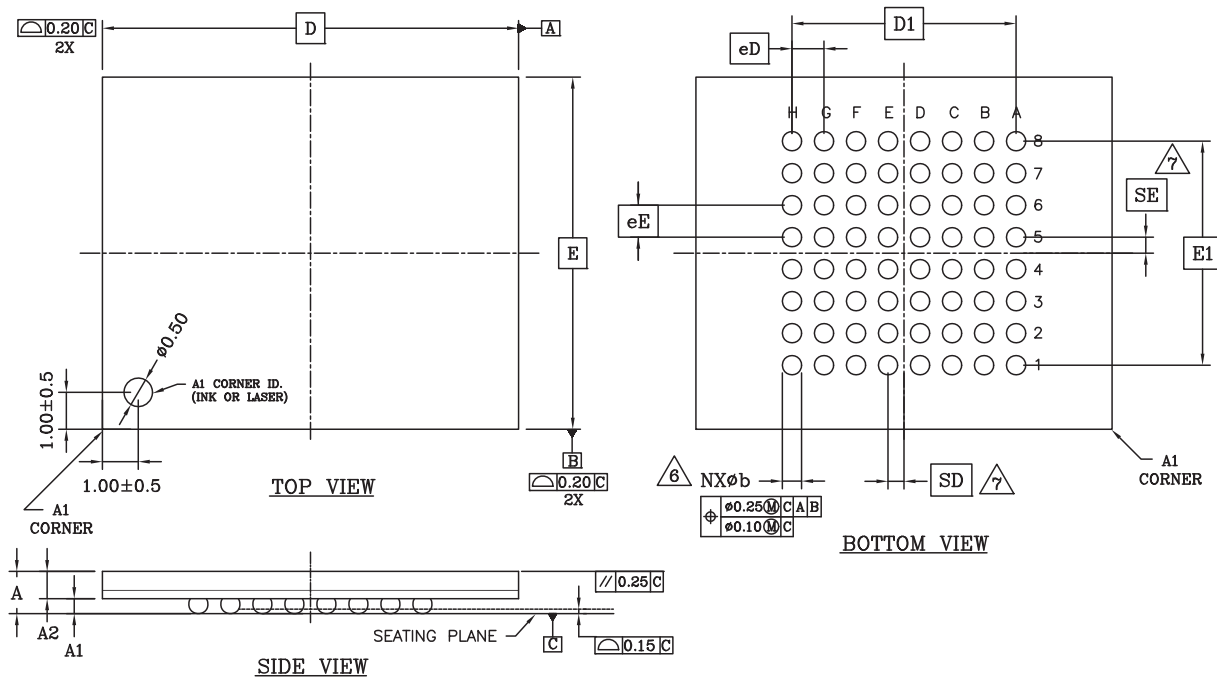
Top View, Balls Facing Down









Note




1. Ball C5 is NC on S29GL032N.

4.5 LAA064 Physical Dimensions




PACKAGE	LAA 064			
JEDEC	N/A			
	13.00x11.00 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	NOTE
A	—	—	1.40	PROFILE HEIGHT
A1	0.40	—	—	STANDOFF
A2	0.60	—	—	BODY THICKNESS
	13.00 BSC.			BODY SIZE
	11.00 BSC.			BODY SIZE
	7.00 BSC.			MATRIX FOOTPRINT
	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
øb	0.50	0.60	0.70	BALL DIAMETER
	1.00 BSC.			BALL PITCH — D DIRECTION
	1.00 BSC.			BALL PITCH — E DIRECTION
SD/SE	0.50 BSC.			SOLDER BALL PLACEMENT
	A1–A8, K1–K8			DEPOPULATED SOLDER BALLS

NOTES:

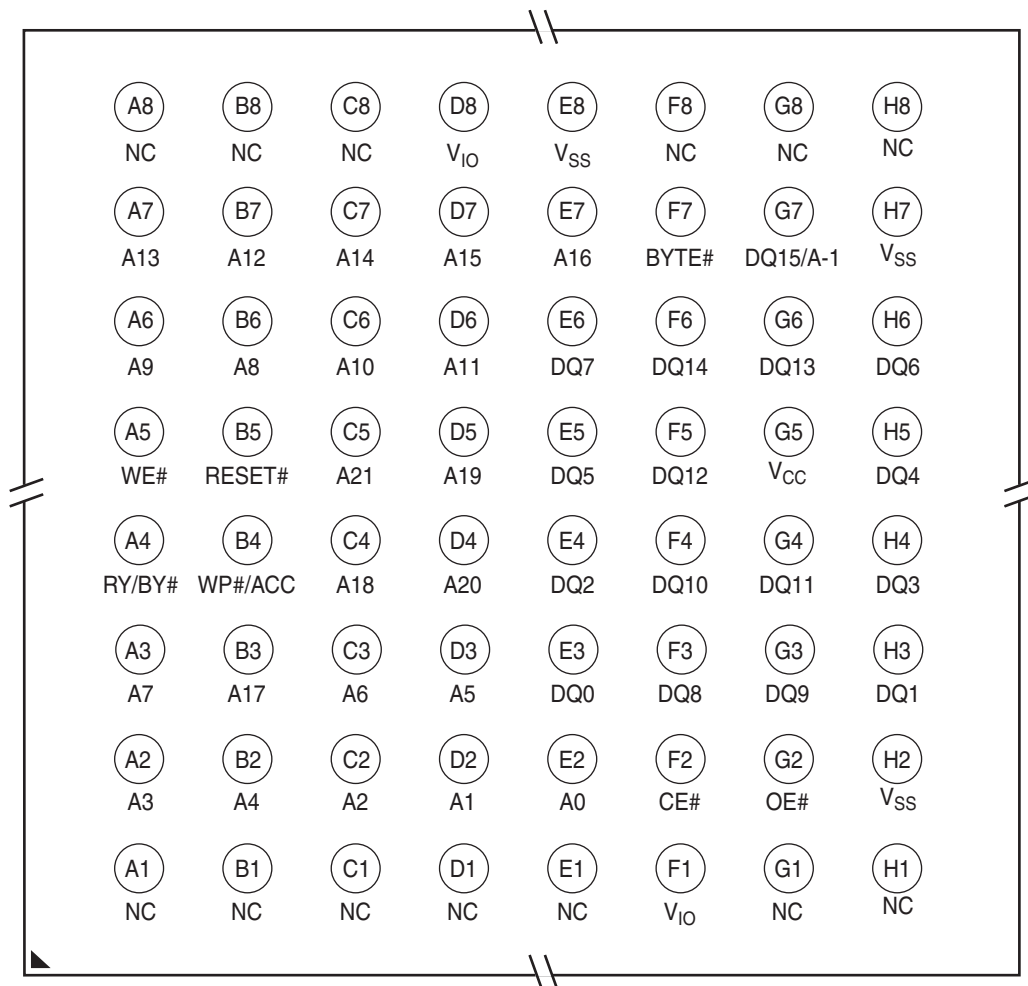
1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JESD 95-1, SFP-010 (EXCEPT AS NOTED).
4.  REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6.  DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM "C".
7.  SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 0.000.

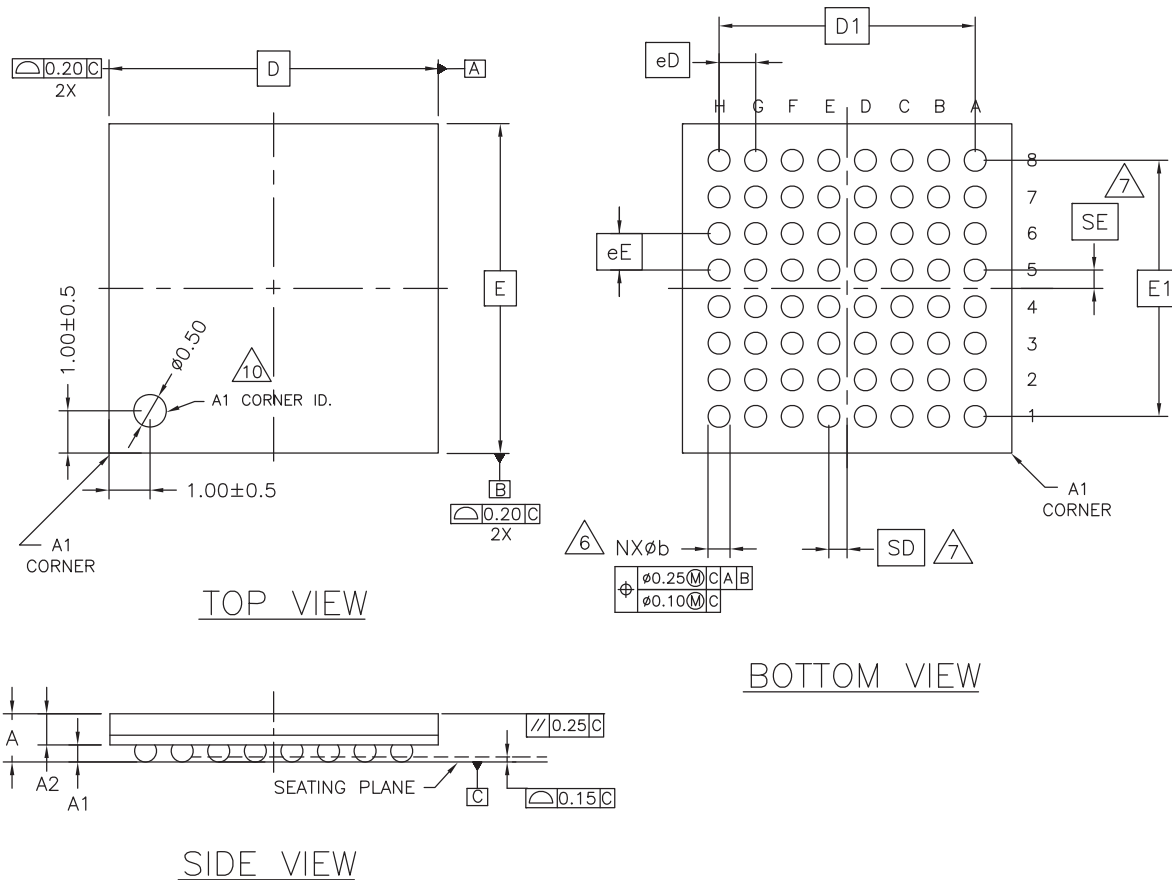
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = 
8. "X" IN THE PACKAGE VARIATIONS DENOTES PART IS UNDER QUALIFICATION.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

4.6 LAE064 Connection Diagram 64-Ball Fortified BGA, 9 mm x 9 mm

Top View, Balls Facing Down



4.7 LAE064 Physical Dimensions



PACKAGE	LAE 064			
JEDEC	N/A			
	9.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
<div>D</div>	9.00 BSC.			BODY SIZE
<div>E</div>	9.00 BSC.			BODY SIZE
<div>D1</div>	7.00 BSC.			MATRIX FOOTPRINT
<div>E1</div>	7.00 BSC.			MATRIX FOOTPRINT
MD	8			MATRIX SIZE D DIRECTION
ME	8			MATRIX SIZE E DIRECTION
N	64			BALL COUNT
φb	0.50	0.60	0.70	BALL DIAMETER
<div>eD</div>	1.00 BSC.			BALL PITCH - D DIRECTION
<div>eE</div>	1.00 BSC.			BALL PITCH - E DIRECTION
SD / SE	0.50 BSC.			SOLDER BALL PLACEMENT
	NONE			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 EXCEPT AS NOTED).
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
N IS THE TOTAL NUMBER OF SOLDER BALLS.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- NOT USED.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

3623 \ 16-038.12 \ 1.16.07

5. Revision History

Section	Description
Revision 01 (March 5, 2007)	
	Initial release.
Revision 02 (March 9, 2007)	
WP# Hardware Protection	Added section
Connection Diagrams & Physical Dimensions	Modified graphics <i>FAA064 Connection Diagram 64-Ball BGA 10 mm x 13 mm</i> and <i>LAA064 Connection Diagram 64-Ball Fortified BGA</i>
Revision 03 (July 5, 2007)	
Revision History	Modified section to include Revision 2
Ordering Options	Added 110 ns options
Revision 04 (October 22, 2007)	
Ordering Options	Deleted Leaded package offerings
Revision 05 (October 27, 2008)	
WP# Hardware Protection	Modified section
Revision 06 (May 27, 2009)	
Ordering Option	Added LAE064
Connection Diagrams	Added LAE064
Revision 07 (November 17, 2010)	
Connection Diagrams	Removed A22 from FAA064 and LAA064 Connection Diagrams.

Document History Page

Document Title: S29GL-N, 64-Mbit/32-Mbit S Models, 3 V, Flash Memory with Page Mode, featuring 110 nm MirrorBit® Process Technology Document Number: 002-01079				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	—	SITA	03/05/2007	Initial release.
*A	—	SITA	03/09/2007	WP# Hardware Protection: Added section Connection Diagrams & Physical Dimensions: Modified graphics FAA064 Connection Diagram 64-Ball BGA 10 mm x 13 mm and LAA064 Connection Diagram 64-Ball Fortified BGA
*B	—	SITA	07/05/2007	Revision History: Modified section to include Revision 2 Ordering Options: Added 110 ns options
*C	—	SITA	10/22/2007	Ordering Options: Deleted Leaded package offerings
*D	—	SITA	10/27/2008	WP# Hardware Protection: Modified section
*E	—	SITA	05/27/2009	Ordering Option: Added LAE064 Connection Diagrams: Added LAE064
*F	—	SITA	11/17/2010	Connection Diagrams: Removed A22 from FAA064 and LAA064 Connection Diagrams. Obsolete document.
*G	5815932	NFB / PRIT	07/13/2017	Reactivate document. Updated to new template. Completing Sunset Review.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2007–2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.