Supplement

32-Mbit, 3.3V, Dual Boot, Simultaneous Read/Write, Burst Flash

General Description

The Infineon S29CL032J device is a floating gate product fabricated in 110-nm process technology. This burst mode flash device is capable of performing simultaneous read and write operations with zero latency on two separate banks. This product can operate up to 62 MHz and use a single 3.0V to 3.6V that makes it ideal for today's demanding automotive applications.

Distinctive Characteristics

- Single or 3.3V for Read/Program/Erase
- 110-nm Floating Gate Technology
- Simultaneous Read/Write Operation with Zero Latency
- x32 Data Bus
- Dual Boot Sector Configuration (top and bottom)
- Flexible Sector Architecture
  - Eight 2K double word, sixty-two 16K double word, and eight 2K double word sectors
- Versatile I/O Control (1.65V to V_{CC})
- Programmable Burst Interface
  - Linear for 2-, 4-, and 8-double word burst with wrap around
- Secured Silicon Sector that can be either factory or customer locked
- 20 Year Data Retention (typical)
- Cycling Endurance: 1,000,000 Write Cycles per Sector (typical)
- Command Set Compatible with JEDEC (JC42.4) Standard
- Supports Common Flash Interface (CFI)
- Persistent and Password Methods of Advanced Sector Protection
- Unlock Bypass Program Command to reduce programming time
- Write Operation Status Bits indicate program and erase operation completion
- Hardware (WP#) Protection of two outermost sectors in the large bank
- Ready/Busy (RY/BY#) output indicates data available to system
- Suspend and Resume Commands for Program and Erase Operation

Performance Characteristics

Read Access Times	
Speed Option (MHz)	**62**
Maximum Asynchronous Access Time, ns (t_{ACC})	54
Maximum Synchronous Latency, ns (t_{IACC})	54
Maximum Synchronous Burst Access, ns (t_{BACC})	8
Maximum CE# Access Time, ns (t_{CE})	54
Maximum OE# Access time, ns (t_{OE})	20

Current Consumption (Max. Values)	
Continuous Burst Read @ 62 MHz	90 mA
Program	50 mA
Erase	50 mA
Standby Mode	60 µA

Typical Program and Erase Times	
Double Word Programming	18 µs
Sector Erase	1.0 s

Features

The S29CL032J flash device is a Burst mode, dual boot, simultaneous read/write flash memory with VersatileI/O manufactured on 110-nm process technology.

The S29CL032J is a 32-Mb, 3.3V-only, single-power-supply, burst mode flash memory device that can be configured for 1,048,576 double words and can be programmed in standard Flash programmers.

To eliminate bus contention, each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls. Additional control inputs are required for synchronous burst operations: Load Burst Address Valid (ADV#), and Clock (CLK).

The device requires only a single 3.3V-only (3.00V – 3.60V) for both read and write functions. A 12.0V V_{PP} is not required for program or erase operations, although an acceleration pin is available if faster programming performance is required.

The device is entirely command set compatible with the JEDEC single-power-supply flash standard. The software command set is compatible with the command sets of the 5V Am29F and 3V Am29LV flash families. Commands are written to the command register using standard micro-processor write timing. Register contents serve as inputs to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other flash or EPROM devices.

The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

The **Simultaneous Read/Write architecture** provides simultaneous operation by dividing the memory space into two banks. The device can begin programming or erasing in one bank, and then simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The device provides a 256-byte **Secured Silicon Sector** with an one-time programmable (OTP) mechanism.

In addition, the device features several levels of sector protection, which can disable both the program and erase operations in certain sectors or sector groups: **Persistent Sector Protection** is a command sector protection method that replaces the old 12V controlled protection method; **Password Sector Protection** is a highly sophisticated protection method that requires a password before changes to certain sectors or sector groups are permitted; **WP# Hardware Protection** prevents program or erase in the two outermost 8KB sectors of the larger bank.

The device defaults to the Persistent Sector Protection mode. The customer must then choose if the Standard or Password Protection method is most desirable. The WP# Hardware Protection feature is always available, independent of the other protection method chosen.

The **VersatileI/O (V_{IO})** feature allows the output voltage generated on the device to be determined based on the V_{IO} level. This feature allows this device to operate in the 1.8V I/O environment, driving and receiving signals to and from other 1.8V devices on the same bus.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, by reading the DQ7 (Data# Polling), or DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **Sector Erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware Data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **Password and Software Sector protection** feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system at V_{CC} level.

The **Program/Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **Hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic Sleep mode**. The system can also place the device into the **Standby mode**. Power consumption is greatly reduced in both these modes.

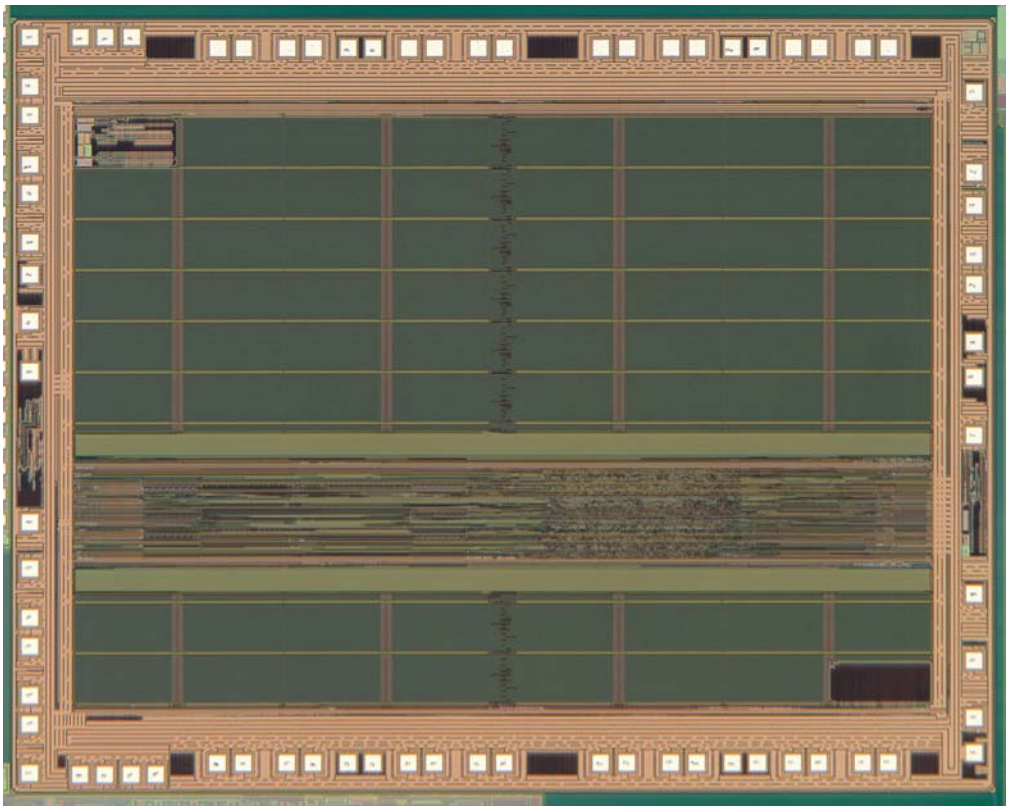
Infineon flash technology combines years of flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

Electrical Specifications

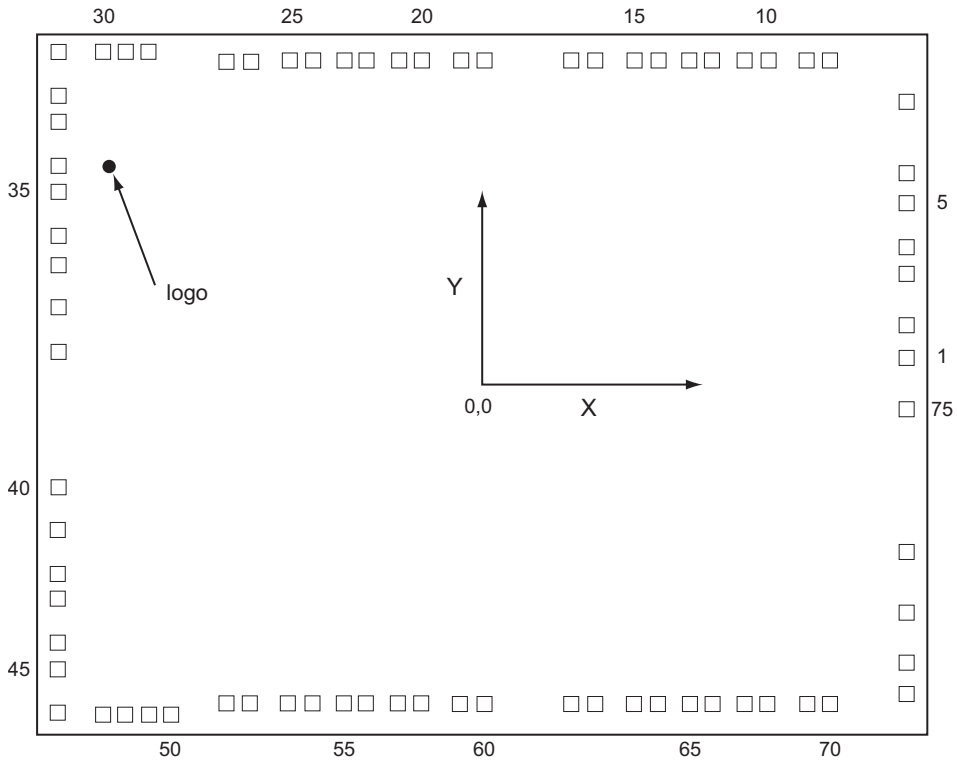
Refer to the *"S29CD032J, S29CD016J, S29CL032J, S29CL016J, 32/16 Mbit, 2.6/3.3 V, Dual Boot, Simultaneous Read/Write, Burst Flash Datasheet (002-00948)"*, for full electrical specifications on the S29CL032J in Known Good Die (KGD) / Known Good Wafer (KGW) form.

Table of Contents

1 Die Photograph



2 Die Pad Locations



3 Pad Description

Table 3-1 Pads Relative to Die Center

Pad Description – Coordinates are relative to die center											
Pad	Signal	Mils		µm		Pad	Signal	Mils		µm	
		X	Y	X	Y			X	Y	X	Y
1	V_{SS}	86.792	5.256	2204.513	133.494	39	V_{CC}	–87.202	6.415	–2214.935	162.944
2	V_{CC}	86.792	11.7	2204.513	297.189	40	A9	–87.202	–21.357	–2214.935	–542.469
3	CE#	86.792	22.321	2204.513	566.951	41	A10	–87.202	–29.891	–2214.935	–759.231
4	OE#	86.792	27.775	2204.513	705.48	42	A11	–87.202	–38.96	–2214.935	–989.577
5	WE#	86.792	36.844	2204.513	935.826	43	A12	–87.202	–44.227	–2214.935	–1123.356
6	WP#	86.792	42.931	2204.513	1090.448	44	A13	–87.202	–53.295	–2214.935	–1353.703
7	IND/WAIT#	86.792	57.644	2204.513	1464.159	45	A14	–87.202	–58.562	–2214.935	–1487.482
8	DQ16	70.902	65.866	1800.915	1672.988	46	A15	–87.202	–67.631	–2214.935	–1717.828
9	DQ17	66.137	65.866	1679.885	1672.988	47	A16	–77.993	–67.901	–1981.026	–1724.687
10	DQ18	58.032	65.866	1474.001	1672.988	48	A17	–73.43	–67.901	–1865.126	–1724.687
11	DQ19	53.267	65.866	1352.971	1672.988	49	A18	–68.665	–67.901	–1744.096	–1724.687
12	V_{IO}	46.741	65.866	1187.215	1672.988	50	A19	–64.102	–67.901	–1628.196	–1724.687
13	V_{SS}	42.079	65.866	1068.798	1672.988	51	DQ0	–52.715	–65.841	–1338.968	–1672.352
14	DQ20	35.575	65.866	903.602	1672.988	52	DQ1	–47.95	–65.841	–1217.938	–1672.352
15	DQ21	30.81	65.866	782.572	1672.988	53	DQ2	–39.845	–65.841	–1012.054	–1672.352
16	DQ22	22.704	65.866	576.688	1672.988	54	DQ3	–35.08	–65.841	–891.024	–1672.352
17	DQ23	17.939	65.866	455.658	1672.988	55	V_{IO}	–28.554	–65.841	–725.268	–1672.352
18	DQ24	0.248	65.866	6.289	1672.988	56	V_{SS}	–23.892	–65.841	–606.851	–1672.352
19	DQ25	–4.517	65.866	–114.741	1672.988	57	DQ4	–17.388	–65.841	–441.655	–1672.352
20	DQ26	–12.623	65.866	–320.625	1672.988	58	DQ5	–12.623	–65.841	–320.625	–1672.352
21	DQ27	–17.388	65.866	–441.655	1672.988	59	DQ6	–4.517	–65.841	–114.741	–1672.352
22	V_{IO}	–23.914	65.866	–607.411	1672.988	60	DQ7	0.248	–65.841	6.289	–1672.352
23	V_{SS}	–28.576	65.866	–725.829	1672.988	61	DQ8	17.939	–65.841	455.658	–1672.352
24	DQ28	–35.08	65.866	–891.024	1672.988	62	DQ9	22.704	–65.841	576.688	–1672.352
25	DQ29	–39.845	65.866	–1012.054	1672.988	63	DQ10	30.81	–65.841	782.572	–1672.352
26	DQ30	–47.95	65.866	–1217.938	1672.988	64	DQ11	35.575	–65.841	903.602	–1672.352
27	DQ31	–52.715	65.866	–1338.968	1672.988	65	V_{IO}	42.101	–65.841	1069.358	–1672.352
28	A0	–68.665	67.926	–1744.096	1725.324	66	V_{SS}	46.763	–65.841	1187.776	–1672.352
29	A1	–73.43	67.926	–1865.126	1725.324	67	DQ12	53.267	–65.841	1352.971	–1672.352
30	A2	–77.993	67.926	–1981.026	1725.324	68	DQ13	58.032	–65.841	1474.001	–1672.352
31	A3	–87.202	67.913	–2214.935	1725.001	69	DQ14	66.137	–65.841	1679.885	–1672.352
32	A4	–87.202	58.845	–2214.935	1494.654	70	DQ15	70.902	–65.841	1800.915	–1672.352
33	A5	–87.202	53.578	–2214.935	1360.875	71	V_{IO}	86.792	–64.051	2204.513	–1626.885
34	A6	–87.202	44.509	–2214.935	1130.529	72	RESET#	86.792	–57.564	2204.513	–1462.136
35	A7	–87.202	39.242	–2214.935	996.75	73	CLK	86.792	–47.015	2204.513	–1194.169
36	A8	–87.202	30.173	–2214.935	766.403	74	RY/BY#	86.792	–34.691	2204.513	–881.144

Pad Description

Table 3-1 Pads Relative to Die Center (Continued)

Pad Description – Coordinates are relative to die center											
Pad	Signal	Mils		µm		Pad	Signal	Mils		µm	
		X	Y	X	Y			X	Y	X	Y
37	V_{SS}	–87.202	24.25	–2214.935	615.942	75	ADV#	86.792	–5.467	2204.513	–138.852
38	ACC	–87.202	15.677	–2214.935	398.202						

4 Ordering Information

The order number (Valid Combination) is formed by the following:

S29CL032J 0N D K H 03 7

Packing Type
7 = Waffle Pack (42 per waffle pack tray)
9 = Wafter in Wafer Jar

Additional Ordering Options
15th Character – S29CL032J only:
0 = 7E, 49, 01/00 Autoselect ID
16th Character – Top or Bottom Boot:
3 = Bottom Boot without Simultaneous Operation

Temperature Range
H = Hot (–40°C to +145°C)

Die Thickness
K = 280 µm

Package Type
D = Die
W = Wafer

Clock Frequency
10th Character – Initial Burst Access Delay:
0 = 5-1-1-1, 6-1-1-1, and above
11th Character – Frequency: N = 62 MHz

Device Number/Description
S29CL032J
32-Mbit (1M x 32-Bit) CMOS 3.3 Volt-Only Burst Mode, Dual Boot, Simultaneous Read/Write Flash Memory
Manufactured on 110-nm Floating Gate Technology

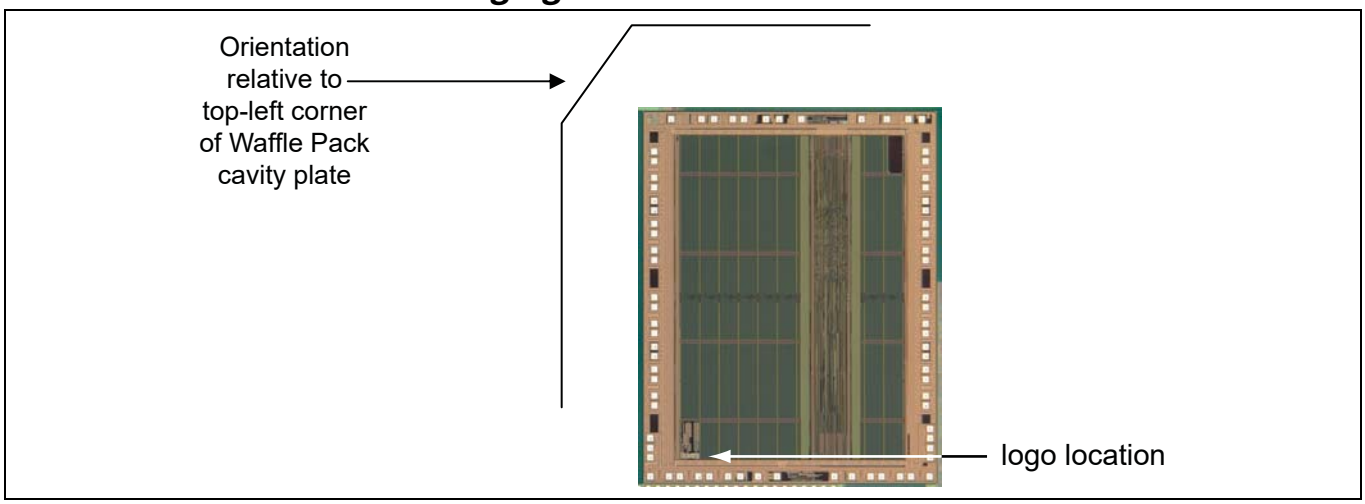
4.1 Valid Combinations

Valid Combinations list the configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 4-1 S29CL032J Valid Combinations

S29CL032J	0N	D	K	H	03	7
S29CL032J	0N	W	K	H	03	9

4.2 Waffle Pack Packaging



5 Product Test Flow

Figure 5-1 provides an overview of Infineon KGD and KGW test flow. For more detailed information, refer to the S29CL032J product Qualification Database. Infineon implements quality assurance procedures throughout the product test flow. These QA procedures also allow Infineon to produce KGD products without requiring or implementing burn-in. In addition, an off-line quality monitoring program (QMP) further guarantees Infineon quality standards are met on KGD products.

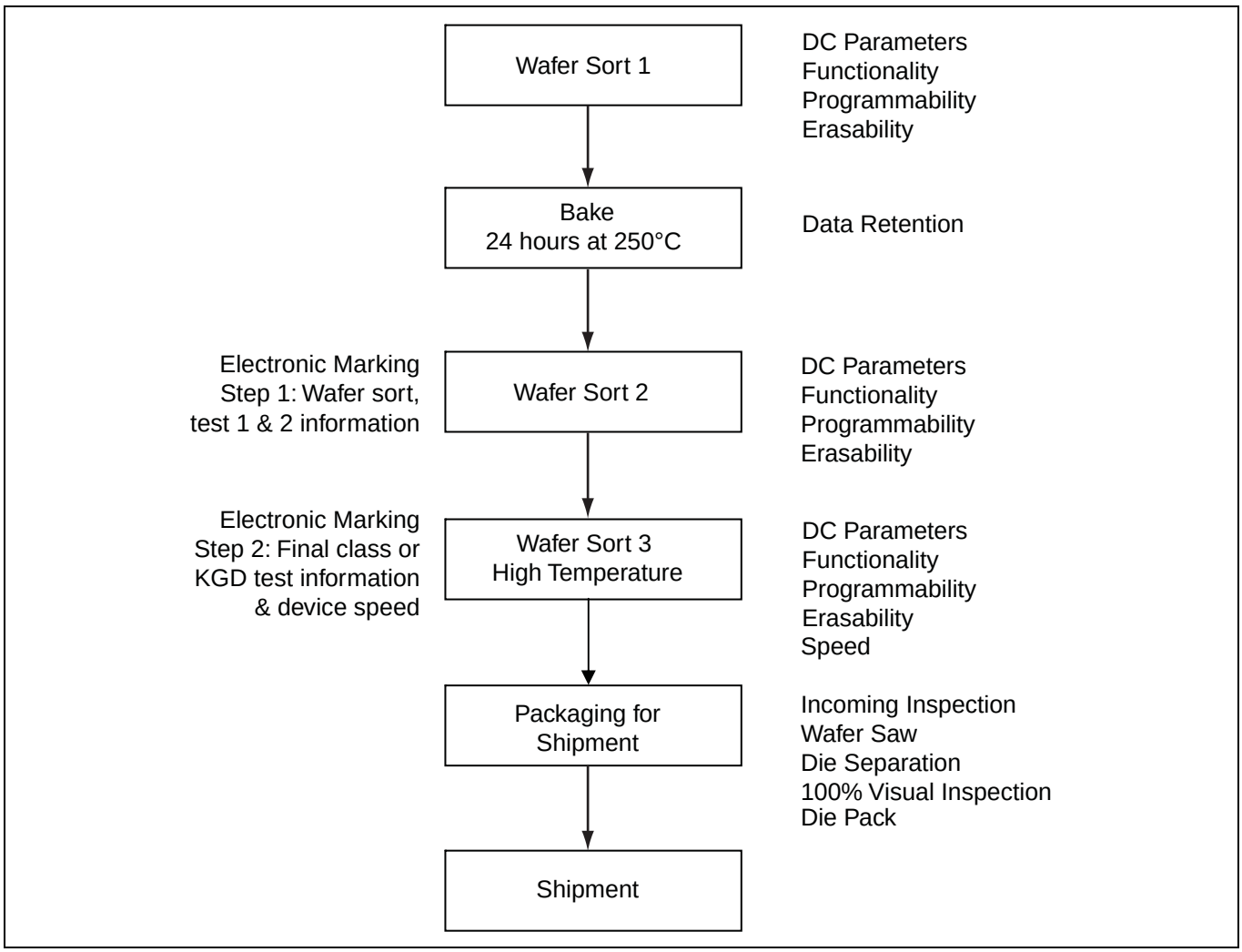


Figure 5-1 Infineon KGD/KGW Product Test Flow

Electronic marking is programmed into every KGD for the purpose of traceability. The electronic marking contains wafer lot number, wafer number of origin, die location on the wafer, mask revision, test program revision, test dates, and speed grade. **Figure 5-1** illustrates the steps where specific electronic marking information is programmed.

6 Absolute Maximum Ratings

Table 6-1 Absolute Maximum Ratings

Parameter		Rating
Storage Temperature		–65°C to +150°C
Ambient Temperature with Power Applied		–65°C to +145°C
V_{CC}, V_{IO}[1]	S29CL032J	–0.5 V to + 3.6 V
ACC, A9, OE#, and RESET#[2]		–0.5 V to +13.0 V
Address, Data, Control Signals	S29CL032J (with the exception of CLK)[1]	–0.5 V to +3.6 V
Output Short Circuit Current[3]		200 mA

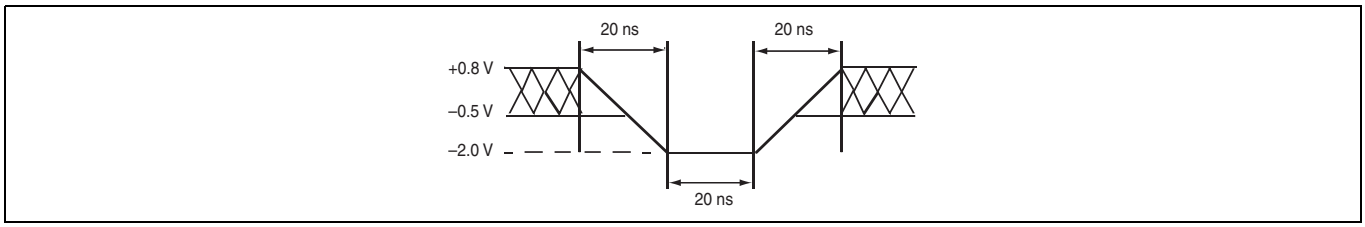


Figure 6-1 Maximum Negative Overshoot Waveform

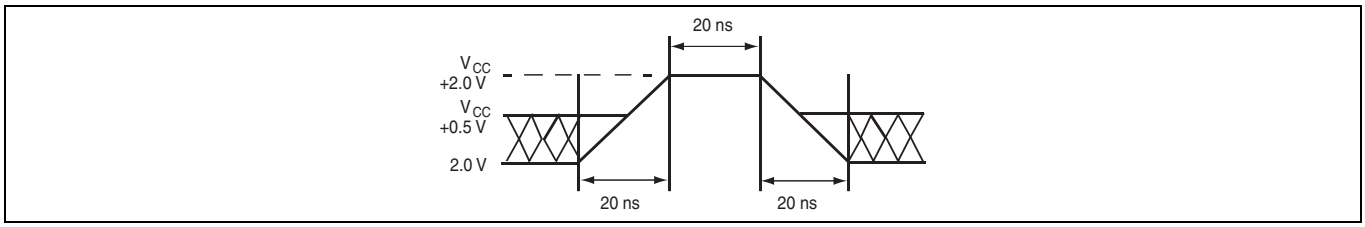


Figure 6-2 Maximum Positive Overshoot Waveform

Notes

1. Minimum DC voltage on input or I/O pins is –0.5V. During voltage transitions, input at I/O pins may overshoot V_{SS} to –2.0V for periods of up to 20 ns. See Figure 6-1. Maximum DC voltage on output and I/O pins is 3.6V. During voltage transitions output pins may overshoot to V_{CC} + 2.0V for periods up to 20 ns.
2. Minimum DC input voltage on pins ACC, A9, OE#, and RESET# is –0.5V. During voltage transitions, A9, OE#, and RESET# may overshoot V_{SS} to –2.0V for periods of up to 20 ns. See Figure 6-2. Maximum DC input voltage on pin A9 and OE# is +13.0V which may overshoot to 13.7V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
4. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

7 Operating Ranges

Table 7-1 Operating Ranges[5]

Parameter		Rating
Ambient Temperature (T_A), Hot Range		–40°C to +145°C
V_{CC} Supply Voltage for regulated voltage range	S29CL032J	3.0 V to 3.6 V
V_{IO} Supply Voltage		1.65 V to V_{CC}

8 Physical Specifications

Table 8-1 Physical Specifications

Specification	Value
Die Dimensions	4.70 x 3.78 mm
Die Thickness	280 µm
Bond Pad Size	80 x 80 µm
Pad Area Free of Passivation	5,776 μm^2
Pads Per Die	75
Bond Pad Metalization	Al/Cu
Passivation	$Si0_2$/SiN

9 Manufacturing Information

Table 9-1 Manufacturing Information

Item Description		Location/Data
Manufacturing Location		Fab 25, TX
Test Location		PNG
Shipment Preparation Location		Penang, Malaysia
Manufacturing ID (Bottom Boot)	S29CL032J	98N06A2B
Fabrication Process		CS69S
Die Revision		1

Note
5. Operating ranges define those limits between which the functionality of the device is guaranteed.

10 Special Handling Instructions

10.1 Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, Infineon recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

10.2 Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

11 DC Characteristics for KGD/KGW Devices at 145°C

Table 11-1 DC Characteristics, CMOS Compatible

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
I_{CC1}	V_{CC} Active Asynchronous Read Current	CE# = V_{IL}, OE#=V_{IL}	1 MHz			10	mA
I_{CC3}	V_{CC} Active Program Current	CE# = V_{IL}, OE#=V_{IH}, ACC = V_{IH}			40	50	mA
I_{CC5}	V_{CC} Standby Current (CMOS)	V_{CC} = V_{CCMAX}, CE# = V_{CC} ± 0.3V				60	µA
I_{CC7}	V_{CC} Reset Current	Reset = V_{IL}				60	µA
I_{CC8}	Automatic Sleep Mode Current	V_{IH} = V_{CC} ± 0.3 V, V_{IL} = V_{SS} ± 0.3V				60	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CCMAX}				±10.0	µA

12 Terms and Conditions of Sale for Infineon Nonvolatile Memory Die

All transactions relating to unpackaged die under this agreement shall be subject to Infineon's standard terms and conditions of sale, or any revisions thereof, which revisions Infineon reserves the right to make at any time and from time to time. In the event of conflict between the provisions of Infineon standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

Infineon warrants its manufactured unpackaged die whether shipped to customer in individual dice or wafer form ("Known Good Die," "KGD", "Die," "Known Good Wafer", "KGW", or Wafer(s)) will meet Infineon published specifications and against defective materials or workmanship for a period of one (1) year from date of shipment.

This limited warranty does not extend beyond the first purchaser of said Die or Wafer(s).

Buyer assumes full responsibility to ensure compliance with the appropriate handling, assembly and processing of KGD or KGW (including but not limited to proper Die preparation, Die attach, backgrinding, singulation, wire bonding and related assembly and test activities), and compliance with all guidelines set forth in Infineon specifications for KGD or KGW, and Infineon assumes no responsibility for environmental effects on KGD or KGW or for any activity of Buyer or a third party that damages the Die or Wafer(s) due to improper use, abuse, negligence, improper installation, improper backgrinding, improper singulation, accident, loss, damage in transit, or unauthorized repair or alteration by a person or entity other than Infineon ("Limited Warranty Exclusions")

The liability of Infineon under this limited warranty is limited, at Infineon option, solely to repair the Die or Wafer(s), to send replacement Die or Wafer(s), or to make an appropriate credit adjustment or refund in an amount not to exceed the original purchase price actually paid for the Die or Wafer(s) returned to Infineon, provided that: (a) Infineon is promptly notified by Buyer in writing during the applicable warranty period of any defect or nonconformity in the Die or Wafer(s); (b) Buyer obtains authorization from Infineon to return the defective Die or Wafer(s); (c) the defective Die or Wafer(s) is returned to Infineon by Buyer in accordance with Infineon shipping instructions set forth below; and (d) Buyer shows to Infineon satisfaction that such alleged defect or nonconformity actually exists and was not caused by any of the above-referenced Warranty Exclusions. Buyer shall ship such defective Die or Wafer(s) to Infineon via Infineon carrier, collect. Risk of loss will transfer to Infineon when the defective Die or Wafer(s) is provided to Infineon carrier. If Buyer fails to adhere to these warranty returns guidelines, Buyer shall assume all risk of loss and shall pay for all freight to Infineon specified location. The aforementioned provisions do not extend the original limited warranty period of any Die or Wafer(s) that has either been replaced by Infineon.

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Known Good Die or Known Good Wafer are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of the die or wafer can reasonably be expected to result in a personal injury. Buyer's use of Known Good Die or Known Good Wafer for use in life support applications is at Buyer's own risk and Buyer agrees to fully indemnify Infineon for any damages resulting in such use or sale.

Revision History

Document Version	Date of Release	Description of Changes
**	10/08/2013	Initial release
*A	11/09/2015	Updated to Cypress template
*B	02/04/2021	Updated to IFX template. Added Known Good Wafer option and OPN.

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