Robustness Against Parasitics By SOI

Monolithic level shifting gate driver ICs suffer heavily from the negative voltage which can occur at the high side reference pin, when standard IC technologies are used. Silicon-on-insulator (SOI) technology, however, provides the robustness to address this behavior. Three half bridge level shifter gate driver ICs are tested under static and transient negative voltage condition. This article discusses the test method and points out the performance of each gate driver IC under the negative voltage condition.

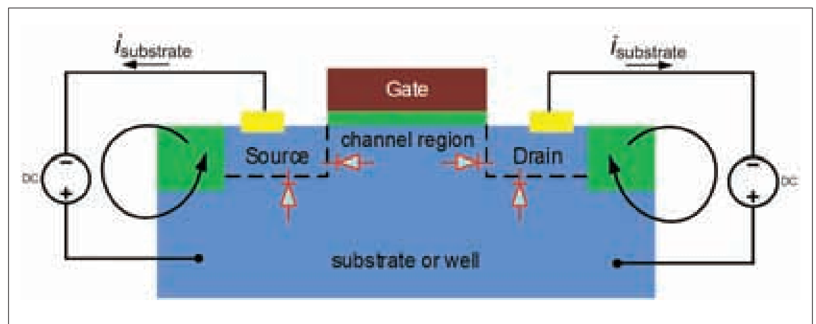
Wolfgang Frank, Jinsheng Song, Infineon Technologies, Neubiberg, Germany

ICs based on standard Silicon technology exhibit low tolerance to negative voltages presented to their inputs and outputs. A small negative voltage in the range of -0.8 to -1 V at one of the IC pins may result in uncontrolled substrate currents. The substrate currents are injected for instance by a forward biased PN junction from substrate to active area according to Figure 1. This usually triggers an undefined IC behavior.

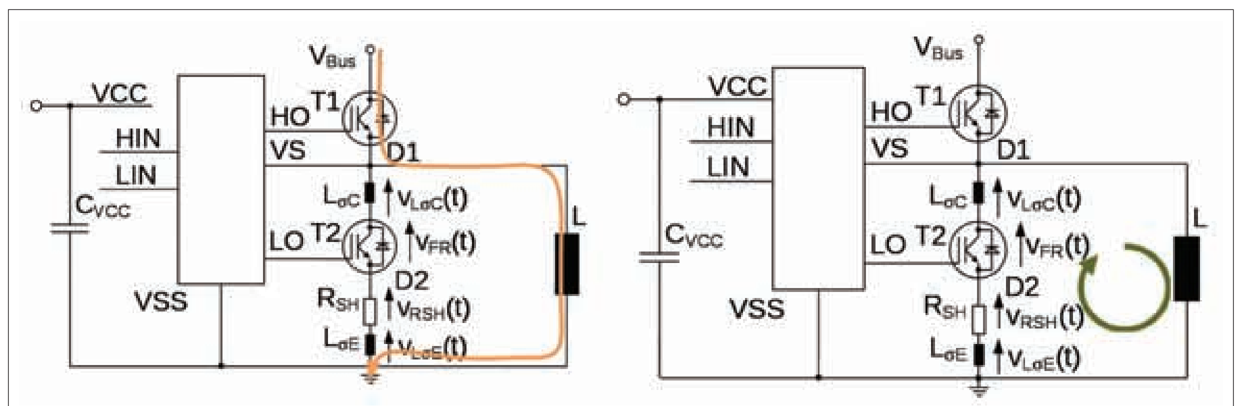
This effect caused by negative voltage transients is particularly pronounced in gate driver ICs. Gate driver ICs are used to control power transistors which operate at high voltages and currents. The switching mode operation of power transistors injects di/dt- or dv/dt-transients. This stimulates resonant circuits consisting of parasitic elements such as stray inductances or coupling capacitances. Oscillations in both, currents and voltages, are the consequence which often exposes gate driver IC terminals to a negative voltage. This can lead to uncontrolled changes of the output states of the gate driver. A latched turn-on state of the gate driver IC can even damage the system. Figure 2 shows examples of a half bridge configuration including its parasitic elements and the voltage which is induced by them.

The half bridge consists of two IGBTs T1 and T2 accompanied by the freewheeling diodes D1 and D2. The half bridge energizes loads such as transformers or electric machines. The load is receiving power from the DC link power supply, when the high side transistor T1 is on according to the left part in Figure 2. When T1 is off, the load current commutates onto the low side portion of the half bridge so that diode D2 conducts the load current as sketched in the right part of Figure 2. Parasitic elements are visible for the low side commutation path only. Similar stray inductances are physically present in the high side path as well.

It can easily be seen that there will be a transient voltage drop over the elements $L_{\sigma C}$, $L_{\sigma E}$, the shunt R_{SH}. Also there is a forward recovery effect of the freewheeling diode D2. All voltage drops result in a negative voltage at terminal VS of the gate driver IC. The amplitude of such negative voltages can reach several 10 V in the system and therefore requires a high robustness of the gate driver IC. Other aspects, such as ground bouncing, also require a high robustness of the IC against



RIGHT Figure 1: Cross section of a transistor structure in bulk technology



BELOW Figure 2: Half bridge configuration with indication of the current path for energizing the load (left) and freewheeling of the inductive load current (right) including the parasitic elements of the low side path

	Infineon 2EDL05N06PF [1]	Device 2	Device 3
Technology	Silicon-On-Insulator	Bulk silicon	Bulk silicon
Isolation level	600V	600V	600V
Isolation method	Level shifter	Level shifter	Level shifter
V_{s_tran} (t < 500ns) [V]	-50	Unknown*	Unknown*
V_{static} [V]	-0.5	-0.3	-0.3
Bootstrapping	Internal diode	Internal FETs	External diode
I_{Opk+} [A]	0.36	0.4	0.35 (min 0.25)
I_{Opk-} [A]	0.70	0.65	0.65 (min 0.5)

* Not specified within the respective product datasheet

LEFT Table 1: **Tested half bridge drivers**

negative voltages at other terminals such as the signal input terminals LIN and HIN. The duration of such transients is related to the time it takes to commutate the current from the high side IGBT T1 into the freewheeling diodes D2. Usually, these negative voltage transients disappear quickly after this period.

This study was performed on various half bridge gate driver ICs. The tested gate drivers and their main operating parameters are listed in Table 1. The parameter list shows that each of the devices is tolerant to negative voltages of various amplitudes and durations. The tests were designed in order to push the tested ICs to their limits and to discover possible anomalies in gate driver operation induced by static and dynamic or pulsed negative voltages.

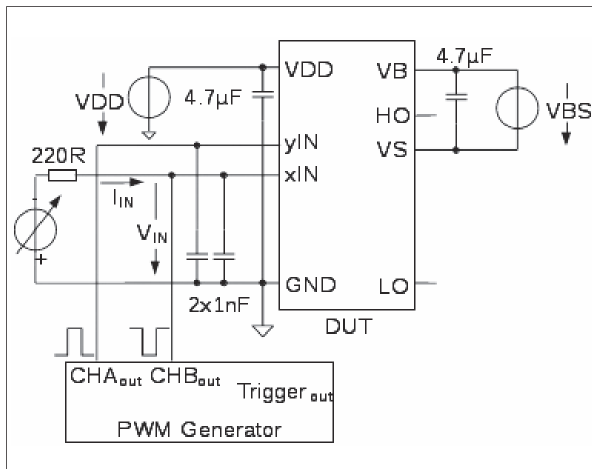


Figure 3: **Simplified test circuit for static tests**

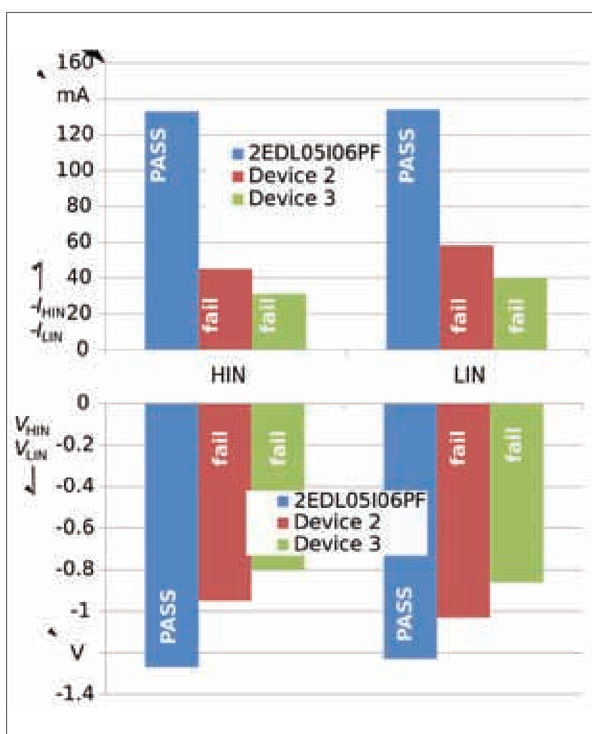


Figure 4: **Test results of static test with negative voltage applied to signal input terminals**

Static tests

The ICs can be exposed to negative voltages statically in case of a malfunction of other circuits. As mentioned above, the driver ICs can also be regularly exposed to short negative pulses as a consequence of transient phenomena. These can have high amplitude up to several tens of volts and usually have a short duration of a few hundreds of nanoseconds. Such pulses can repetitively appear at the terminal VS of the gate driver during a normal circuit operation due to existing parasitic elements as explained in Figure 2. In both cases the driver ICs should be able to maintain a normal operation without a malfunction in order to prevent damage to the power devices.

The static tests were performed using the circuit given in Figure 3. The IC is supplied from a 15 V source to enable the operation of the gate driver outputs. The acceptance criterion of the test is the uninterrupted transmission of the continuous PWM input signals to the related output. Any kind of latch state of any output will lead to “fail”.

The static test injects a voltage to the input signal terminals for the low side

output or the high side output according to Figure 3. The negative voltage opens a path from ground to the input terminals either by means of forward biased PN-junctions in case of bulk technologies or by discrete clamping diodes in case of SOI. The clamping therefore has a diode characteristic.

Figure 4 shows the fail conditions at the end of the test. The 2EDL05I06PF is the only part, which achieved "PASS" in this test. The negative voltage for this part is approximately V_{IN} = -1.25 V for terminal HIN and LIN. The injected input current exceeds I_{IN} = -130 mA. The test had been stopped in order to avoid a thermal overstress of the clamping diode structure.

Device 2 shows faulty behavior once the negative voltage at the inputs reaches about V_{IN} = -1.0 V. The failure mode observed can be both, latch-on and latch-off. It is important to note that the latch states are occurring randomly. Even more critical is the fact that even the not tested channel can latch as well. Thus, the high side output HO latches when the low side input LIN is under test and vice versa. The device 3 also shows unstable behavior. This occurs at approximately V_{IN} = - 0.8 V. The injected current is only about I_{IN} = -40 mA. The result also is a latched output similar as with device 2; the outputs may latch either on or off.

Dynamic tests

The dynamic tests were performed using the circuit given in Figure 5. The negative pulses were applied directly at terminal VS of the device under test as these are most likely the ones where such a high amplitudes and short durations of the negative pulses occur. The input side of the DUT was supplied by signals from a PWM generator.

The IC is supplied from two 15 V power supplies V_{DD} and V_{BS} to establish a normal circuit operation. The second power supply V_{BS} is required since the bottom switch in the phase arm is not available for bootstrapping and the IC is not affected by any bootstrapping activity. The bottom switch was replaced by a pull down resistor in order to enable suitable injection of negative voltages to the terminal VS during intervals when the bottom switch is supposed to be on. The PWM generator was manually triggered to generate a sequence of nine pulses. The fifth pulse in the sequence is triggering the second pulse generator which is used to drive the negative voltage. This synchronization is done to maintain the negative pulse generation to the time interval when the upper switch is turned off. During the on-state of IGBT T1 in Figure 5, the voltage on VS is clamped to the DC link voltage of 100 V. The injection of negative voltages is therefore restricted. The amplitude of the negative pulse is controlled by the voltage supply -VN whereas the duration of the pulse is controlled by settings of the pulse generator. The amplitude of the pulse is varied from -10 to -60 V; the duration of the pulse varies between 50 and 600 ns.

The test pulse configuration is shown in Figure 6. The negative pulse is applied in the moment just after the turn-off of the upper switch. This pulse configuration was chosen because in a practical application it is most probable that negative voltage pulses would be injected into terminal VS in this instant due to changes of the power devices' switching states and freewheeling effects. The delay Δt as well as the pulse width T_{PW} of the negative pulse are varied in a wide range when the DUT revealed sensitivity to negative pulses further away from the switching transitions. This is done to include cases when the negative pulses are generated in rather remote locations within the power circuit, for example in other circuit phases.

The acceptance criteria for all the tests is the undisturbed transmission of the input PWM signal from the input terminals LIN and HIN to the outputs LO and HO, respectively.

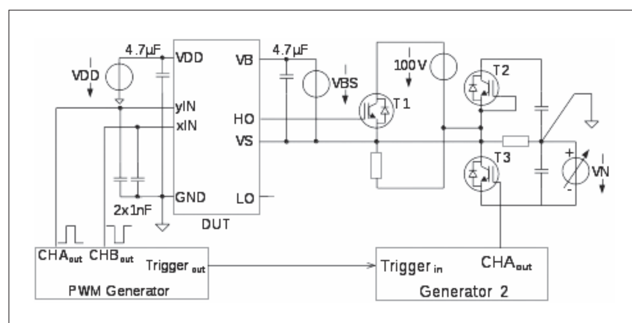


Figure 5: Simplified test circuit for dynamic tests

Test results

The 2EDL05I06PF performed in the tests without any critical observation. The high side output reacts after the IC´s turn-off propagation delay $t_{pd(off)}$. This is followed by the decrease of the emitter voltage due to the pull-down resistor being connected to the emitter of transistor T1 according to Figure 5. The negative pulse of the duration T_{PW} is applied after the interval Δt right after the turn-off of T1. There are no anomalies detected in the driver function.

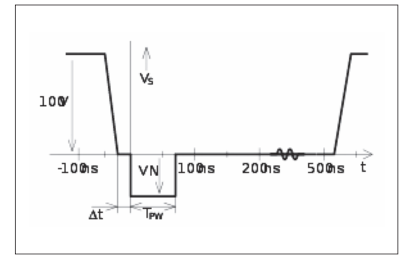


Figure 6: Test pulse configuration, negative pulse at turn-off of the upper switch

Device 2 behaves as expected at negative pulses with amplitudes higher than –20 V respectively pulses shorter than approximately 400 ns. In case of pulses with lower amplitude or longer duration, the high side output HO tends to change from Low state to High state even if not requested by the input signal.

Device 3 performed well in the test. Anomalies were detected in the driver function when the negative pulse exceeds -50 V and 500 ns.

Conclusion

Three level shifter half bridge driver ICs with focus on the negative voltage influence were compared in this article The executed tests include static tests and dynamic or pulse tests in order to cover various situations which can occur in practical applications. The Silicon-On-Insulator (SOI) technology is stable during operation even under statically applied negative voltages. From the test results presented, it can be concluded that the SOI-based 2EDL05I06PF gate driver IC outperforms other driver ICs based on conventional bulk silicon technology regarding negative voltage immunity. SOI-Technology eases the designers challenge to create robust power electronic devices and inherently leads to more reliable designs.

Literature

Frank W., Song J., SOI technology provides robustness against parasitic elements injecting negative voltages, Proceedings PCIM Europe 2015