Isolated 48 V to 12 V 275 W eighth-brick converter using digital controller XDPP1100-Q024

275 W half-bridge center-tap rectifier voltage mode control

About this document

Scope and purpose

This document describes Infineon's XDPP1100-based 48 V to 12 V eighth-brick demo board. The purpose is to demonstrate the capability of the XDP™ IDC digital controller in a typical eighth-brick telecom application.

Intended audience

This document is intended for power supply engineers using XDP™ IDC, who need training in the flexibility and features that this digital IC offers in PWM DC-DC brick converter designs.

Table of contents

1 Introduction

This document describes the design and performance of a digitally controlled 275 W half-bridge center-tap (HB-CT) rectification converter with Voltage Mode Control (VMC). The eighth-brick has a main power stage which converts 36 V to 75 V to 12 V output, and an auxiliary power supply to provide bias voltage for primary gate driver, secondary gate driver and 3.3 V VDD. The XDPP1100 is a digital controller based on a 32-bit, 100 MHz ARM® Cortex™-M0 RISC microprocessor with analog/mixed-signal capabilities. The digital controller provides the utmost flexibility in design and efficiency optimization. This evaluation unit follows the DOSA mechanical outline for eighth-bricks.

The main Infineon components used in the 275 W digital HB-CT eighth-brick are:

- XDPP1100 digital controller
- DHP1050N10N5 OptiMOS™ HB complete power stage (drivers and 100 V, 5 mΩ FETs)
- 80 V OptiMOS™ 5, BSC040N08NS5, 80 V 4 mΩ, SuperS08 power transistors
- EiceDRIVER™ 2EDN7524G, Infineon's dual-channel gate driver

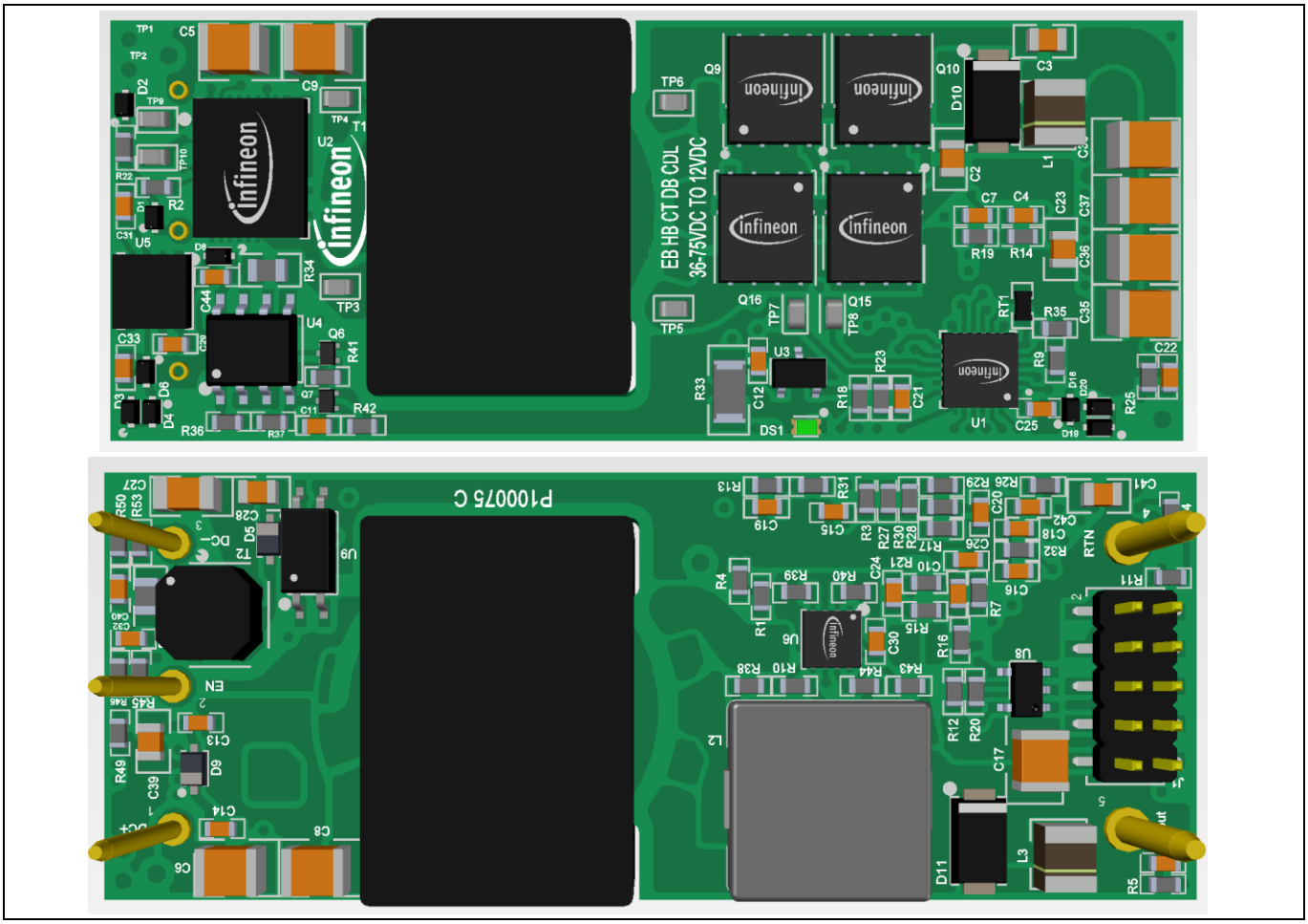


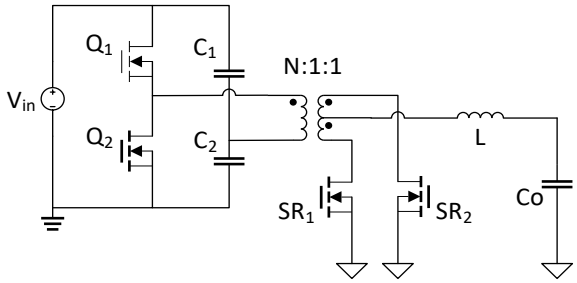
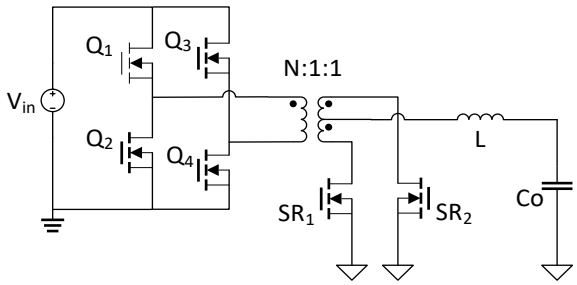
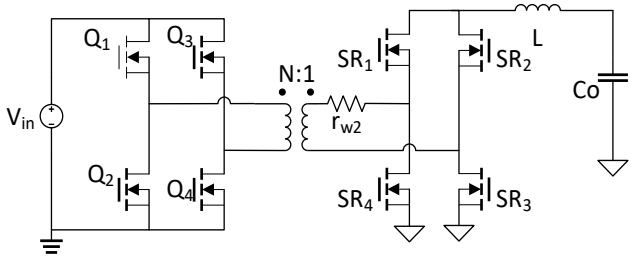
Figure 1 Infineon 275 W digital HB-CT eighth-brick evaluation unit outline

2 Background and system description

The trend in SMPS in recent years has been toward increased power density with optimized cost. **Table 1** shows the comparison of major topologies of the telecom bricks that convert 48 V input to 12 V output.

High efficiency is a key parameter in achieving this increasing power density because the heat dissipation must be minimized. Furthermore, higher efficiency directly impacts the ownership cost during the lifetime of the converter. Toward this goal, HB-CT rectification topology is considered to be the best approach for the power range 120 W to 300 W.

Table 1 Major topologies of telecom bricks (quarter-brick and eighth-brick)

Topology	Circuit	Cost/complexity	Efficiency	Output power
HB-CT		Excellent, low component count on both primary and secondary	Medium	120 W to 300 W
FB-CT		Medium, the secondary driver is reference to ground	High	300 W to 600 W
FB-FB		High, both primary and secondary are HB type	Highest	600 W to 800 W

2.1 System description

The 275 W isolated HB-CT eighth-brick DC-DC converter is a new generation of digitally controlled DC-DC power module designed to support telecom 12 V DC intermediate bus applications. The Infineon evaluation unit operates from an input voltage range of 36 V DC to 75 V DC and provides up to 275 W output power. Note, below 42 V DC the converter will lose 12 V DC regulation and will drop to around 10.8 V at 36 V input. But it still provides the same output current. The output is fully isolated from the input, allowing versatile polarity configurations and grounding connections to the input and output terminals. The 275 W digital HB-CT eighth-brick design consists of a primary-side HB converter with Synchronous Rectification (SR) in CT configuration switching at 250 kHz, with an Infineon-designed CDL lossless snubber used on the secondary side. The DHP1050N10N5 is an integrated power stage with a HB driver and two 100 V/5 mΩ MOSFETs in one package.

The dual low-side gate driver 2EDN7524G is used to drive the secondary SR MOSFETs, as shown in the block diagram in **Figure 2**.

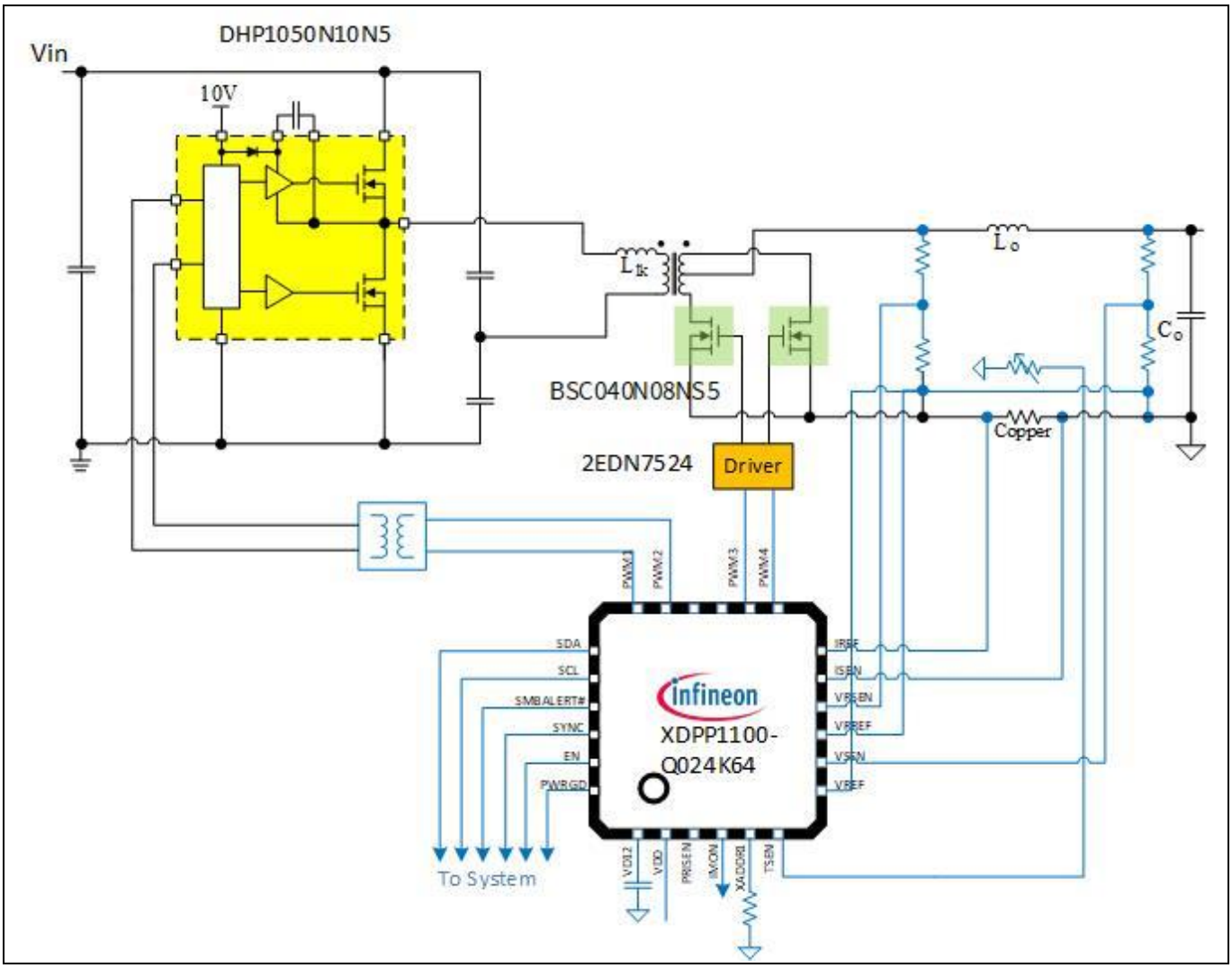


Figure 2 Infineon 275 W digital HB-CT evaluation board – simplified block diagram

The loop control is implemented with Infineon XDPP1100. The XDPP1100 is a digital power supply controller based on a 32-bit, 100 MHz ARM® Cortex™-M0 RISC microprocessor with analog/mixed-signal capabilities, on-chip memories and communication peripherals. The device is specifically optimized to enhance the performance of isolated DC-DC applications and reduce the solution component count in the telecom brick converters. It has a -40 to 125°C operational temperature range.

The Voltage Sense (VS) ADC is an 11-bit ADC with 50 MHz sampling rate. The ADC resolution is 1.25 mV and enhanced with three-bit digital modulation for output voltage regulation. This gives 156 µV resolution at the sense pin and 1.58 mV resolution at the 12 V output with a scale of 0.099. The hardware resolution limits the highest resolution the board can achieve. Hence, setting PMBus command VOUT_MODE to -10 (resolution 0.976 mV), -11 (resolution 0.488 mV) or -12 (resolution 0.244 mV) will give the same result. This design configures VOUT_MODE = -12.

The voltage ADC is also designed to sense high-frequency switching signals and this makes it a perfect fit to sense the input voltage from the transformer secondary side at the switching node V_{RECT}. This eliminates the use of isolated op-amps or other types of isolator for input voltage sensing. The input voltage is computed based

on the resistor-divider ratio and transformer turns ratio. The information is used for V_{IN} telemetry, protection and Feed-Forward (FF) compensation.

The Current Sense (CS) ADC is a 9-bit ADC with 25 MHz sampling rate. Exceptional noise immunity is achieved by the use of the internal current estimator. Based on the state of the PWM pulse, the controller continuously predicts DC and ripple current. The result of the prediction is combined with the actual measured current to be processed by the controller. Hence, the instantaneous noise in the measurement can be filtered out without losing the valuable ripple current information.

The XDPP1100 has a 9-bit telemetry ADC with a sample frequency of 1 MHz. The telemetry ADC block consists of eight channels and can be configured to digitize voltages, currents, impedance and temperature. The 24-pin version XDPP1100-Q024 has one external temperature sense pin (ATSEN) and supports internal PTAT sensing (ITSEN). In this design, ATSEN senses PCB shunt resistor temperature and is used for CS temperature compensation. ITSEN is used to monitor chip junction temperature.

The XDPP1100-Q024 has one address pin. A resistor between the address pin and ground programs the address offset of the device. The address pin supports an 8-valent or 16-valent address table. When more than one eighth-brick module is connected in parallel, the address offset allows the system to communicate and program multiple devices via the same I^2C bus. The address offset resistor is not populated on the brick board and it is usually programmed by the resistor on the system board.

The outstanding performance of the digital controller, the OptiMOS™ and the planar magnetic construction enables power density in the range of 21 W/cm^3 (350 W/in^3). The board is designed as a testing platform, with easy access to probe test points, and easy reworking/replacement of components.

2.2 Sync rectifier timing

The secondary SR timing is critical in telecom brick design for efficiency optimization. The isolator delay must be taken into account along with the propagation delays in drivers to make sure there is no shoot-through between the primary and the secondary opposite phases. The dead-time of the SR should be set as small as possible, to have the highest efficiency and minimize body diode conduction losses. The ideal gate timing diagram is shown in **Figure 3** and the bad gate timing diagram is shown in **Figure 4** for reference.

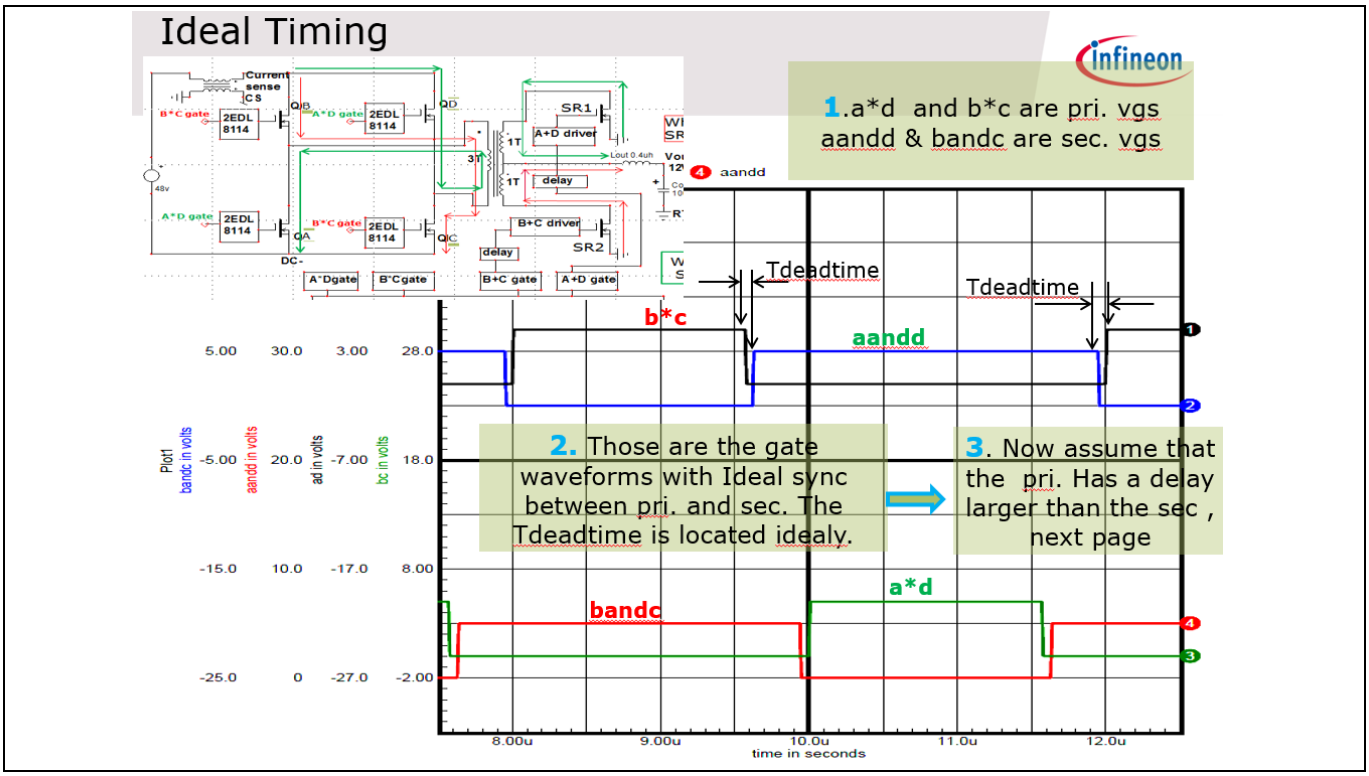


Figure 3 Ideal secondary gate timing example

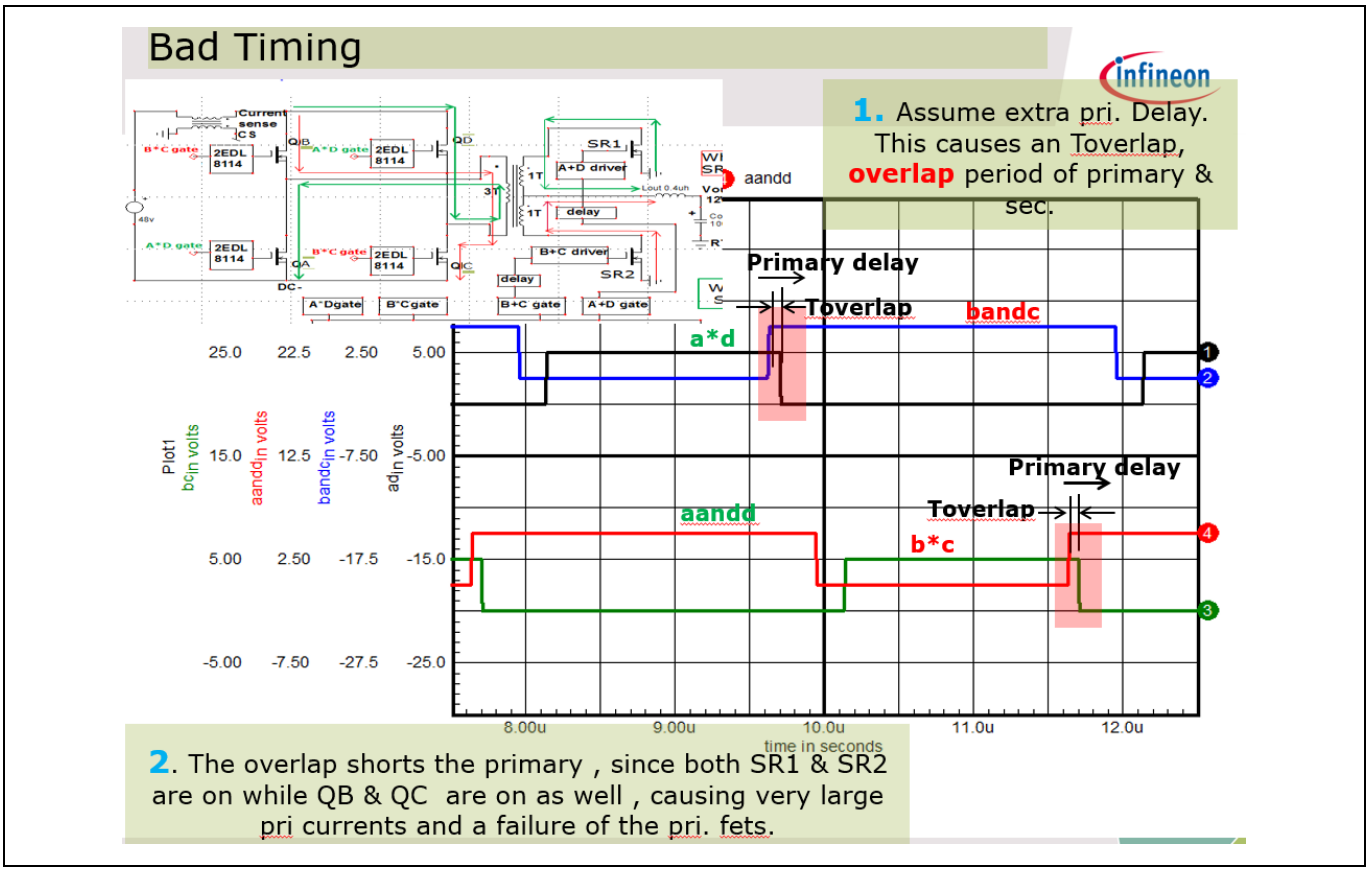


Figure 4 Bad gate timing example

The beauty of digital control is that the parameters can be fine-tuned after the board hardware is fixed. The XDPP1100 enables configuration of the dead-time for each PWM output separately. The rising edge and falling edge delay can be programmed independently – see section 4.1.6 for details. Dynamic dead-time can be implemented by firmware to further improve efficiency over the full load range.

3 Power board information

3.1 Specification

The specification of the 275 W HB-CT board is listed in **Table 2**.

Table 2 Specification

	Min.	Typ.	Max.	Unit
Input voltage range	36	48	75	V
V_{IN} turn-on threshold	32	34	36	V
V_{IN} turn-off threshold	30	32	34	V
Maximum input current (100 percent load, 36 V_{IN})			8	A
No-load input current		160		mA
Off-mode converter input current		20		mA
Output voltage		12		V
Output current			23	A
Output voltage load regulation (V_{IN} = 48 V)		±30	±80	mV
Output voltage line regulation (I_{OUT} = 0 A)		±50		mV
Output voltage regulation over-temperature (V_{IN} = 48 V, T_c = -40°C to 85°C)		±100		mV
Overall output voltage regulation	11.5		12.3	V
Output voltage ripple (peak-to-peak at full load) with overall output capacitance of 1154 µF			120	mV
Recommended output capacitor	100		10000	µF
Load transient (48 V_{IN}, 1000 µF and 154 µF, 1 A/µs) 50 percent to 75 percent load		±300		mV
Load-transient settling time		300		µs
V_{OUT} over-voltage protection		16		V
Switching frequency		250		kHz
External sync. tolerance	-6		6	%
Logic output high	2.6			V
Logic output low			0.4	V
Logic input high	1.2			V
Logic input low			0.8	V
Efficiency at 48 V, full load		95.3		%
Operating temperature (ambient)	-40		80	°C
Isolation voltage		1500		V
Monitoring accuracy – READ_VIN	-2		2	%
Monitoring accuracy – READ_VOUT	-10		10	mV
Monitoring accuracy – READ_IOUT	-1		1	A
Monitoring accuracy – READ_TEMPERATURE	-5		5	°C

3.2 Schematic

Figure 5 is the schematic of the power stage of the 12 V/23 A HB-CT converter. The primary MOSFET is a 100 V/5 mΩ **DHP1050N10N5** integrated symmetrical HB MOSFET with a combination of HB driver based on a bootstrap functionality. The secondary SR uses two 80 V/4 mΩ **BSC040N08NS5** in parallel at each location. The SR MOSFETs are driven by **2EDN7524G**, an advanced dual-channel driver.

A planar transformer is used for the lowest board profile. The transformer core is ML95S EQ20 + plate from Hitachi Metals. The transformer turns ratio is 3:2.

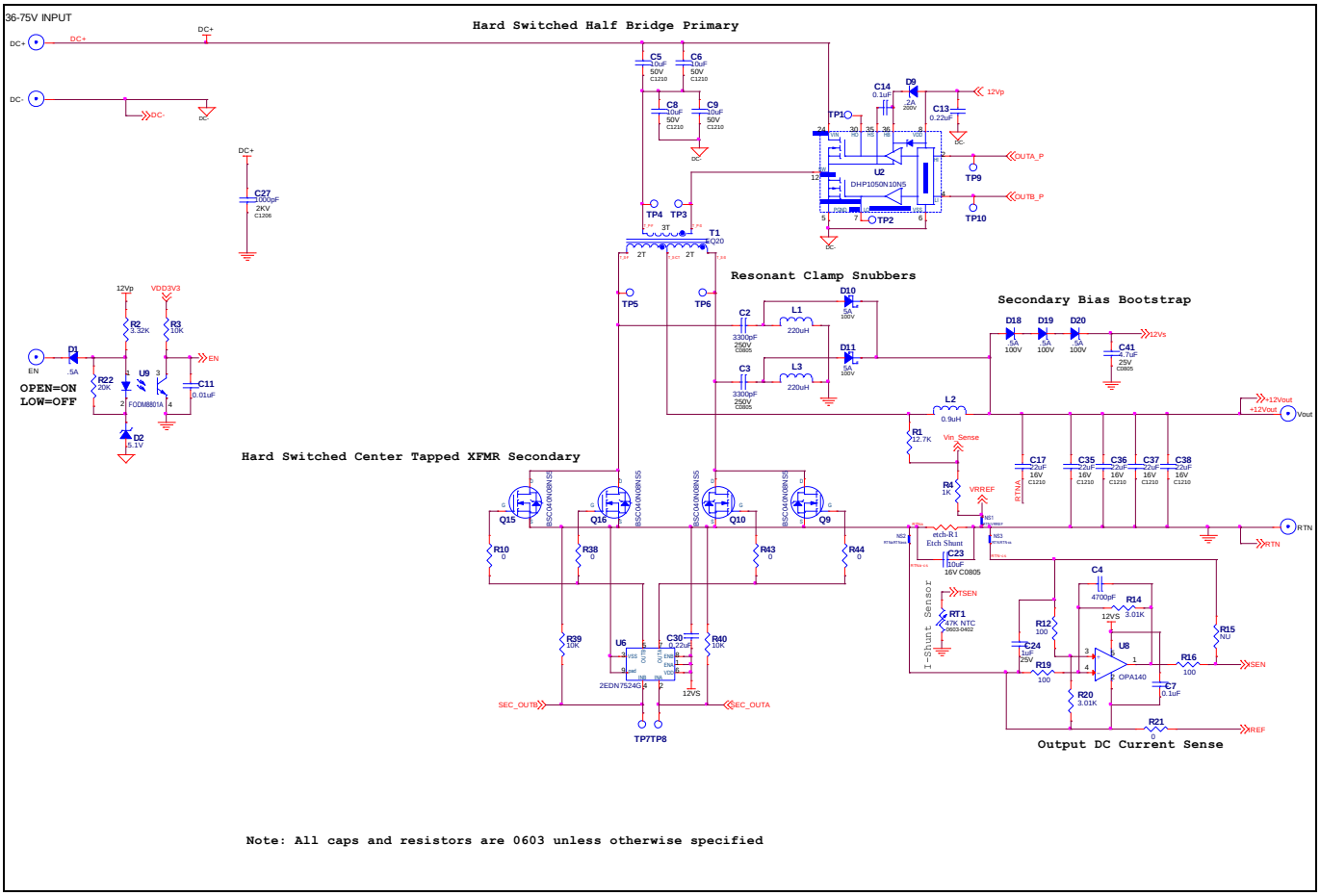


Figure 5 275 W 12 V/23 A HB-CT power-stage schematic

The schematic of the control circuit and auxiliary power supply is shown in **Figure 6**.

In this reference design, the XDPP1100 uses VMC. The output voltage is sensed by VSEN/VREF ADC. The other voltage ADC VRSEN/VRREF is used to sense the input voltage through the transformer secondary winding. There is one high-speed current ADC. AISEN is used to sense the output current.

XDPP1100 devices can be configured with an easy-to-use Graphical User Interface (GUI). The software can be downloaded from the Infineon website.

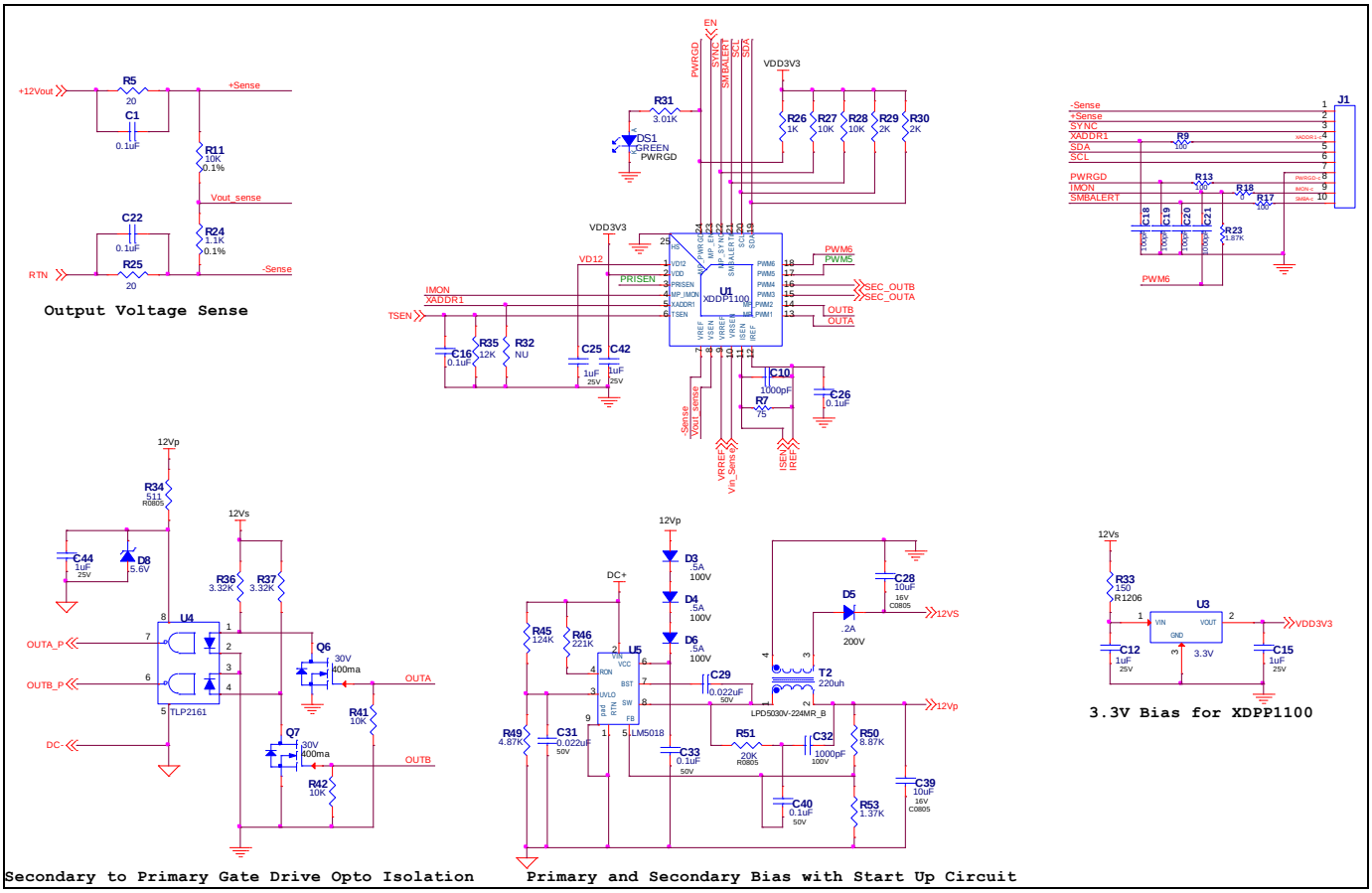


Figure 6 XDPP1100 control circuit

3.3 Test fixture

A test fixture is used as the test plaform for the eighth-brick. It provides power connection terminals, communication and debugging ports, as well as a cooling fan.

Figure 7 shows the schematic of the test fixture. It has an I²C connector for I²C and PMBus communication, and a SWD debugger port for firmware debugging. The fan should be biased with external DC power supply, in the 5 V to 12 V range for different airflow.

Switch SW1 at the primary is the enable switch to turn on the eighth-brick. The brick is enabled when SW1 is turned toward J1. This works with the default setting in the XDPP1100, which configures the enable polarity to “active high”. If EN “active low” is preferred, the user can change the configuration by writing PMBus command ON_OFF_CONFIG. Please note that in this case SW1 turns on the converter when it is flipped toward the edge of the board.

A 3.3 V LDO on the test fixture provides pull-up voltage to the SDA/SCL I²C communication bus provided that 5 to 12 V is applied to the external bias connector.

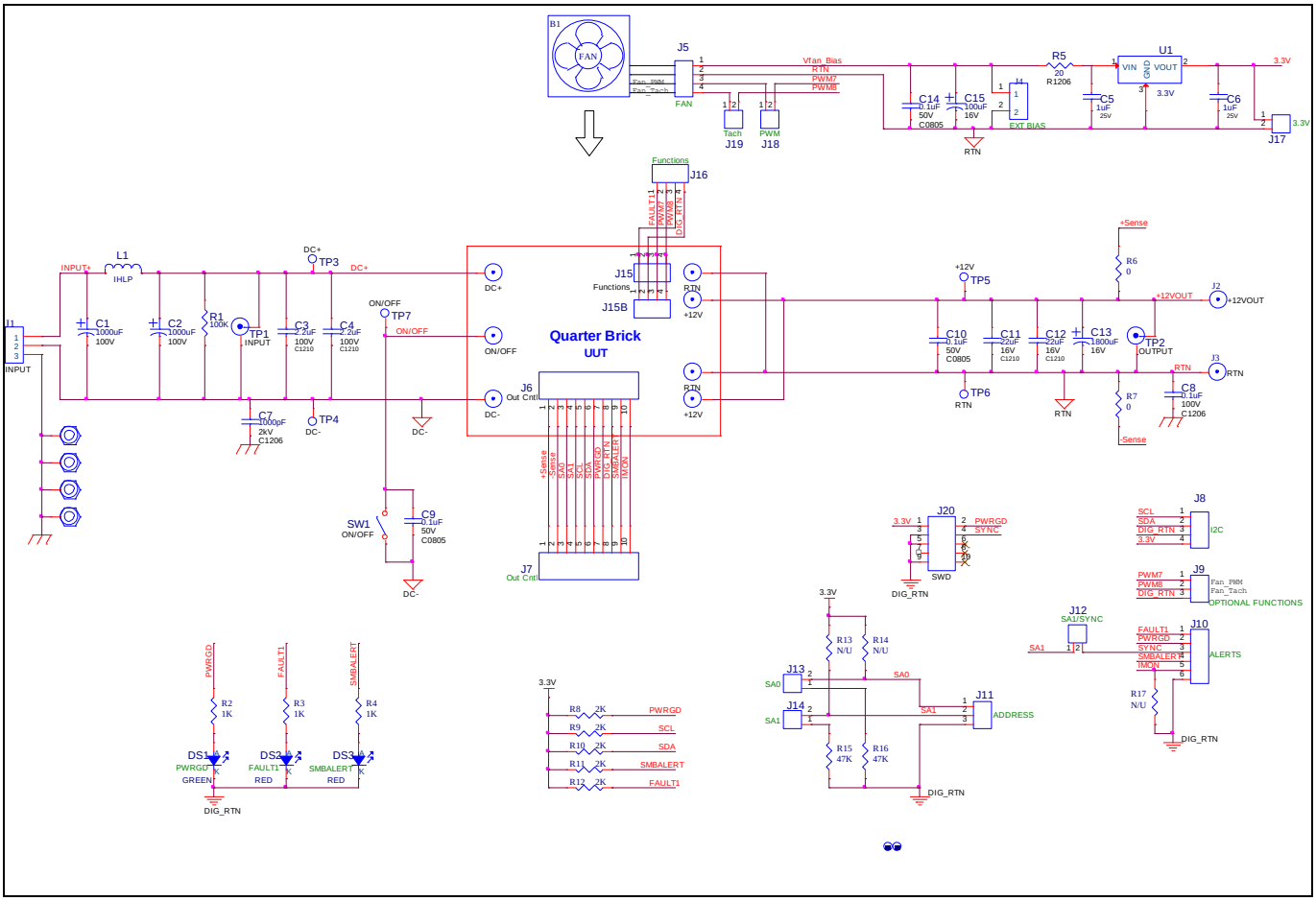


Figure 7 Test fixture schematic

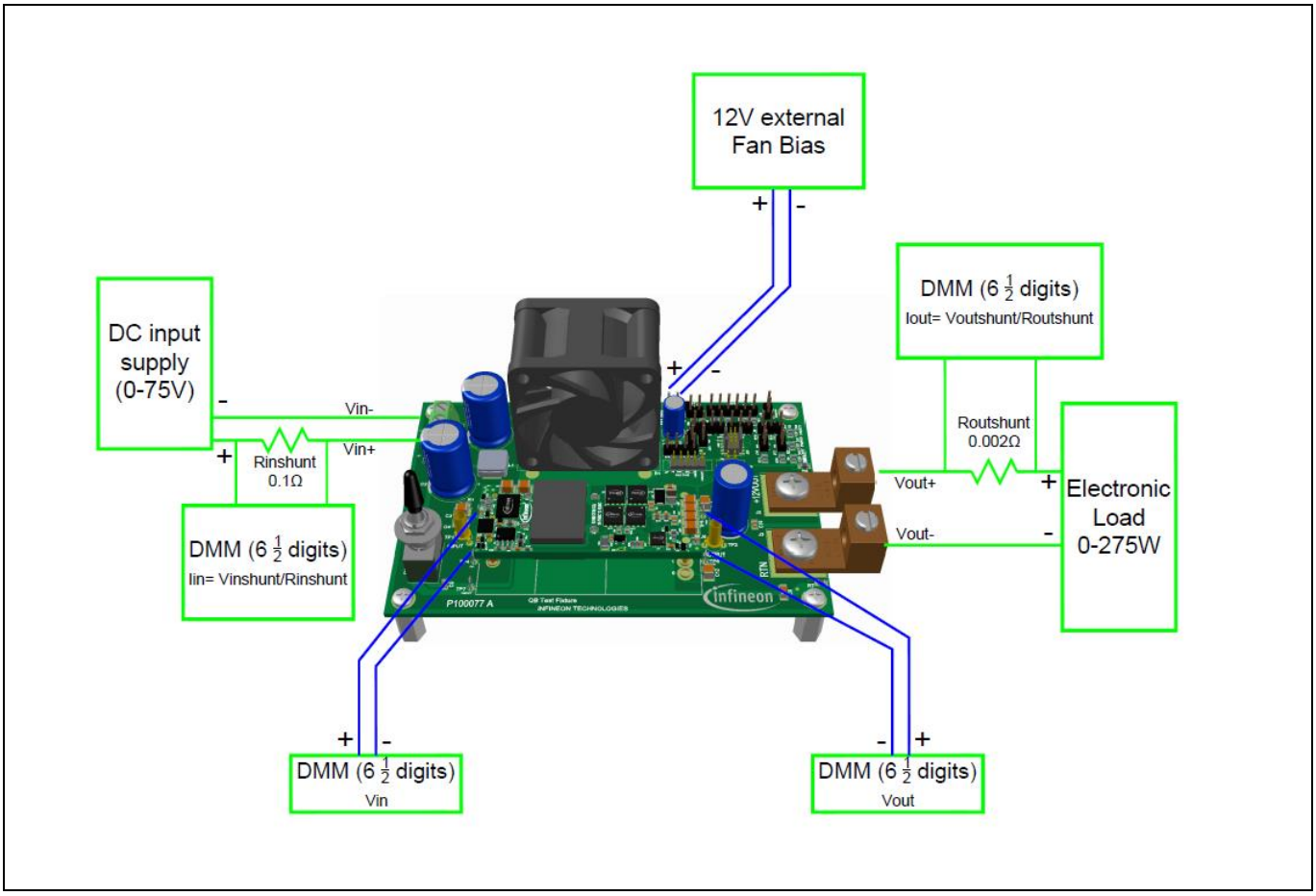


Figure 8 Board connection

Necessary connections to operate the board:

- Connect the eighth-brick to the test fixture. Make sure the DC input, 12 V output and signal connector J6 on the test fixture have good contact.
- Connect 48 V input power supply to J1.
- Connect e-load to J2 and J3.
- Bias fan with 5~12 V DC power supply at J4 (EXT BIAS).
- Conect the XDPP1100 USB dongle (USB007 revA) to J8. Find the direction by identifying the ground pin G (black wire). The blue wire of USB007 is not used and can be left floating.
- Make sure the switch SW1 is in the off position.
- Turn on the 48 V input power supply. A minimum of 35 V is required to enable the auxiliary power supply.
- Measure the secondary 12 VS. It should have 10 V ±1 V output.
- This demo board comes with a default patch and configuration stored in non-volatile memory (OTP) and can be turned on once the operation command is asserted from the XDPP1100 GUI.
- In order to assert the operation command, open XDPP1100 GUI and click on “Auto populate”. The auto populate option is on the top-left corner just below the “file” option.
- Check if the PMBus commands are configured properly by reading VOUT_COMMAND. It should read 12 V.
- Write “ON” to PMBus command 0x01 OPERATION, and turn SW1 to the on position (sequence is not critical). The converter should regulate at 12 V output for an input voltage range of 42 V to 75 V.

3.4 Board layout

The following layout guidelines are recommended for the XDPP1100 controller.

Within the allotted implementation area, orient the switching components first. The switching components are the most critical because they carry large amounts of energy and tend to generate high levels of noise. Switching component placement should take into account power dissipation. Align the output inductors and MOSFETs such that space between the components is minimized.

Critical small-signal components including the VDD and VD12 decoupling capacitors, ISEN resistors, TSEN capacitors, and voltage feedback RC filters should be placed near the controller.

For each VS and CS input, i.e. VSEN/VREF, ISEN/IREF, route the signal and its reference in differential pairs (Kelvin connection).

Avoid routing the VRSEN/VRREF near any switching nodes. Unlike output VS, VRSEN measures pulse signal, and so it can't use a large filter to reduce noise. It is recommended to keep the trace shielded by the ground plane.

Avoid putting the CS resistor or copper shunt next to any switching node. In high-gain CS mode, put the XDPP1100 as close as possible to the sense resistor. One good practice is putting the XDPP1100 on top of the sense resistor on the other side of PCB. If the copper shunt is used for CS, put the temperature sense NTC or sense diode close to the copper shunt for accurate temperature compensation.

If low-gain mode is selected for CS, put the CS amplifier as close as possible to the shunt resistor.

Figure 9 and **Figure 10** are the top and bottom assembly drawings of the HB brick converter with CT full-wave rectification at the secondary side.

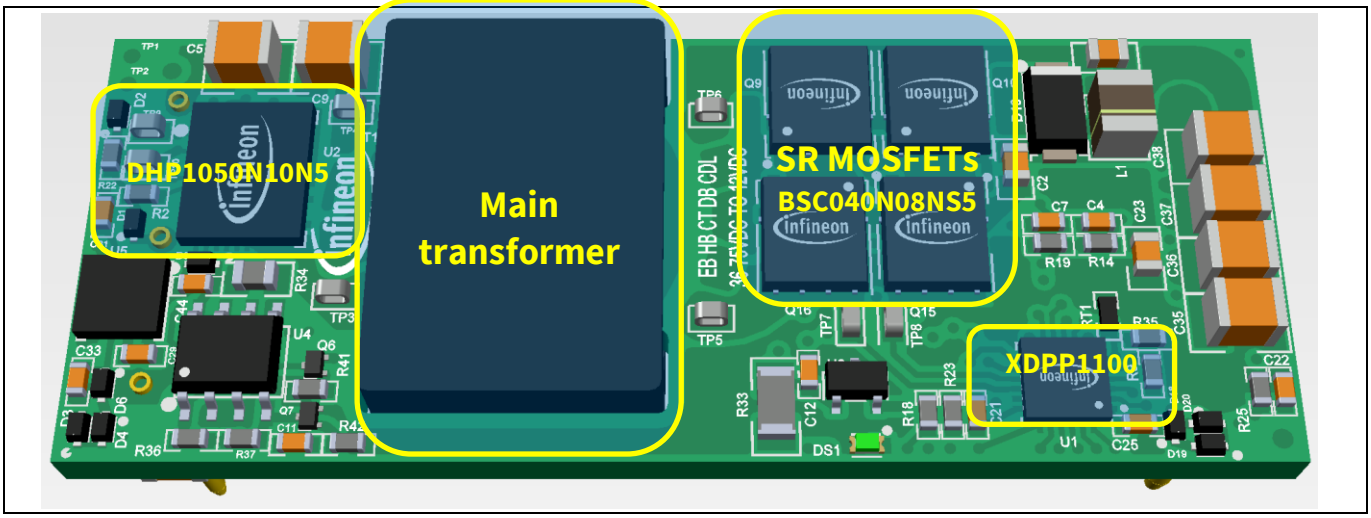


Figure 9 Top assembly

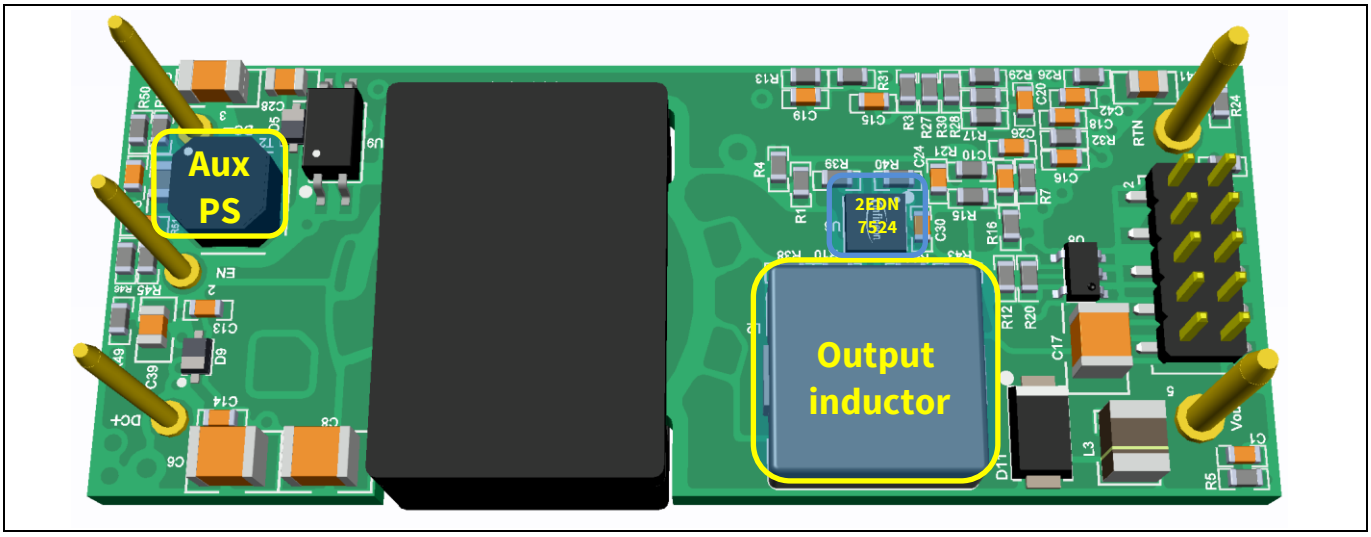


Figure 10 Bottom assembly

3.5 Main transformer

The planar transformer has three turns in primary and two turns in secondary. The primary winding takes layers 1, 4, 5 and 8, one turn per layer. The secondary winding takes layers 2, 3, 6 and 7, one turn per layer. The middle layer has 5 oz. copper and the top and bottom layer have 4 oz. thickness.

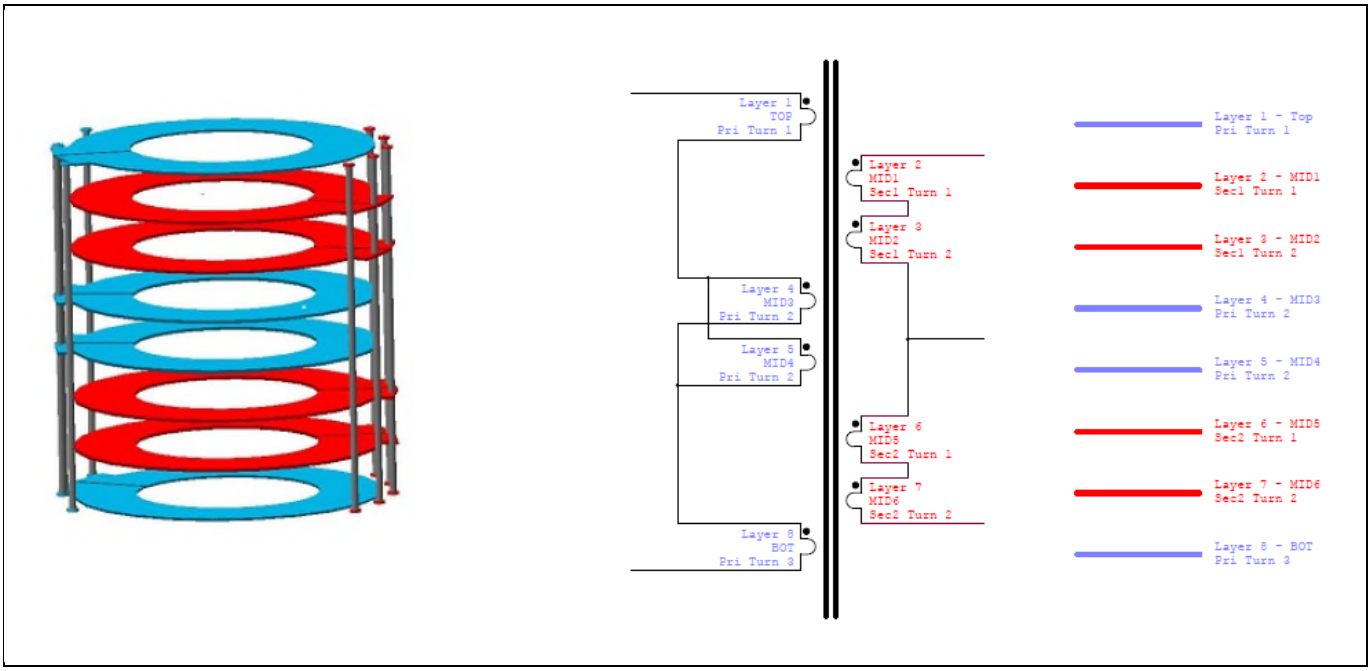


Figure 11 Planar transformer drawing

3.6 Bill of Materials (BOM)

Table 3 BOM

Item	Qty	Ref.	Manufacturer	Part number
1	1	BRD1		P100075 C

Item	Qty	Ref.	Manufacturer	Part number
2	8	C1,C7,C14,C16,C22,C26,C33,C40	TDK	C1608X7R1H104K080
3	2	C2,C3	TDK	C2012C0G2E332K
4	1	C4	TDK	C1608C0G2A472K
5	4	C5,C6,C8,C9	TDK	C3225X7R1H106M250
6	3	C10,C21,C32	TDK	C1608C0G2A102J
7	1	C11	TDK	C1608X7R1H103K080
8	6	C12,C15,C24,C25,C42,C44	TDK	C1608X7R1E105K
9	2	C13,C30	TDK	C1608X7R1H224K080
10	5	C17,C35,C36,C37,C38	TDK	C3225X7R1C226K250
11	3	C18,C19,C20	TDK	C1608C0G2A101K
12	3	C23,C28,C39	Samsung	CL21B106KOQNNNE
13	1	C27	Kemet	C1206C102JGR
14	2	C29,C31	TDK	C1608X7R1H223K080
15	1	C41	TDK	CGA4J1X7R1E475M125
16	1	DS1	Wurth	150060GS75000
17	7	D1,D3,D4,D6,D18,D19,D20	NXP	BAS516,135
18	1	D2	On	MM5Z5V1T1G
19	2	D5,D9	On	BAS20HT1G
20	1	D8	On	MM5Z5V6T1G
21	2	D10,D11	On	NRVTSAF5100ET3G
22	1	J1	Harwin	M22-5320505
23	2	L1,L3	Taiyo Yuden	CBC3225T221KR
24	1	L2	Eaton	HCMA1104-R90-R
25	2	Q6,Q7	Toshiba	SSM3K15AMFV
26	4	Q9,Q10,Q15,Q16	Infineon	BSC040N08NS5
27	1	RT1	Murata	NCP15WB473F03RC
28	1	R1	Panasonic	ERJ-3EKF1272V
29	3	R2,R36,R37	Panasonic	ERJ-3EKF3321V
30	7	R3,R27,R28,R39,R40,R41,R42	Panasonic	ERJ-3EKF1002V
31	2	R4,R26	Panasonic	ERJ-3EKF1001V
32	2	R5,R25	Panasonic	ERJ-3EKF20R0V
33	1	R7	Panasonic	ERJ-3EKF75R0V
34	6	R9,R12,R13,R16,R17,R19	Panasonic	ERJ-3EKF1000V
35	6	R10,R18,R21,R38,R43,R44	Panasonic	ERJ-3GEY0R00V
36	1	R11	Panasonic	ERJ-PB3B1002V
37	3	R14,R20,R31	Panasonic	ERJ-3EKF3011V
38	2	R15,R32	Panasonic	Not used
39	1	R22	Panasonic	ERJ-3EKF2002V
40	1	R23	Panasonic	ERJ-3EKF1871V
41	1	R24	Panasonic	ERA-3AEB112V

Item	Qty	Ref.	Manufacturer	Part number
42	2	R29,R30	Panasonic	ERJ-3EKF2001V
43	1	R33	Panasonic	ERJ-8GEYJ151V
44	1	R34	Panasonic	ERJ-6ENF5110V
45	1	R35	Panasonic	ERJ-3EKF1202V
46	1	R45	Panasonic	ERJ-3EKF1243V
47	1	R46	Panasonic	ERJ-3EKF2213V
48	1	R49	Panasonic	ERJ-3EKF4871V
49	1	R50	Panasonic	ERJ-3EKF8871V
50	1	R51	Panasonic	ERJ-6ENF2002V
51	1	R53	Panasonic	ERJ-3EKF1371V
52	8	TP3,TP4,TP5,TP6,TP7,TP8,TP9,TP10	Harwin	S2761-46R
53	1	T1	Hitachi	EQ20-ML95S Plate
54	1	T2	Coilcraft	LPD5030V-224MR_B
55	1	U1	Infineon	XDPP1100-Q024
56	1	U2	Infineon	DHP1050N10N5
57	1	U3	LT	LT1460KCS3-3.3#TRMPBF
58	1	U4	Toshiba	TLP2161(TP,F)
59	1	U5	TI	LM5018SD/NOPB
60	1	U6	Infineon	2EDN7524G
61	1	U8	TI	OPA140AIDBVT
62	1	U9	Fairchild	FODM8801A
63	3	1,2,3	Mil Max	3104-3-00-15-00-00-08-0
64	2	4,5	Mil Max	4357-0-00-15-00-00-03-0

4 Configuration

The FW patch and optimized configuration are stored in the non-volatile memory OTP. The user could run the demo board without additional configuration by following the instructions in section 3.3. To evaluate the XDPP1100, the user can change configurations such as fault thresholds or response. Most of the configurations can be changed on the fly. The modified configurations are stored in RAM and can be modified unlimited times. On the other hand, the modifications will be lost and reset to the default OTP settings once the input voltage and 3.3 V VDD are removed. To store new configurations to OTP, please refer to the XDPP1100 configuration guide. The “Force i2c/PMBus OK” is not mandatory to be used, as the demo board is shipped with a stored product ID that recognizes the device by using “Auto populate”. Loading the design file EB_HBCT_VMC_XDPP1100 is recommended if the user wants to verify the design tool “PID – Bode Plot”. This is because the load models are not stored in the OTP and won’t be read by the “Auto populate”. The design file will provide information on the load model (such as the output capacitance and ESR) for bode plot emulation.

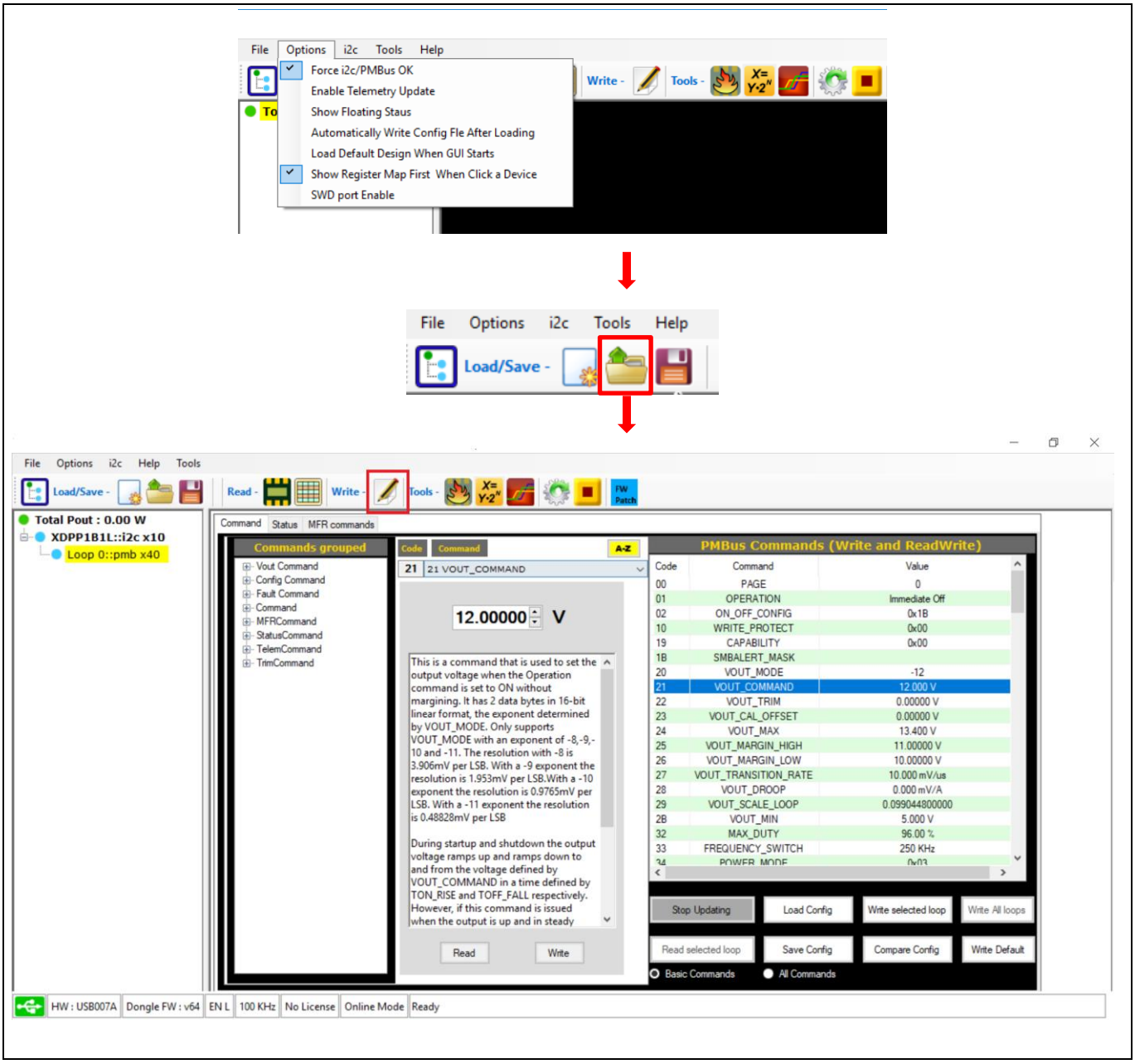


Figure 12 Load design file through GUI

The key PMBus commands are listed in **Table 4.**

4.1 PMBus configuration

Table 4 Basic PMBus configuration (Loop0)

Command	Name	Data	Meaning
00	PAGE	00	0
01	OPERATION	80	On
02	ON_OFF_CONFIG	1F	0x1F
20	VOUT_MODE	18	-12
21	VOUT_COMMAND	0C00	12.000 V
24	VOUT_MAX	0D00	13.400 V
27	VOUT_TRANSITION_RATE	E850	10.000 mV/µs
29	VOUT_SCALE_LOOP	B067	0.0990448000
32	MAX_DUTY	F180	96.00 percent
33	FREQUENCY_SWITCH	087D	250 kHz
34	POWER_MODE	03	0x03
61	TON_RISE	F050	20.000 ms
CD	MFR_VRECT_SCALE		0.071289
CE	MFR_TRANSFORMER_SCALE		0.666016
EA	MFR_IOUT_APC		0.841797

The XDPP1100 is compliant with the PMBus Power System Management Protocol Specification(PSMPS), revision 1.3.1. The standard PMBus commands are not going to be explained here. The Infineon MFR PMBus commands are described in this section.

4.1.1 0xC5 FW_CONFIG_REGULATION

FW_CONFIG_REGULATION (**Figure 13**) configures multi-segment droop parameters and flexible start-up/shutdown functions.

The function of flexible start-up and shutdown includes:

- CURRENT_DOUBLE_ENABLE: Enable secondary current doubler configuration
- EN_BOOST_FEED_FORWARD: Enables feed forward calculation from firmware for buck-boost topology only, reserved for future use and not recommended for current designs
- EN_DE_SHUTDOWN: Enable diode emulation mode (disable SR) during soft-off
- EN_IOUT_APC_TEMP_COMP: Enable temperature compensation of CS
- INTERLEAVE_ENABLE: Enable interleave mode
- EN_DEADTIME_ADJ: Enables changing of dead-time per load current (not implemented in ROM code, but could be implemented by FW patch. Example patch code is available on request)
- EN_VSEN_OPEN_PROTECT: Enable VS pin short/open protection at start-up (not implemented , currently the open sense fault is enabled only by setting the open sense threshold vspX_osp_thresh to non-zero value and not controlled by this bit)
- EN_L_ESTIMATE: Enable inductance estimation at start-up (not implemented)

- EN_C_ESTIMATE: Enable output capacitance estimation at start-up (not implemented)
- EN_ILIM_START-UP: Enable current limit at start-up
- EN_PID_ADJ: Enable PID adjustment at start-up (not implemented)
- EN_PRIM_ISENSE: Enable both ISEN and BISEN channels to support simultaneous primary and secondary current sense on a single loop, single phase topology. It should be enabled in designs that use BISEN in Loop0 such as primary current sensing, but corresponding MFR_IOUT_APC of BISEN should be configured using Loop1 PMBus command.
- EN_DE_START-UP: Enable diode emulation mode (disable SR) during soft-start

The note "not implemented" indicates the function or feature is not implemented in ROM code. The features are reserved to be implemented in the FW patch.

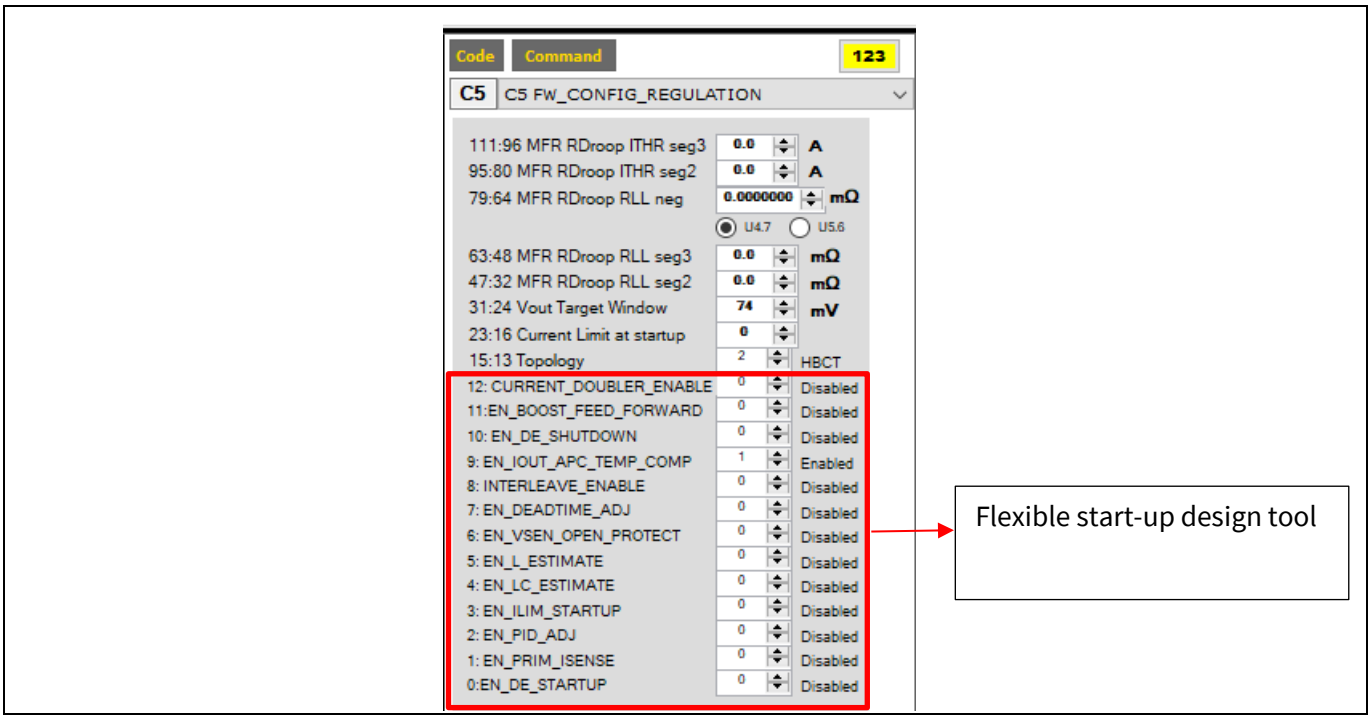


Figure 13 FW_CONFIG_REGULATION

V_{OUT} Target Window (bit 31:24): Defines the SR enabling threshold during DE start-up. If EN_DE_START-UP is set to 1, the SR gate will be held low during soft-start until output voltage approaches target V_{OUT}. The SR gate will be enabled at VOUT_COMMAND minus V_{OUT}_Target_Window.

Current limit at start-up (bit 23:16): Defines start-up clamping current in amps.

This demo board uses PCB copper trace to sense output current. To compensate for the temperature drift of the copper resistance, set bit [9] to 1 to enable the adjustment of IOUT_APC (see 4.1.7) based on the temperature obtained by READ_TEMPERATURE_1 (see 4.1.8). The temperature compensation feature is implemented in the ROM with a fixed coefficient of 0.0039. A different temperature coefficient could be used by overwriting the ROM code with a FW patch.

4.1.2 0xCA MFR_IOUT_OC_FAST_FAULT_RESPONSE

The MFR_IOUT_OC_FAST_FAULT_RESPONSE command instructs the device on action to be taken in response to a fast output over-current fault (when exceeding 0xD1 MFR_IOUT_OC_FAST_FAULT_LIMIT). Unlike the

regular I_{OUT} OC fault response, the I_{OUT} OC fast-fault response only supports two types of response: “continuous to operate (Constant Current)” and “shut down and retry”.

4.1.3 0xD1 MFR_IOUT_OC_FAST_FAULT_LIMIT

This command defines the threshold of fast over-current protection. Similar to the regular over-current protection, this protection is also based on output average current, but with no filter to the signal, so it could act faster. The fast over-current fault response is configured by PMBus command 0xCA MFR_IOUT_OC_FAST_FAULT_RESPONSE.

4.1.4 0xCD MFR_VRECT_SCALE

MFR_VRECT_SCALE is calculated based on V_{RECT} resistor-divider (R1, R4).

4.1.5 0xCE MFR_TRANSFORMER_SCALE

MFR_TRANSFORMER_SCALE is the transformer turns ratio, equal to N_s/N_p. Here $N_p = 3$, $N_s = 2$.

4.1.6 0xCF PWM_DEADTIME

Dead-time can be set in the XDPP1100 GUI design tools, under the Device Topology tool (**Figure 14**) or using PMBus command 0xCF PWM_DEADTIME. Dead-time is set by adding a delay to the rising edge or falling edge of each PWM output. The dead-time of PWM rise and fall time can be configured separately. In most situations only dead-time at the rising edge needs to be set. The maximum dead-time can be set to 318.75 ns with a resolution of 1.25 ns. When dead-time is configured, please consider the isolator delay, which will be added to the primary PWMs.

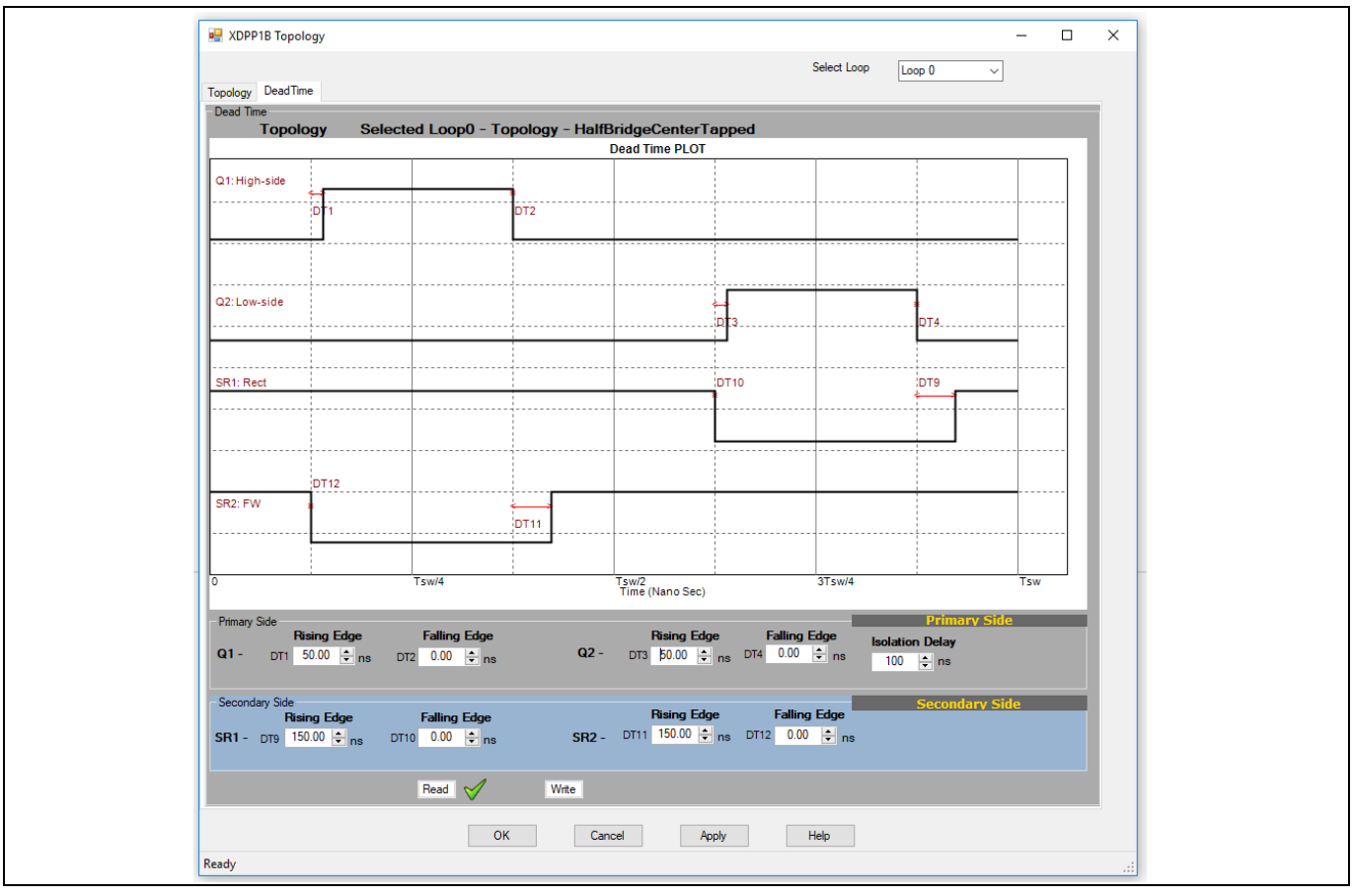


Figure 14 Design tool set dead-time

Figure 15 shows PMBus command 0xCF PWM_DEADTIME to configure dead-time. Only the active PWMs in the selected loop can be configured and they are highlighted using different colors.

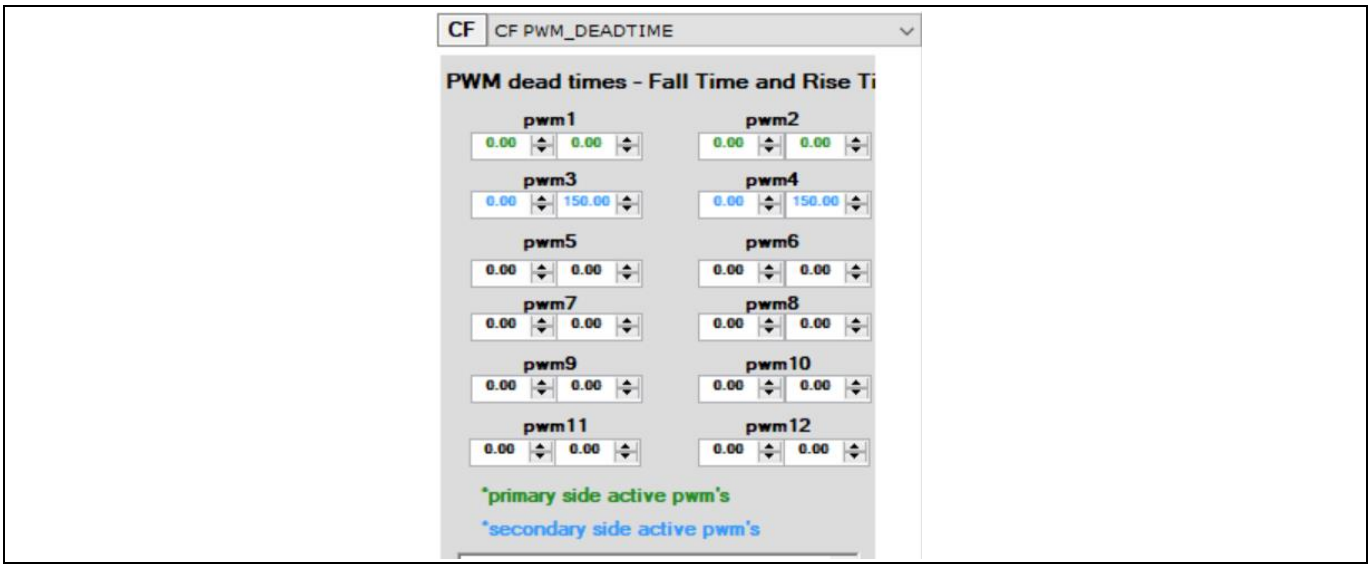


Figure 15 PWM_DEADTIME

4.1.7 0xEA MFR_IOUT_APC

MFR_IOUT_APC (Ampere Per Code) defines the CS gain. The calculation of MFR_IOUT_APC is:

$$MFR\_IOUT\_APC = ISEN\_LSB/R_{sns}$$

The ISEN_LSB is the resolution of I_{ADC} which is determined by the isenX_gain_mode register. XDPP1100 offers two levels of gain: 100 µV and 1.45 mV, with reference to ground (GND); and one IPS mode whose resolution is 1.45 mV and is referenced to a DC bias range from 1.11 V to 1.6 V. The gain mode is configured by register isen_gain_mode. In this demo, the ISEN_LSB is set to 1.45 mV, GND (isen1_gain_mode = 2).

The secondary current is sensed by PCB copper trace (0.134747 mΩ). The signal is very small and an external op-amp (U8) is used to amplify the signal with a gain of 31.1. The signal is then divided by R16 and R7 at the input of XDPP1100. Thus the equivalent secondary sense resistor is 0.134747*31.1 = 4.191 mΩ. This implies that for a current of 1 A, the amplifier output is 4.191 mV. The voltage at the sense pin of the controller after resistor-divider (R16, R7) is 1.796 mV. Hence, the secondary IOUT_APC = 1.45 mV/1.796 mV = 0.80735. Based on the parasitic's effect, IOUT_APC to 0.841797 is adjusted for more accurate output current telemetry.

Please note the PCB trace resistance varies from board to board across a wide range. The IOUT_APC of each board should be calibrated per actual measurement.

4.1.8 0xDC MFR_SELECT_TEMPERATURE_SENSOR

Use MFR_SELECT_TEMPERATURE_SENSOR to configure the temperature sensor. The XDPP1100 supports both external temperature sensing and internal temperature sensing for protection and monitoring. External temperature sensing is performed with a 47 kΩ NTC thermistor, in parallel with a 12 kΩ resistor that is connected between ATSEN and ground.

This demo uses ATSEN to sense PCB temperature near the CS copper. It is used to compensate for CS resistor value. This temperature sensor must be mapped to READ_TEMPERATURE_1 for temperature compensation and over-temperature protection.

The board also uses ITSEN to sense the internal controller temperature. Use the "Fault source select" drop-down menu in order to choose "tempi" as the fault source.

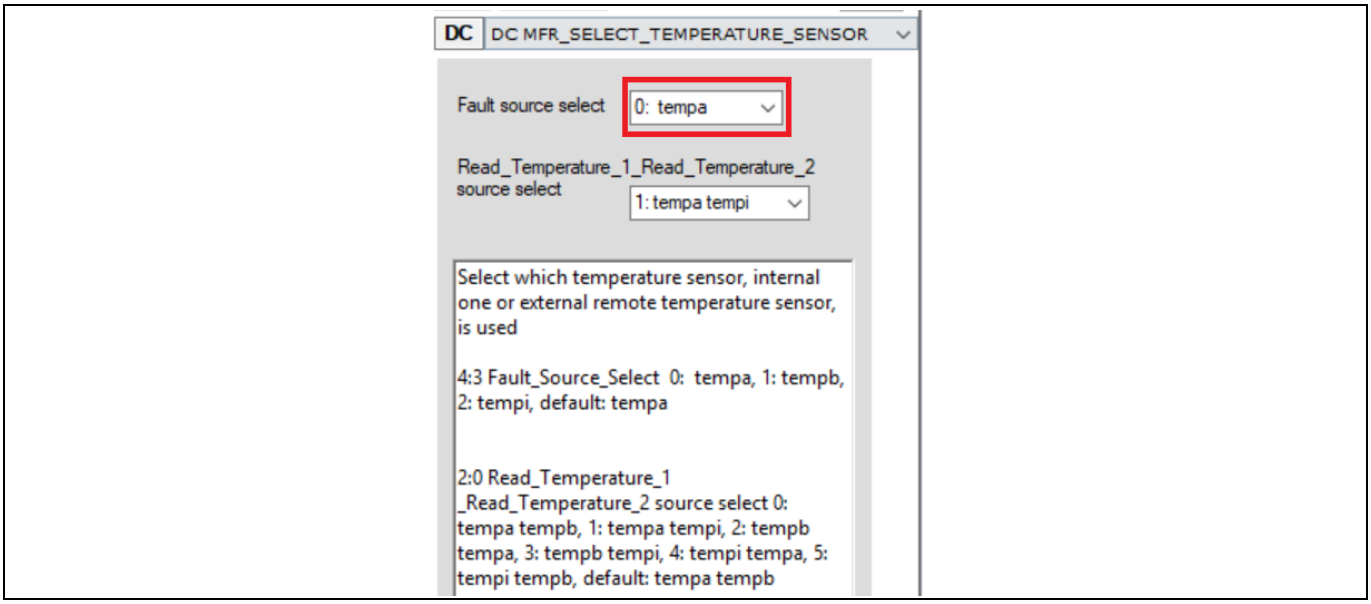


Figure 16 MFR_SELECT_TEMPERATURE_SENSOR

4.2 Register configuration

The XDPP1100 GUI provides the necessary design tools for the user to configure the registers. In the XDPP1100 GUI, go to the “Design Tools” tab and follow the design tool steps from 1 to 7. Some key parameters are configured as follows.

Table 5 HBCT_VM register set-up

Register name	Value	Register name	Value
ce0_ktrack_hiz	1	ramp0_m_flavor	2 (trailing-edge modulation)
ce0_ktrack_off	4	ramp0_half_mode	1
ce0_ktrack_on	2	ramp0_min_pw_state	0
ce0_kslope_didv	216	mode_control_loop0	0 (voltage mode control)
ce0_pwmwin_dly	10	ramp0_dutyc_lock	0 (disable flux balancing)
ce0_kslope_lm	0	vrs_voltage_init	57
pid0_kfp1_index_1ph	40	ki_fbal	0
pid0_kfp2_index_1ph	32	kp_fbal	0
pid0_kp_index_1ph	37	fbal_max	0
pid0_ki_index_1ph	27	fbal_time_only	0
pid0_kd_index_1ph	62	ical_en	1
pid0_ff_vrect_override	639	vsp1_vrs_sel	1
pid0_ff_override_sel	0	tlm0_iout_src_sel	0
pid0_ff_vrect_sel	0	tlm0_iin_src_sel	2

4.2.1 Loop PID configuration

The loop PID coefficients should be configured by using the 3 PID – Bode Plot design tool.

Figure 17 shows the PID design tool and parameters of the demo board in VMC. The user could tune K_p, K_i, K_d and the two low-pass filters’ bandwidth to obtain the desired gain and phase margin. The design tool shows the bode plot based on the load model and the compensation. The tool also helps the user determine the PID parameters if the load model is provided. Please note that the accurate load model is required for a correct bode plot. The critical parameters are output inductor value L, output capacitor value and ESR, input voltage

V_{IN}, output voltage V_{OUT} and output current I_{OUT}. Once the load model inputs are provided, go to the “Bode Plot” page and place the desired poles and zeroes in the right-hand side table, then click <== to calculate the PID compensation parameters.

In general, the two zeroes could be placed at the double-pole of the output LC filter, and pole 1 can be placed at half of the switching frequency. Once the tool calculates PID parameters, use ==> to view the adjusted poles and zeroes.

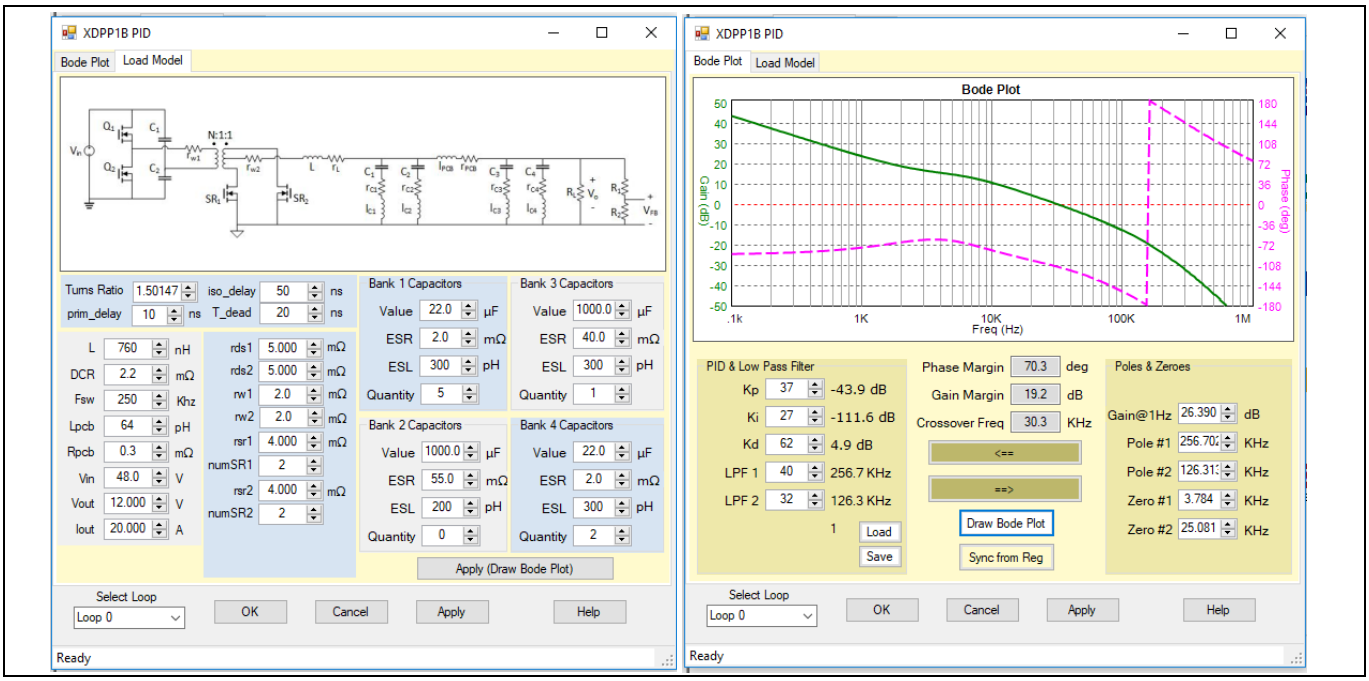


Figure 17 PID – bode plot design tool

4.2.2 Output and input CS configuration

Output current, input current, input voltage and PWM/ramp are configured by design tool 6 Basic Configuration. **Figure 18** shows the configuration of output CS.

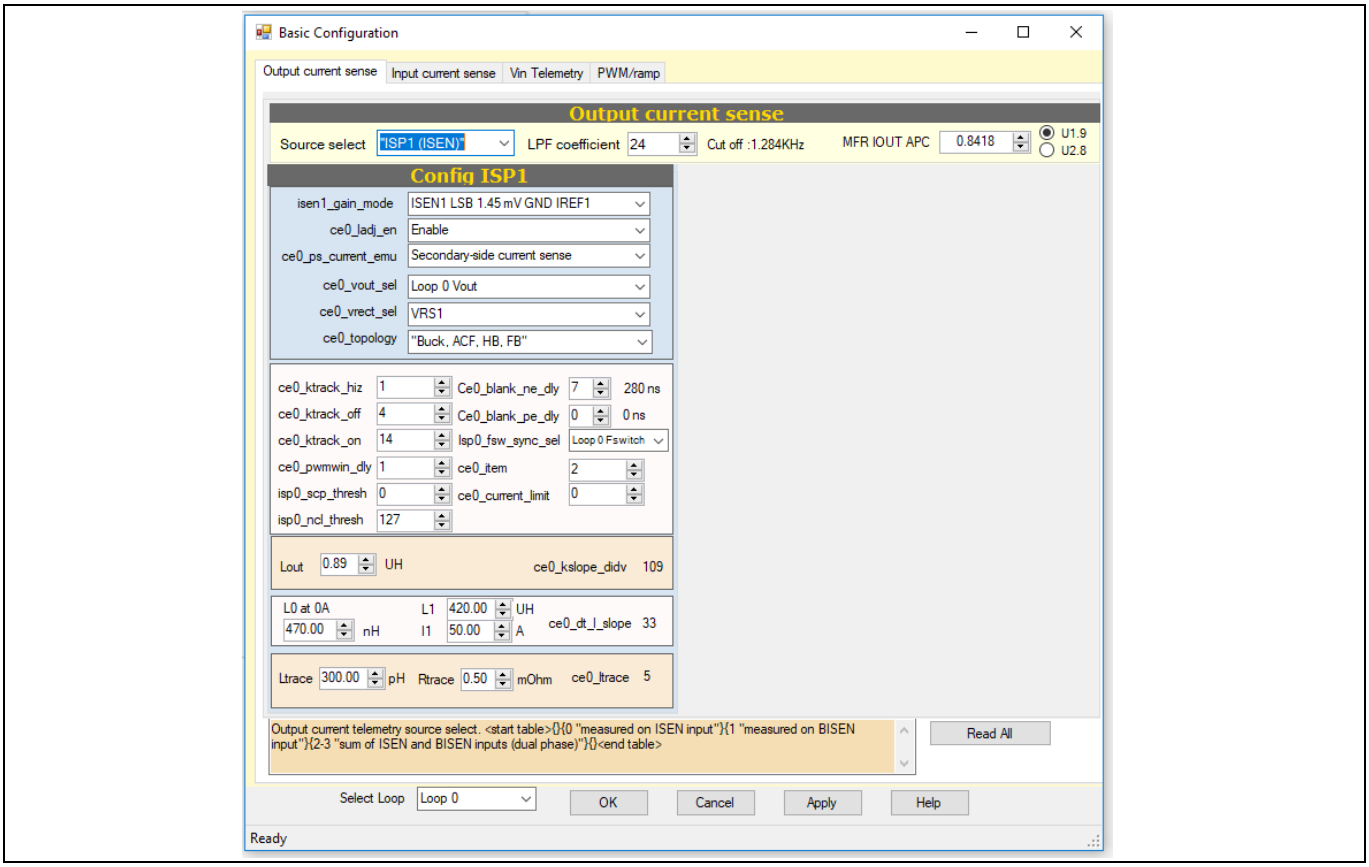


Figure 18 Output CS configuration tool

- The ktrack registers are used to set the track gain of the current estimator. The value of the ktrack gain can be set in a range of 0 to 15. When set to 0, the current estimator will not track to ADC sensed current but will fully rely on estimation, which is calculated based on voltage and inductor value (ce_kslope_didv). When ktrack gain is set to 15, the current estimator uses the actual sensed current. Other values set the weight of sensed current over estimated current with a ratio of x/15.
- kslope_didv defines output inductor current slope. It is calculated based on IOUT_APC and L_{OUT} value.

  For output CS:

$$ce0\_kslope\_didv = \frac{1(V) \cdot 10(ns)}{Lout(nH) \cdot APC\ (\mathrm{A})} \times 2^{13}$$

- ce0_pwmwin_dly defines the “PWM Window Delay”, used to align the internal PWM signal to incoming CS waveform. Delay time is defined by (ce0_pwmwin_dly + 1) x 10 ns.
- ceX_blank_ne_dly and ceX_blank_pe_dly define the leading-edge blanking time for the CS at the negative edge and positive edge of PWM. The blanking time can be set between 0 ns and 280 ns.
- ceX_dt_l_slope defines the output inductor derating slope. If the inductance drop with instantaneous current, the current estimator adjusts the di/dt slope accordingly.
- ceX_ltrace compensates for the parasitic inductance of the CS resistor.

When the converter is configured in VMC, the input current telemetry can only be selected as “estimated input current” based on I_{OUT}. The register tlm0_iin_src_sel = 2.

4.2.3 Input VS and FF configuration

The XDPP1100 use VRSEN/VRREF ADC to sense the input voltage from the secondary side of the transformer. The input voltage is calculated based on the sensed VRSEN voltage, the V_{RECT} resistor-divider ratio and the transformer turns ratio.

Figure 19 shows how the sampling of the V_{RECT} waveform works. Noise has been added to the ideal VRSEN waveform to highlight the importance of sampling window timing.

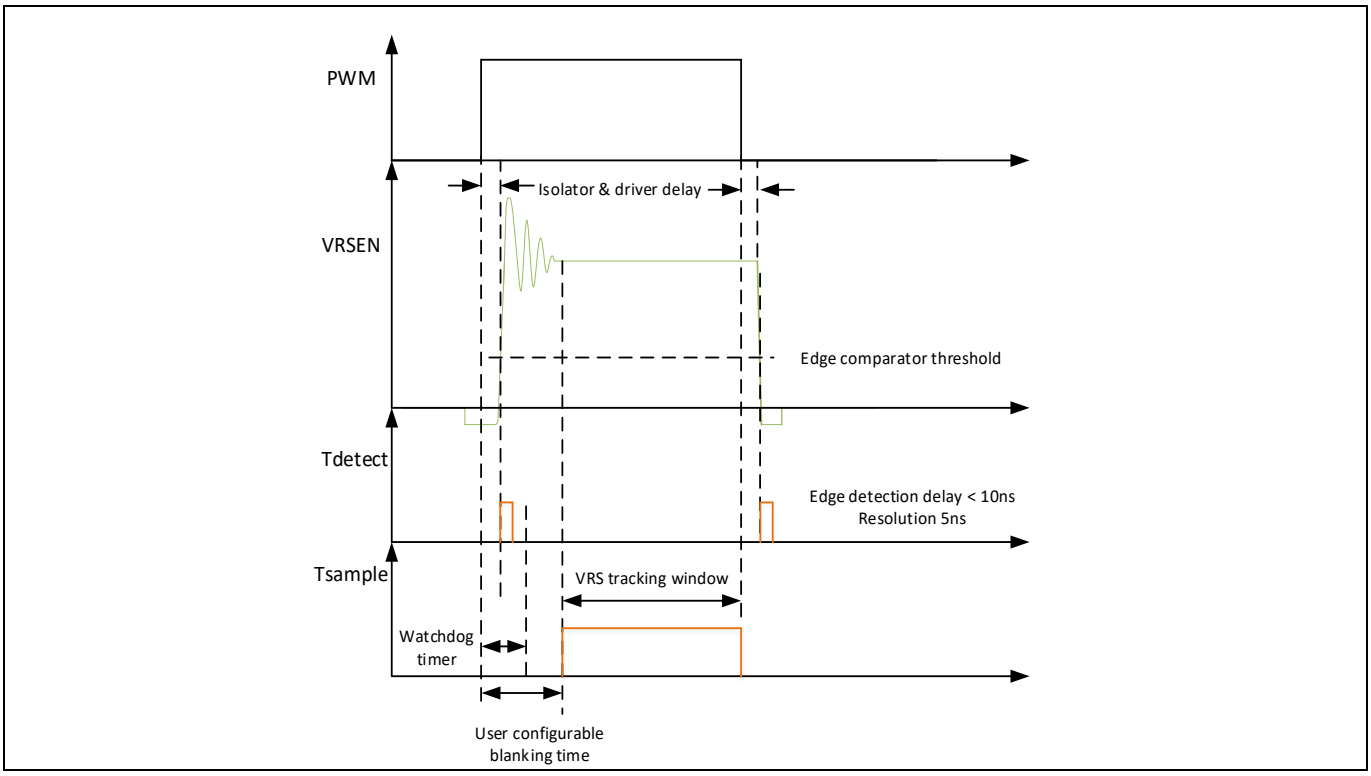


Figure 19 Timing of V_{RECT} sensing by VRSEN

The VRS edge detector works at 200 MHz clock. It senses the rising and falling edges of the V_{RECT} waveform with delay less than 10 ns. T_{detect} waveform is the output of edge detector logic. The rising edge of the rectified voltage waveform is detected and a programmable blanking window is added to it. The blanking time should be configured longer than the voltage spike and ringing duration. The blanking time should also be set longer than 250 ns for the tracking ADC to settle (vrs_track_start_thr register).

The edge comparator has two configurable reference voltage thresholds: 500 mV and 300 mV, defined by register vrs_cmp_ref_sel. The user can choose a proper threshold based on the VRSEN signal level. To optimize VRSEN accuracy, it is recommended to scale V_{RECT} voltage to VRSEN in the 600 mV to 2.1 V range. The V_{in} under-voltage fault threshold is 30 V, V_{IN} over-voltage fault threshold is 80 V; transformer turns ratio is 3:2. V_{RECT} amplitude spans from 10 V to 27 V between the two V_{IN} fault limits. Setting the V_{RECT} resistor-divider ratio to 0.071289 scales V_{RECT} to 0.71 V~1.92 V, nicely fitting within the VRSEN input voltage range.

After the blanking window, sampling of the rectified voltage can occur (shown as the T_{sample} waveform). The sampling window ends when the associated PWM signal goes low. If input voltage changes during this period, VRS ADC tracks the change. At the end of a sampling window, VRS ADC remembers the value of the last ADC sample and uses this value for the FF computation for the next switching cycle.

At start-up prior to PWM switching, the FF is computed with an initial voltage that is configured by register vrs_voltage_init. The initial input voltage is typically set to nominal input voltage per application.

Configuration

The FF computation is implemented in hardware and thus offers the fastest response. The XDPP1100 computes FF duty-cycle based on input voltage and output voltage, and the result is added to the feedback loop PID filter output to resolve PWM duty-cycle (**Figure 20**).

$$computed\_feed\_forward = \frac{Vout,target}{Vin \times trans\_scale\_loop}$$

Here, trans_scale_loop is the transformer turns ratio, defined by N_S/N_P in FB or active clamp forward topologies, and $N_S/(2N_P)$ in a HB topology. Wherein N_P is the transformer primary turns number, and N_S is the transformer secondary turns number. The user can define the transformer scale by PMBus command MFR_TRANSFORMER_SCALE (N_S/N_P) for all isolated topologies. The XDPP1100 FW will calculate the trans_scale_loop based on MFR_TRANSFORMER_SCALE command and device topology. The FW takes care of factor 2 for the HB topology, and the user should not be concerned with setting it manually.

The register pid_ff_vrect_sel selects the FF input source. In this demo board, VRSEN is used for the FF computation.

$$computed\_feed\_forward = \frac{Vout,target}{Vrect}$$

The user could configure the FF registers by using GUI design tool 7 “Advanced features”, “Feed-forward” tab (**Figure 21**).

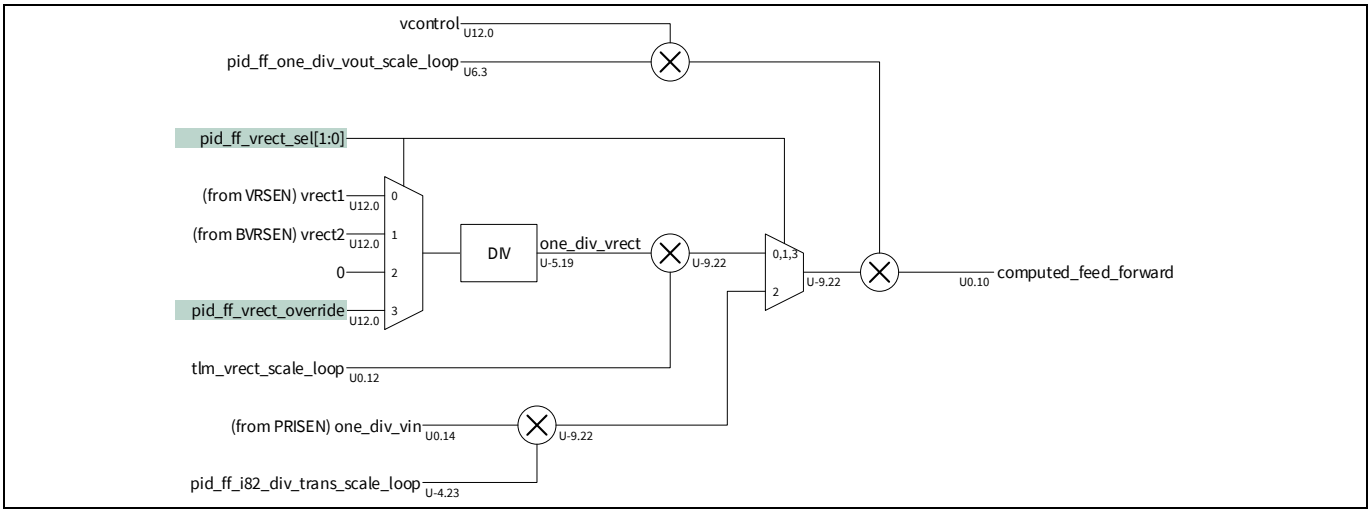


Figure 20 XDPP1100 FF computation

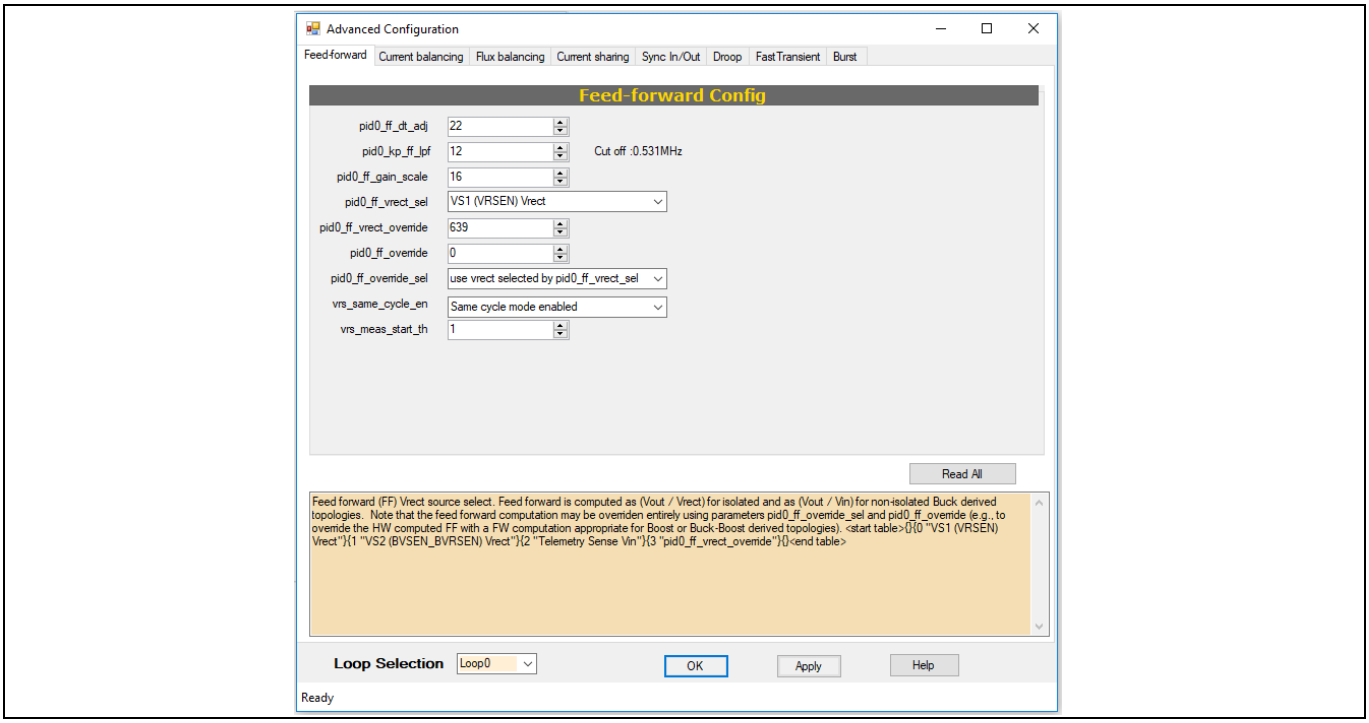


Figure 21 FF configuration tool

More details of input voltage sensing and FF can be found in the XDPP1100 application note.

5 Regulation and telemetry

5.1 Line and load regulation

Line and load regulation was tested at 36 V, 48 V and 75 V input, at 0 A/5 A/10 A/15 A/20 A load. The regulation is within target +/-0.5 percent. The HB-CT board is designed to work in open-loop condition at low-line (less than 40 V), and output voltage drops with V_{IN}. Thus the output voltage command is changed to 10 V at 36 V input.

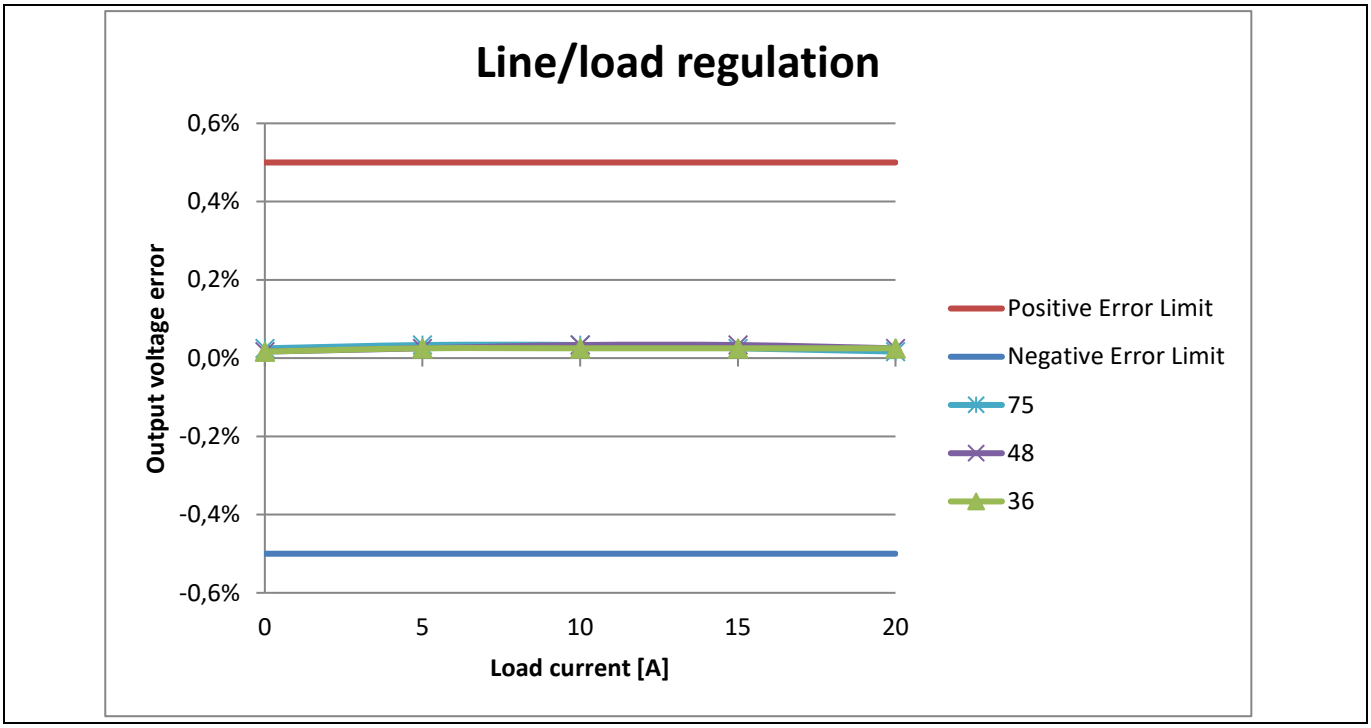


Figure 22 12 V/20 A HB-CT regulation

5.2 Output voltage ripple

Output voltage ripple was measured at the tip-and-barrel test-point at 20 MHz BW. Output voltage ripple is below 120 mV.

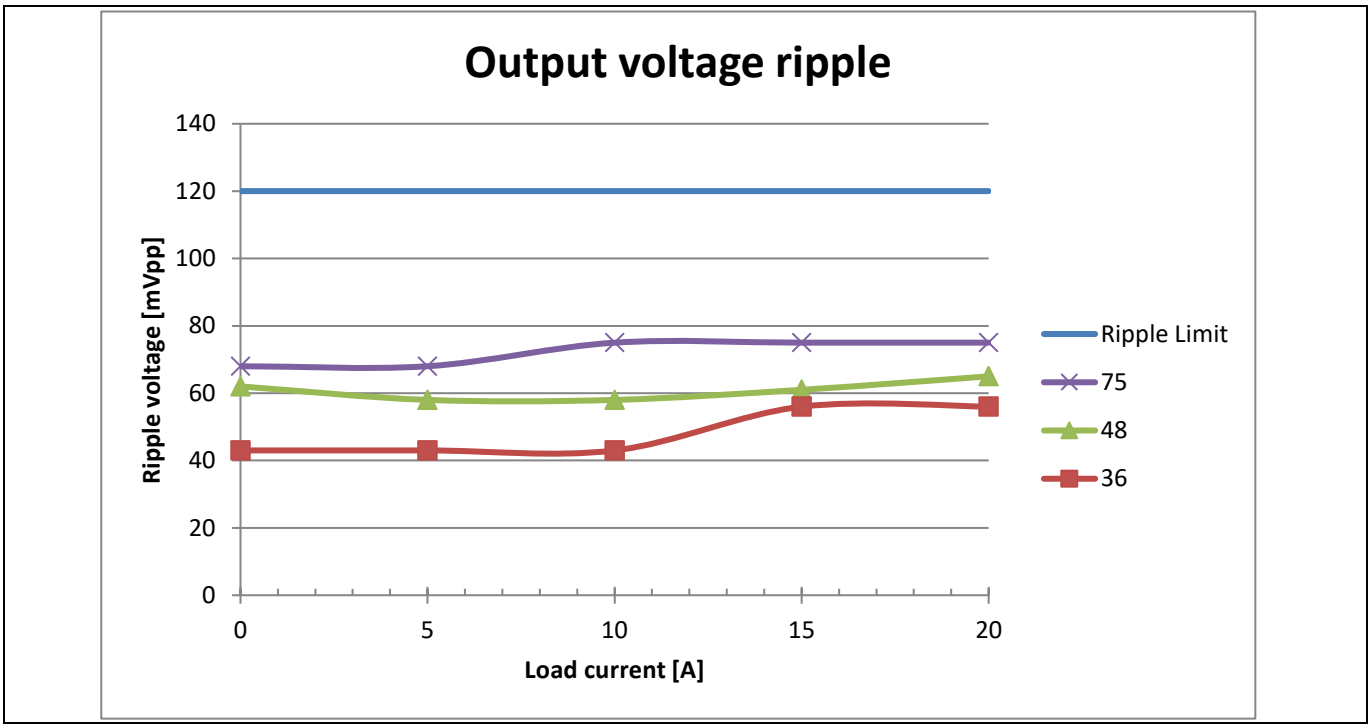


Figure 23 Output voltage ripple

Output ripple waveforms are shown in **Figure 24**.

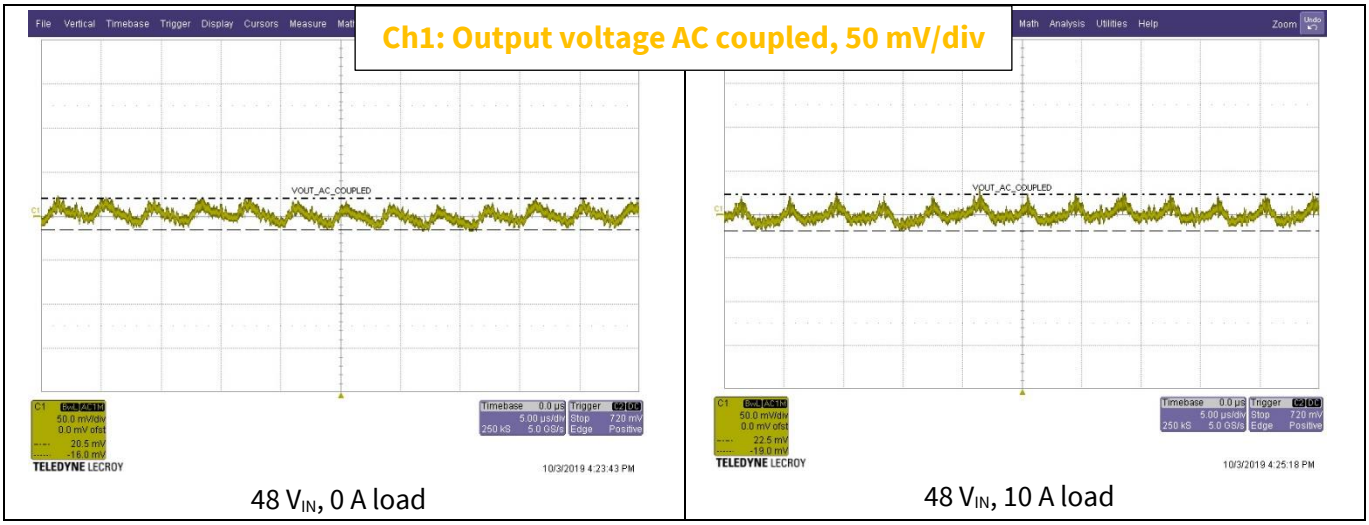


Figure 24 Output ripple waveforms

5.3 V_{IN} telemetry

XDPP1100 senses input voltage from the secondary side of the transformer through V_{RECT} sensing. At heavy load, the voltage drop on the power path resistance could introduce READ_VIN error. XDPP1100 enables resistive compensation, which is set by register tlm0_vrect_rcorr (LSB=3.90625 mΩ). Setting this register to 20 (78.125 mΩ) gave a good compensation result.

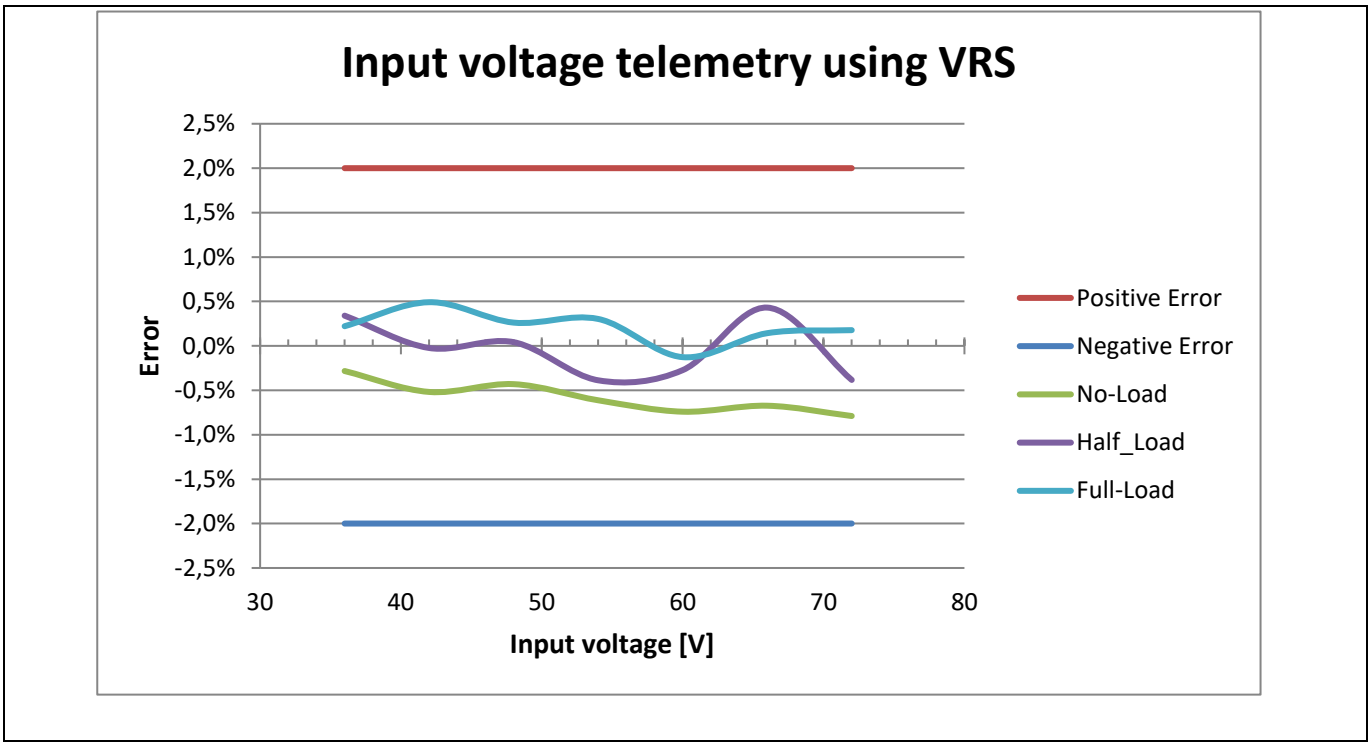


Figure 25 READ_VIN accuracy

5.4 I_{OUT} telemetry

Output current telemetry has a large error at light load due to op-amp offset and small-scale signals. Above 4 A output the read output current or telemetry reading is within a 1 A window over all input lines.

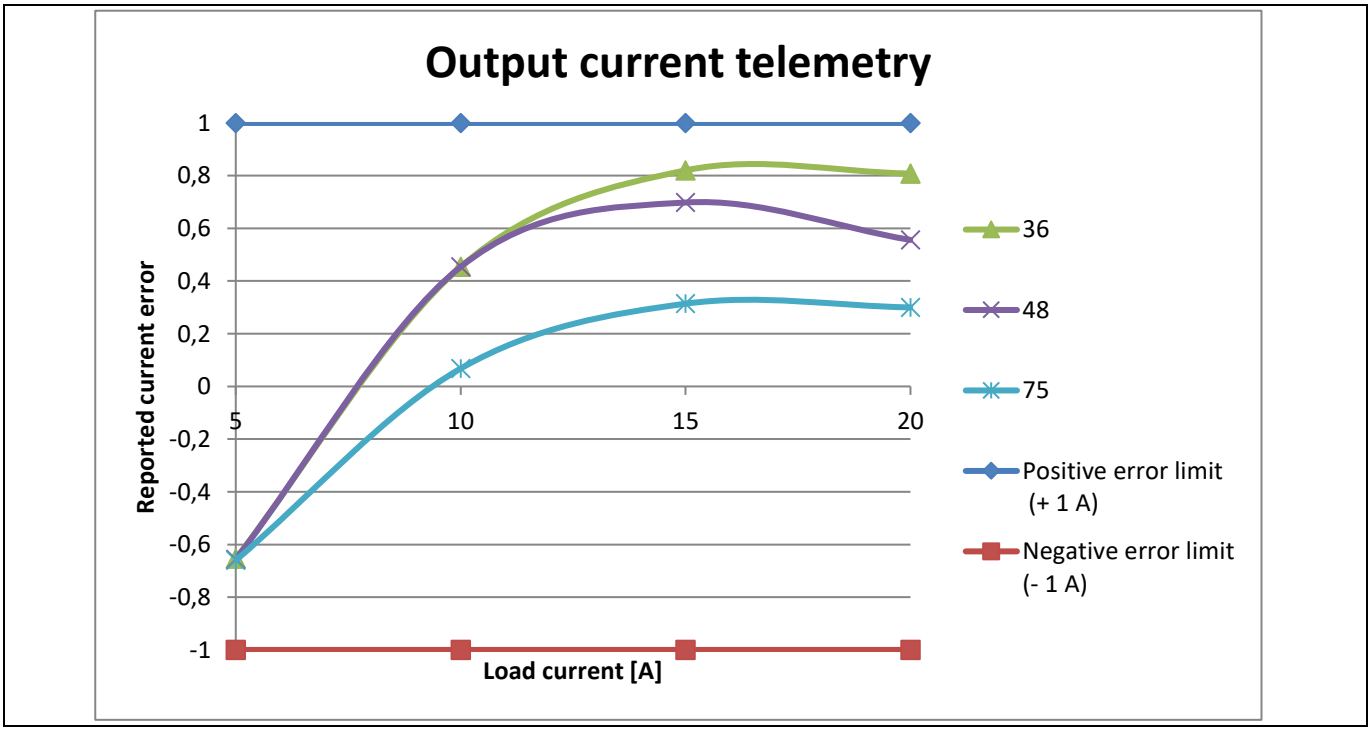


Figure 26 READ_IOUT accuracy

5.5 I_{IN} telemetry

Input current is estimated based on I_{OUT} and V_{IN} (tlm0_iin_src_sel = 2). Current read with temperature compensation is enabled.

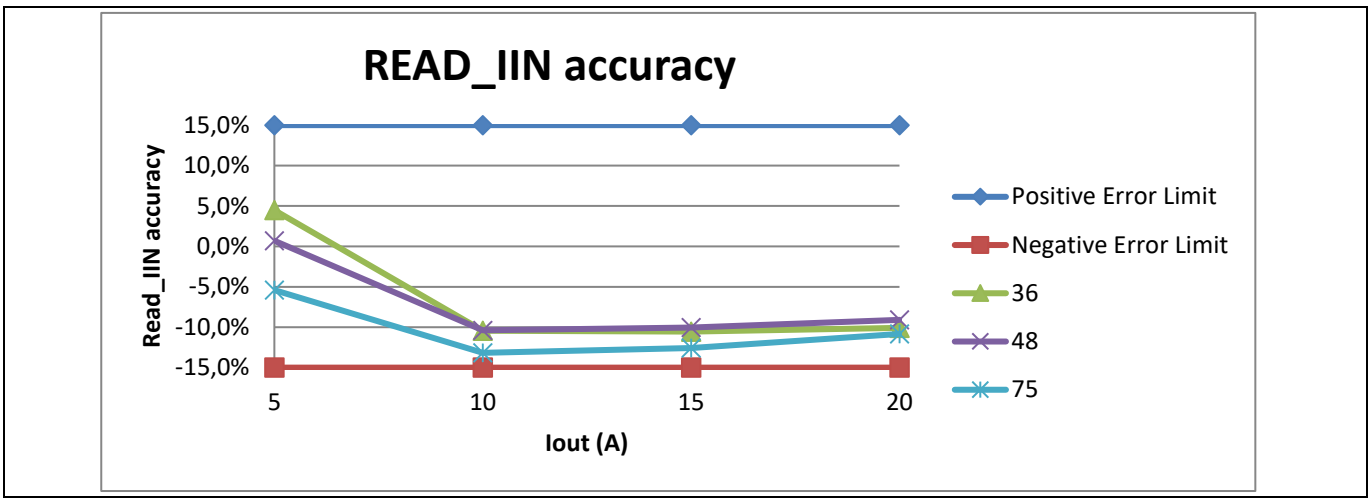


Figure 27 READ_IIN accuracy

5.6 Efficiency

Efficiency was measured over line and load range at different load points. At 36 V_{IN}, V_{OUT} is set to 10 V for regulation, thus the maximum output power is 200 W at 36 V_{IN}.

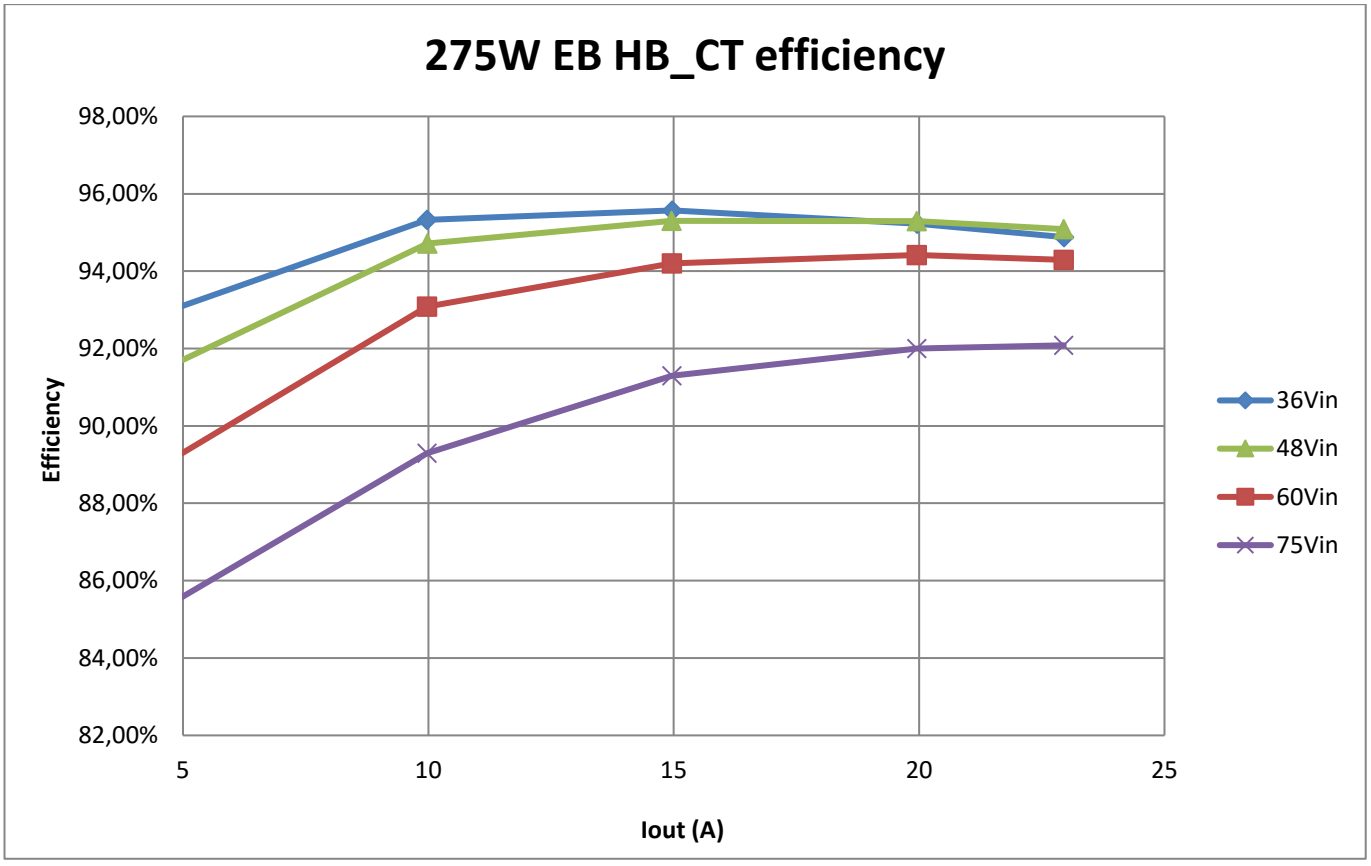
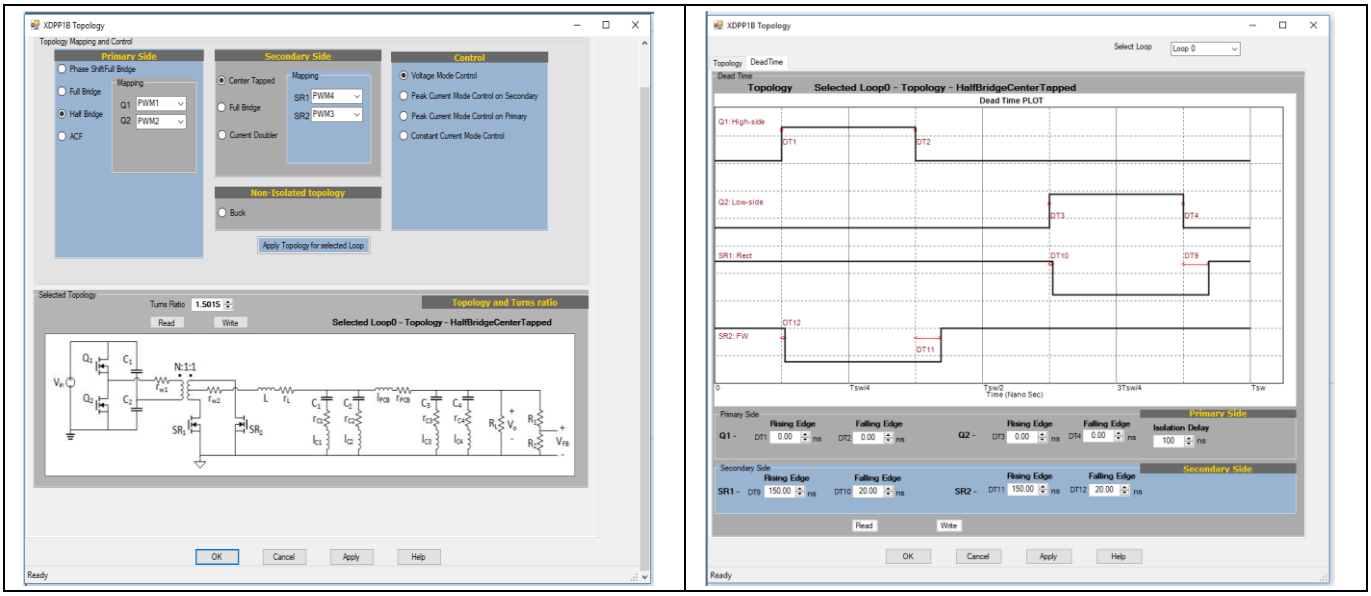


Figure 28 Efficiency of 275 W eighth-brick HB-CT with digital controller XDPP1100

Table 6

V_{IN} (V)	I_{IN} (A)	P_{IN} (w)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
Efficiency at 36 V DC input						
36.004	1.4905	53.66	10.009	4.9917	49.96	93.10 percent
36.007	2.912	104.85	10.018	9.9772	99.95	95.33 percent
36.003	4.363	157.10	10.029	14.9705	150.14	95.57 percent
36.004	5.8438	210.40	10.037	19.9622	200.36	95.23 percent
36.002	6.7497	243.00	10.043	22.9566	230.55	94.88 percent
Efficiency at 48 V DC input						
48.01	1.3634	65.456834	12.013	4.9969	60.0277597	91.71 percent
48.008	2.6383	126.659506	12.021	9.9793	119.961165	94.71 percent
48.001	3.934	188.835934	12.03	14.9594	179.961582	95.30 percent
48.008	5.251	252.090008	12.038	19.955	240.21829	95.29 percent
48.005	6.0534	290.593467	12.042	22.9458	276.313324	95.09 percent
Efficiency at 60 V DC input						
60.008	1.1186	67.1249488	12.012	4.9901	59.9410812	89.30 percent
60.003	2.1468	128.81444	12.021	9.9744	119.902262	93.08 percent
60.004	3.1847	191.094739	12.028	14.9662	180.013454	94.20 percent
60.003	4.2404	254.436721	12.038	19.9562	240.232736	94.42 percent
60.003	4.8841	293.060652	12.042	22.9478	276.337408	94.29 percent
Efficiency at 75 V DC input						
75.009	0.934	70.058406	12.012	4.9915	59.957898	85.58 percent
75.01	1.7899	134.260399	12.018	9.9753	119.883155	89.29 percent
75.012	2.6282	197.146538	12.026	14.9664	179.985926	91.30 percent
75.011	3.48	261.03828	12.034	19.9558	240.148097	92.00 percent
75.012	3.9995	300.010494	12.039	22.947	276.258933	92.08 percent

Gate timing settings used for efficiency measurement.



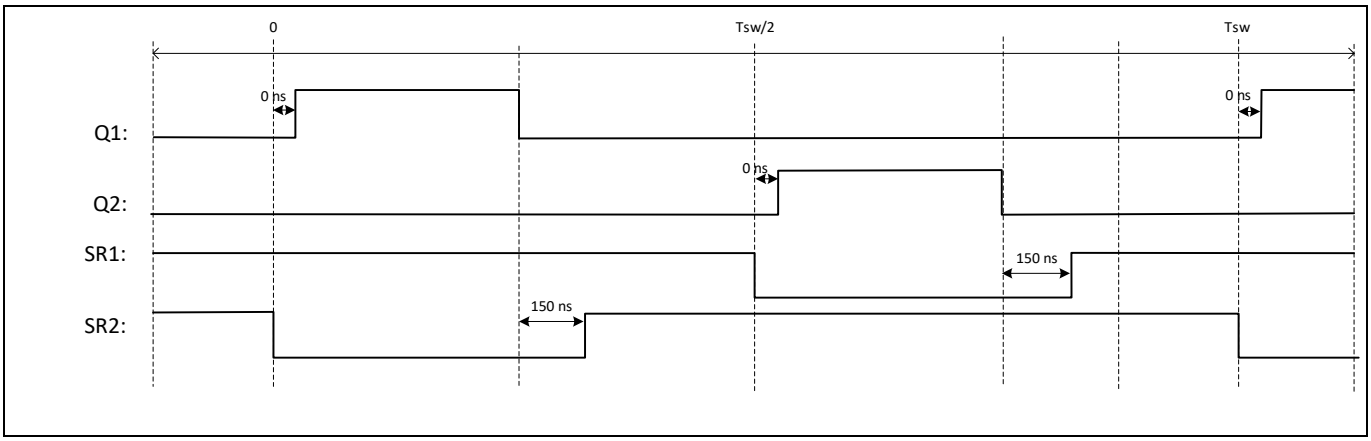


Figure 29 Gate timing settings used for efficiency measurement

5.7 Temperature telemetry

XDPP1100 supports both external temperature sensing and internal temperature sensing for protection and monitoring. External temperature sensing is performed with a 47 kΩ NTC thermistor, in parallel with a 12 kΩ resistor that is connected between TSEN or BTSEN and ground. This demo uses a NTC resistor to sense PCB temperature near the CS copper. The temperature is used to compensate for CS resistor value.

To test temperature telemetry, the unit was heated up while reading the board temperature through the XDPP1100 controller. The board was tested at nominal input voltage of 48 V DC and 20 A output load. The fan speed was slowly reduced, causing the board temperature to heat up. The measurement was taken by using a Flir thermal camera. The telemetry reading was fairly close to the actual temperature measurement.

Table 7 Temperature telemetry accuracy

Temperature, T_a (telemetry)	Temperature, T_i (telemetry)	Real I_{sense} trace temperature (Flir thermal camera)
20	22	22.3
39	42	41
48	50	49.3
60	63	62.1
83	88	86

5.8 Thermal image

The following thermal images were captured for eighth-brick HB-CT isolated DC-DC converter mounted on Infineon quarter-brick test fixture over two different line voltages, 48 V and 75 V at 23 A full-load current. The cooling fan voltage was set to 6.5 V for this test.

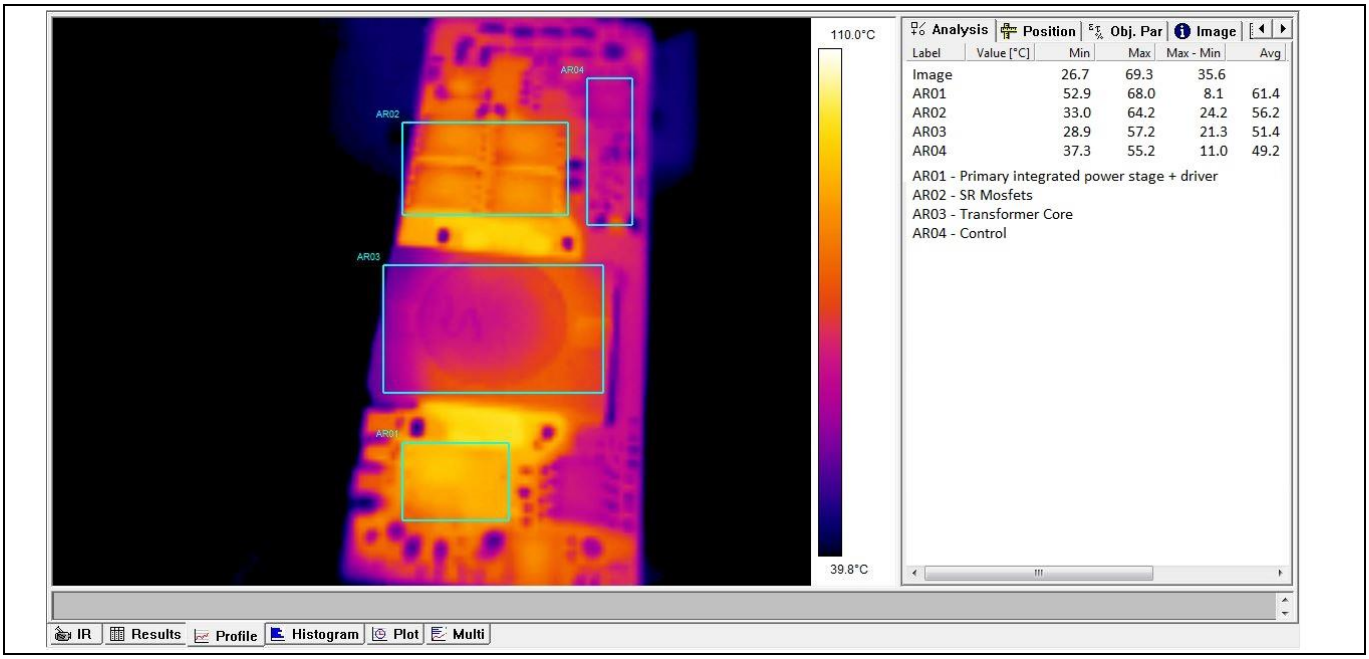


Figure 30 Thermal image at 48 V_{IN}, 12 V_{OUT} at 23 A load current

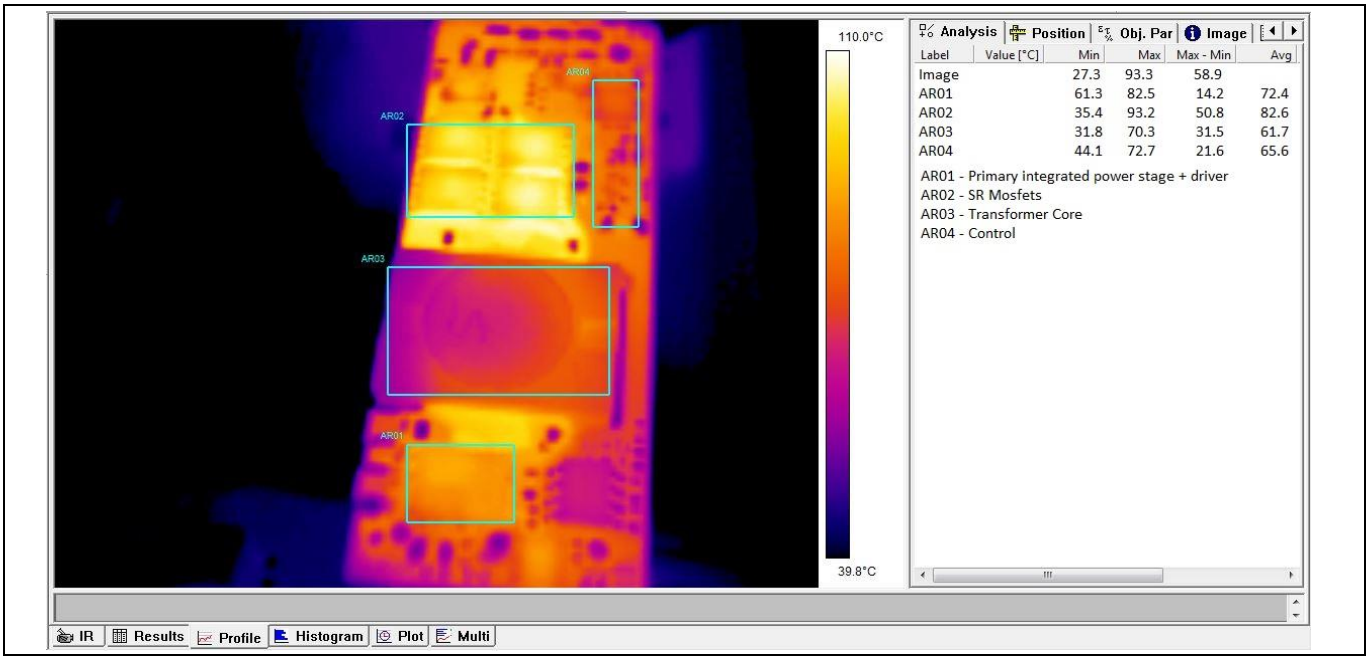


Figure 31 Thermal image at 75 V_{IN}, 12 V_{OUT} at 23 A load current

6 Operation waveforms

6.1 Soft-start

Tested start-up at 0, 50 percent, 100 percent load, at 48 V/72 V. SR is enabled from the beginning of start-up (diode emulation mode is disabled). Tested at TON_RISE = 20 ms. V_{OUT} has monotonic ramp without glitch. Write vrs_voltage_init = 57 to set 48 V initial vrs voltage.

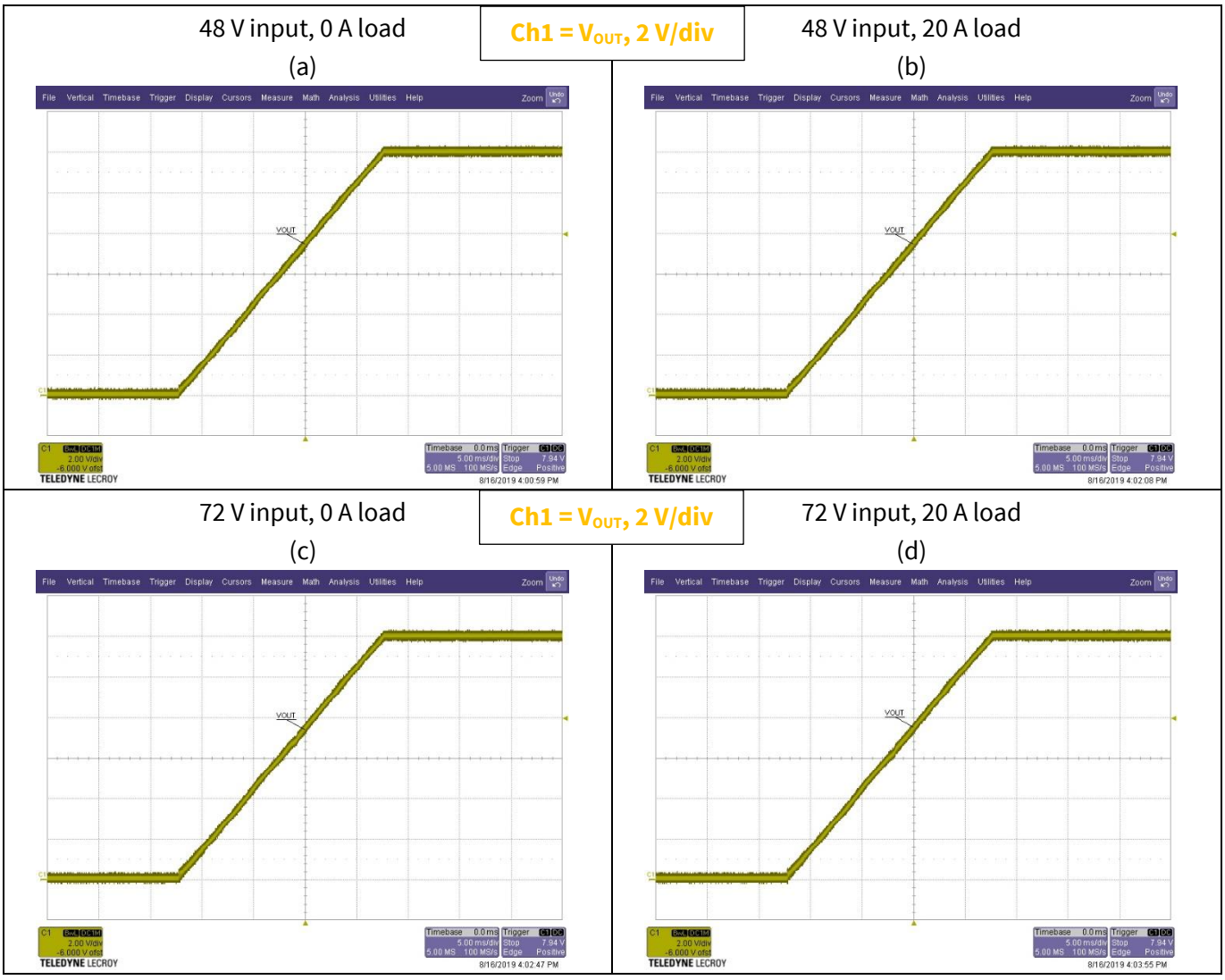


Figure 32 Monotonic start-up

6.2 Pre-bias start-up

Pre-bias start-up was tested at no-load condition, with Diode Emulation (DE) mode (PMBus command 0xC5 FW_CONFIG_REGULATION bit:0 = 1, EN_DE_START-UP = 1), and with SR enabled (PMBus command 0xC5 FW_CONFIG_REGULATION bit:0 = 0, EN_DE_START-UP = 0).

The start-up ramp will keep the same slope as regular start-up without pre-bias. The start time is calculated by FW using the equation below:

$$Ramp\_Time = \left(TON_{RISE} \times Prebias_{voltage}\right) \div VOUT\_COMMAND$$

Operation waveforms

Figure 33 shows the test results with pre-bias voltage set to 90 percent of the target V_{OUT} and vrs_voltage_init = 57 (initial input voltage set to 48 V).

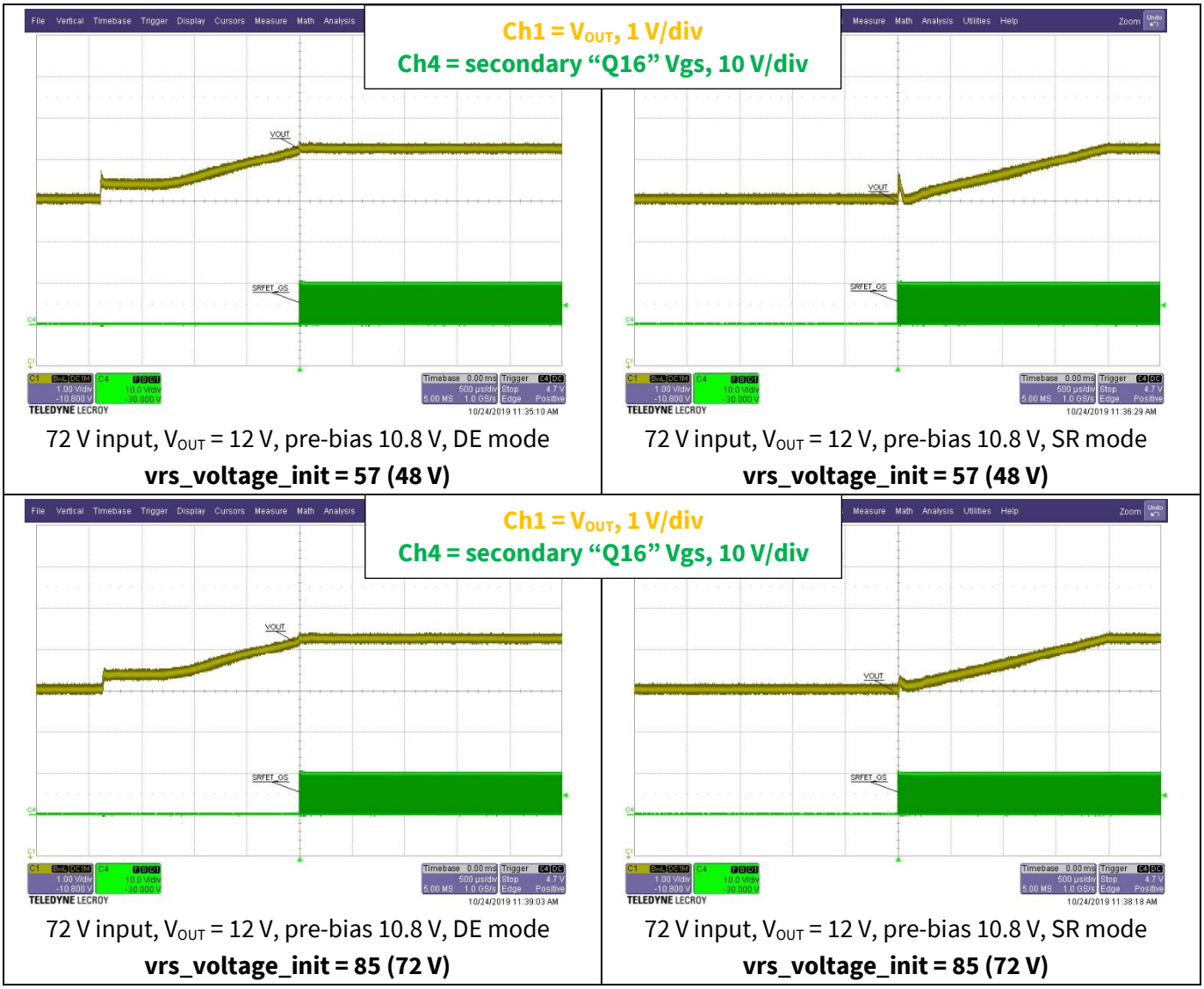


Figure 33 Pre-bias start-up at 72 V_{IN}, 90 percent V_{OUT}, 0 A load

A voltage step at no-load is observed with diode emulation start-up (DE mode). This is because the start-up duty-cycle is predicted by the FF circuit based on $V_{OUT}/(V_{IN}*N_s/N_p)$. This works when SR is enabled. The actual desired duty-cycle is very narrow at no-load in DE mode. The energy that is delivered to load is more than required, thus the output voltage is charged up with a step. The feedback loop will then reduce the duty-cycle or even turn off primary PWM. But since there is no load to the discharge capacitor, the voltage plateau exists until the internal ramp exceeds the plateau voltage and continues charging the output capacitor toward target V_{OUT}.

At the end of the ramp, SR will turn on when V_{OUT} reaches the target voltage, which is defined by (VOUT_COMMAND – V_{OUT}_target_window). The V_{OUT}_target_window is configured by PMBus 0xC5 FW_CONFIG_REGULATION bit 31:24.

At 72 V input pre-bias start-up, a higher voltage spike is observed at the beginning of the ramp. This is because the initial voltage is set to 48 V and the FF duty-cycle is calculated based on 48 V input. This results in a larger duty-cycle than required duty for the system. When the initial voltage is changed to 72 V, the voltage spike is reduced. This shows that the user can improve the pre-bias response by using a direct primary voltage sensing

so that the FF is calculated based on the actual input voltage. This demo is designed only for the VRS sensing. Please refer to the “XDPP1100 isolated 48 V to 12 V 600 W quarter-brick converter” application note to study the impact of PRISEN or direct input voltage sensing on the pre-bias response.

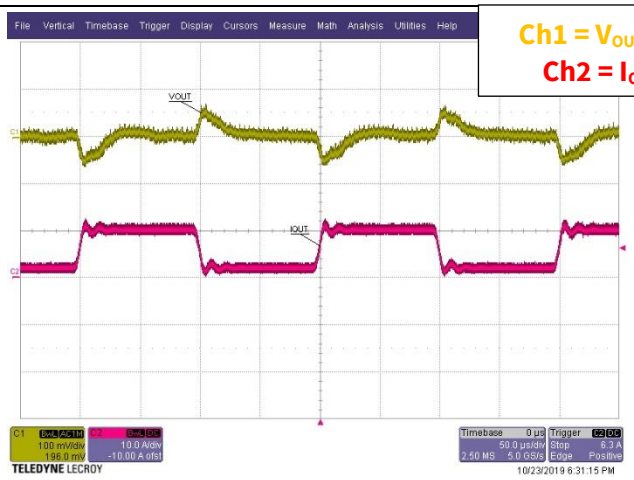
In addition to FF, the control loop compensator values also impact the pre-bias start-up response. A good optimized compensator parameter provides good pre-bias response as well.

6.3 Load-transient VMC

The loop is optimized with the following loop values using VMC. For 36 V DC input the output is set to regulate at 10 V.
pid0_kp_index_1ph = 53, pid0_ki_index_1ph = 34, pid0_kd_index_1ph = 74

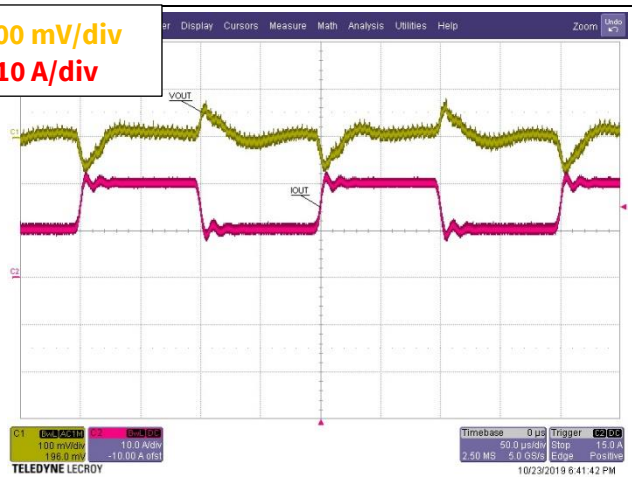
E-load transition rate is set to 2.5 A/µs.

The overshoot and undershoot during load transient is less than 100 mV. The loop settling time is less than 50 µs.



V_{IN} = 36 V DC at 10 to 50 percent – 10 output load transient

(a)

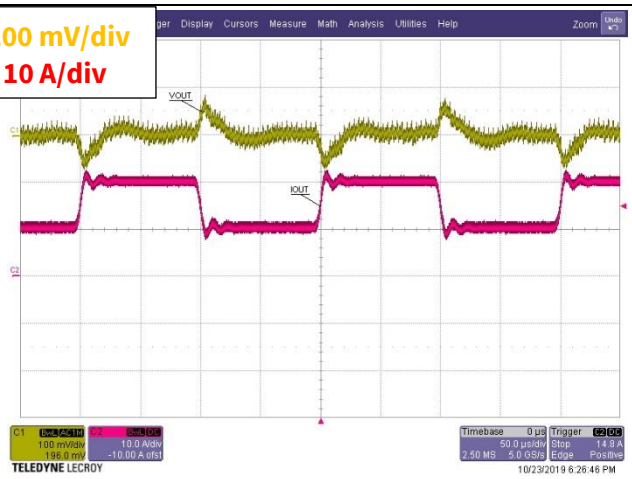


V_{IN} = 36 V DC at 50 to 100 percent – 50 output load transient

(b)

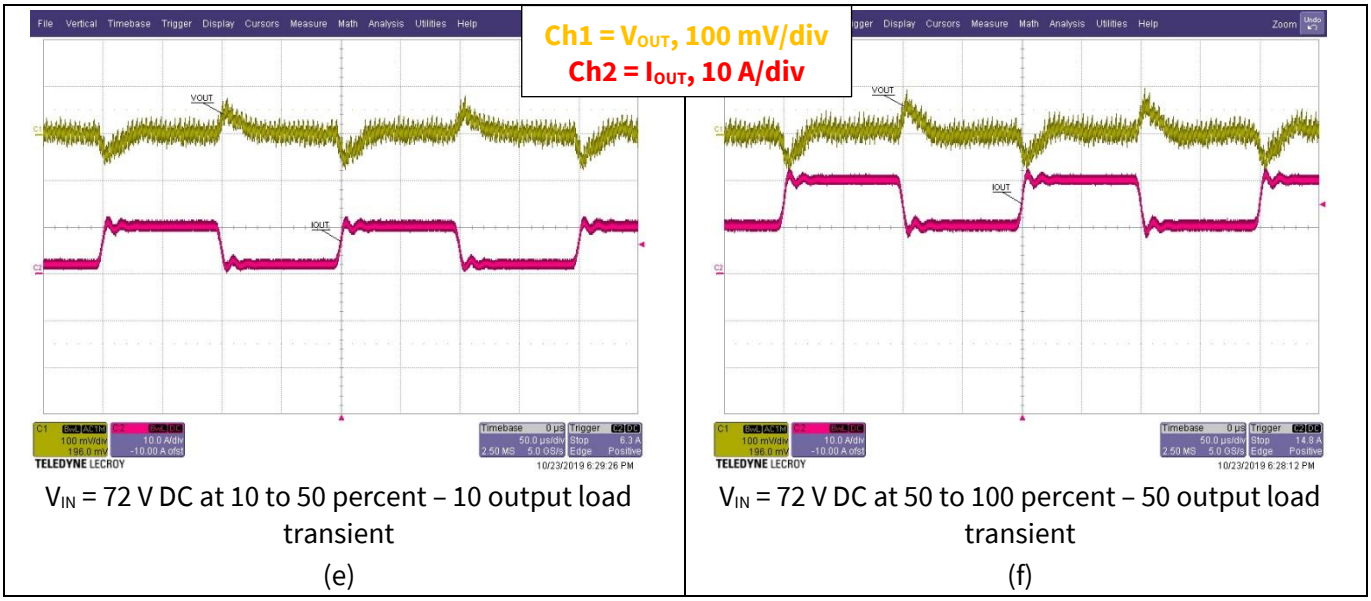
V_{IN} = 48 V DC at 10 to 50 percent – 10 output load transient

(c)



V_{IN} = 48 V DC at 50 to 100 percent – 50 output load transient

(d)



V_{IN} = 72 V DC at 10 to 50 percent – 10 output load transient
(e)

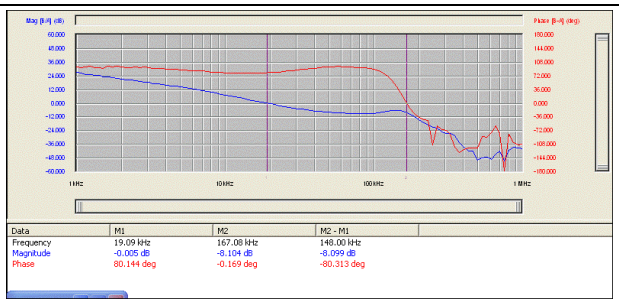
V_{IN} = 72 V DC at 50 to 100 percent – 50 output load transient
(f)

Figure 34 Load-transient waveforms (ch1: V_{OUT}, AC coupled 100 mV/div, ch3: I_{OUT}, 10 A/div)

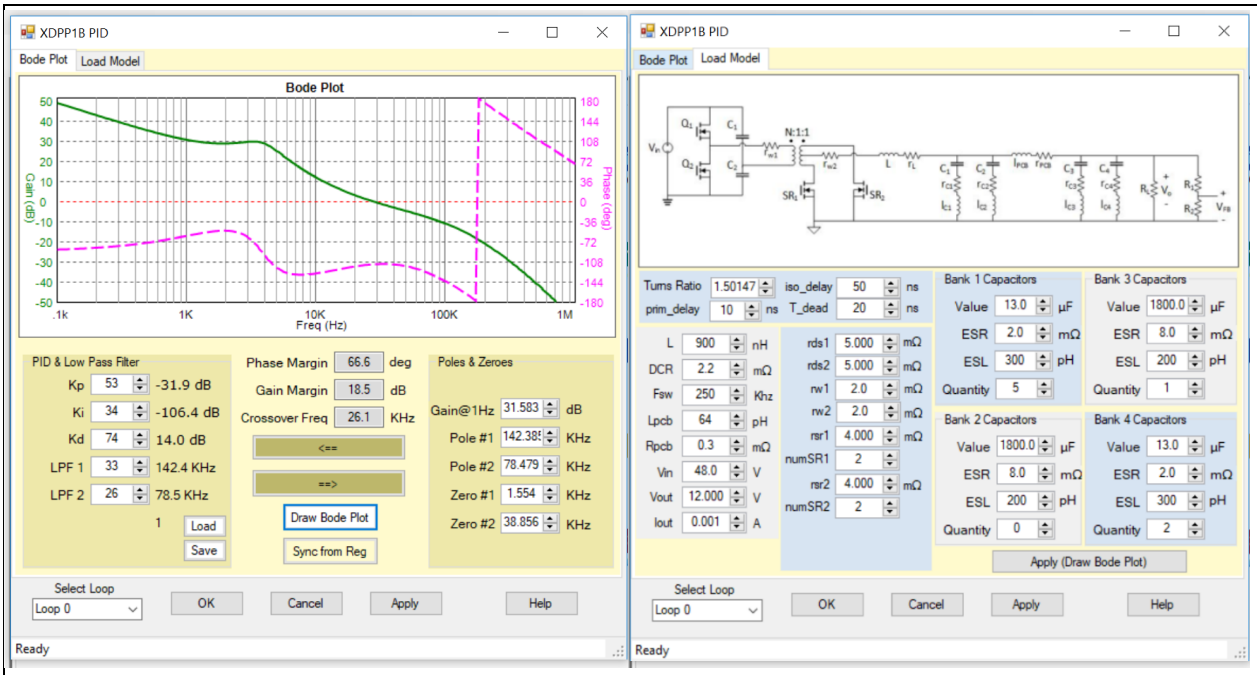
6.4 Bode response

This section compares the actual bode plots measured using a Model 200 network analyzer against GUI predicted bode response. The loop was optimized with the following loop values for voltage mode control. Below are the measured bode plots taken at 48 V and 0 A, 20 A in comparison to the GUI predicted plots.

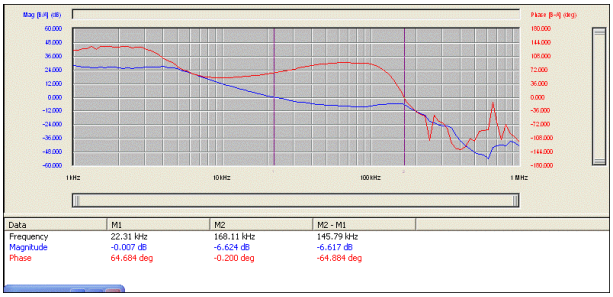
pid0_kp_index_1ph = 53, pid0_ki_index_1ph = 34, pid0_kd_index_1ph = 74



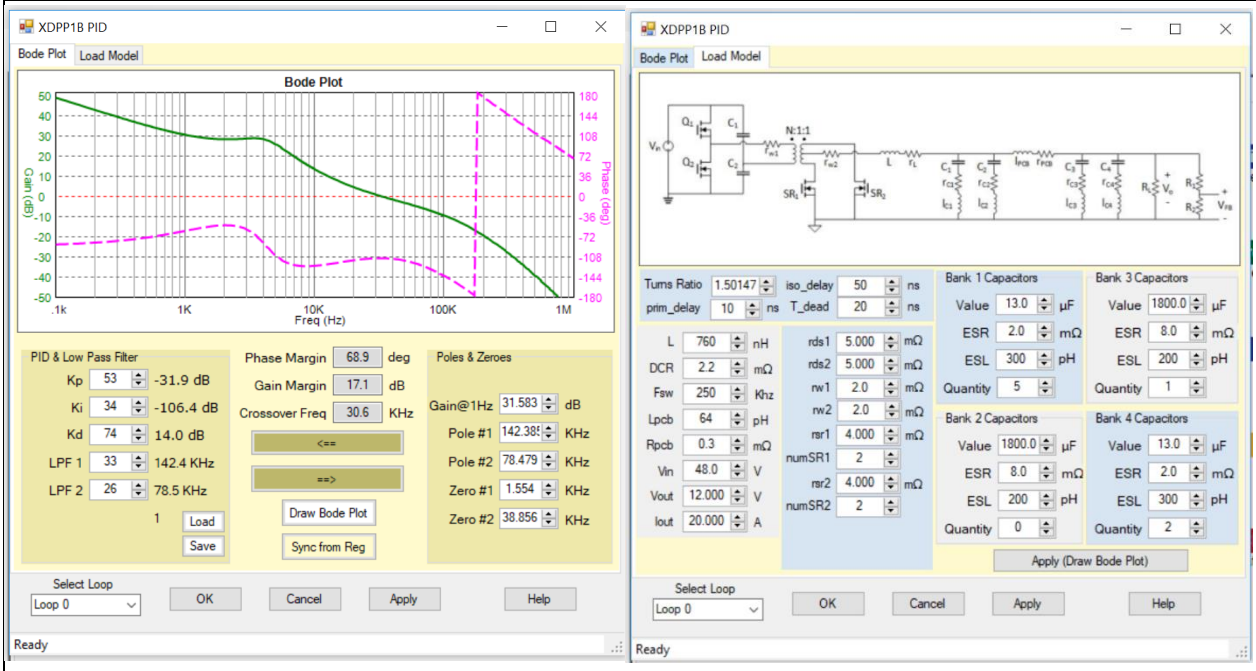
Measured bode plot, 48 V_{IN}, 0 A



GUI bode plot, 48 V_{IN}, 0 A



Measured bode plot, 48 V_{IN}, 20 A



GUI bode plot, 48 V_{IN}, 20 A

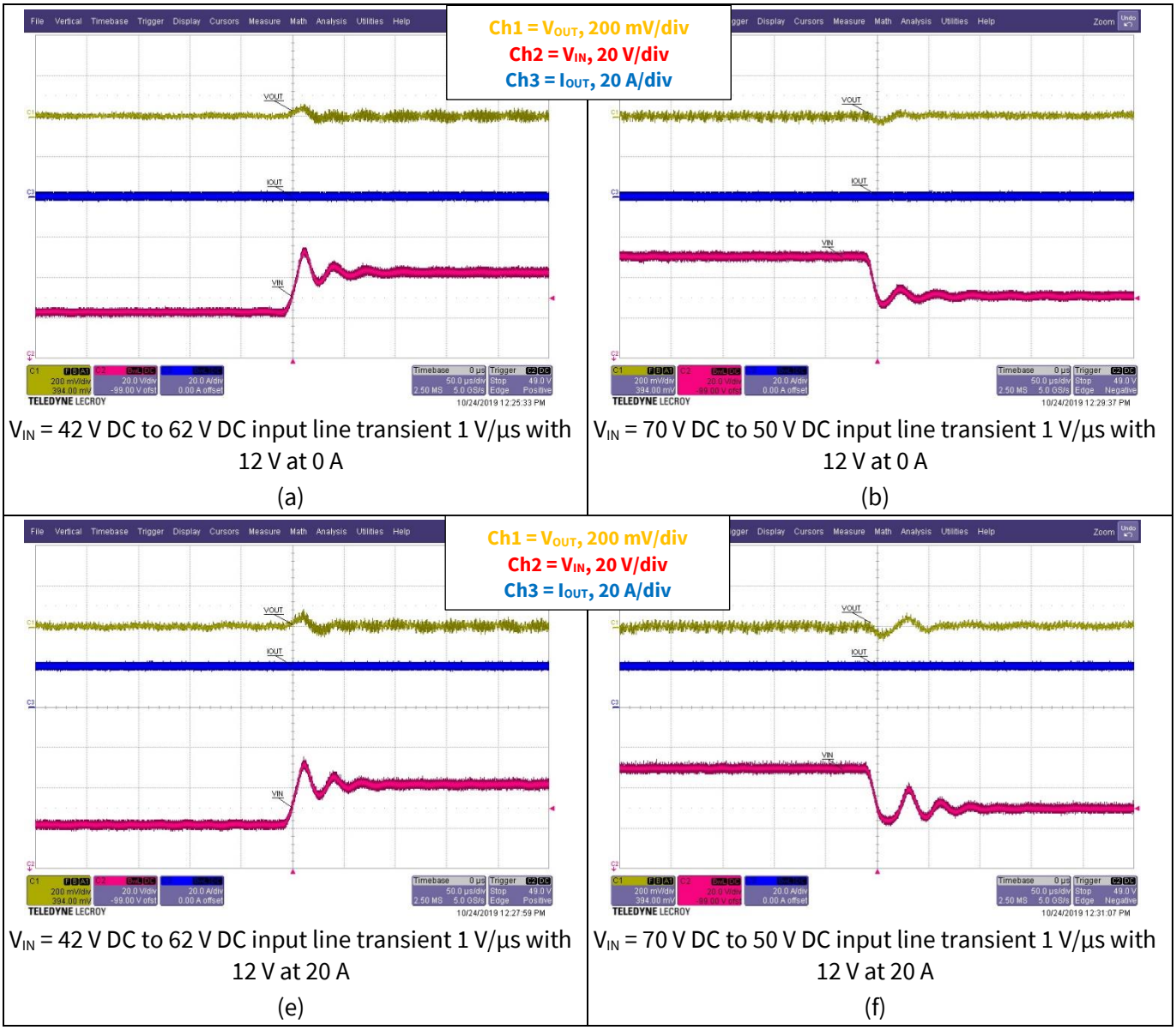
Figure 35 Bode response at 48 V input

Please note that the bode plot design tool will be updated to allow more parasitic parameters to be configured by the user. Please update the GUI on a regular basis to ensure you have the latest version.

It is observed that measured crossover is fairly close to the predicted GUI bode response. The small difference in crossover frequency is most likely because of the tolerences in the loop values used and the output filter itself. It is also observed that the GUI bode reponse is not closely related to the practical plot at no-load or under very light-load conditions because of the negative current flowing into secondary MOSFETs.

6.5 Line transient

Line transient was tested with FF enabled. Set pid0_ff_vrect_sel = 0 to select V_{RECT} as the source of input voltage sensing.



V_{IN} = 42 V DC to 62 V DC input line transient 1 V/µs with 12 V at 0 A

(a)

V_{IN} = 70 V DC to 50 V DC input line transient 1 V/µs with 12 V at 0 A

(b)

V_{IN} = 42 V DC to 62 V DC input line transient 1 V/µs with 12 V at 20 A

(e)

V_{IN} = 70 V DC to 50 V DC input line transient 1 V/µs with 12 V at 20 A

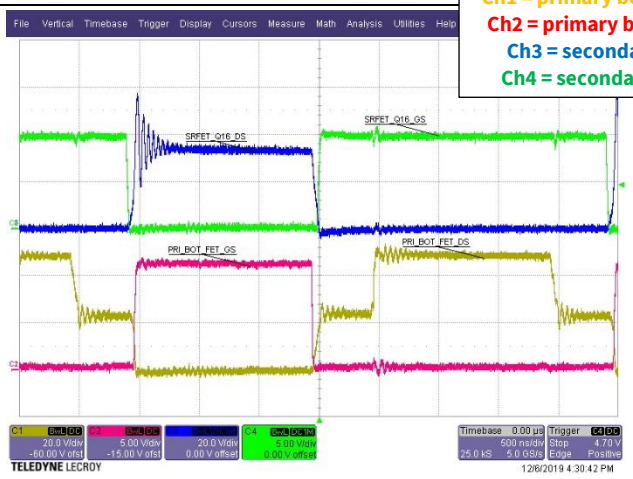
(f)

Figure 36 Input line-transient waveforms

6.6 Primary and secondary gate-drive signals

The following waveforms were taken to show the optimization of dead-time between the primary and secondary MOSFETs in an isolated eighth-brick HB-CT converter. This experiment was conducted over the line and load range per the specifications of the converter.

Ch1 = primary bottom FET V_{ds}, 20 V/div
Ch2 = primary bottom FET V_{gs}, 5 V/div
Ch3 = secondary Q16 V_{ds}, 20 V/div
Ch4 = secondary "Q16" V_{gs}, 5 V/div



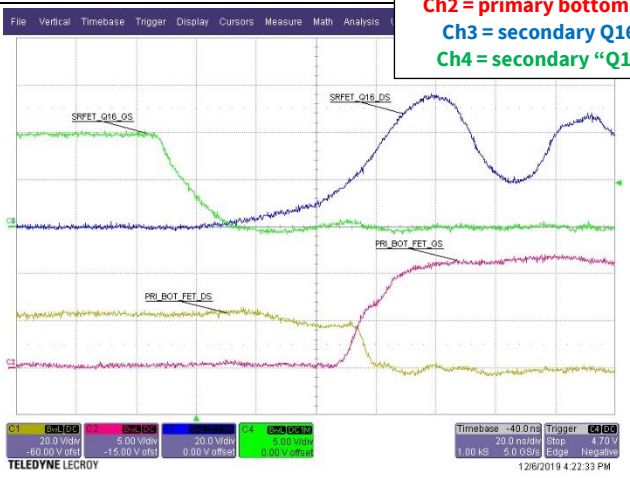
48 V, 12 V_{OUT}, 0 A

(1)

48 V, 12 V_{OUT}, 0 A, zoomed in on SR FET rising

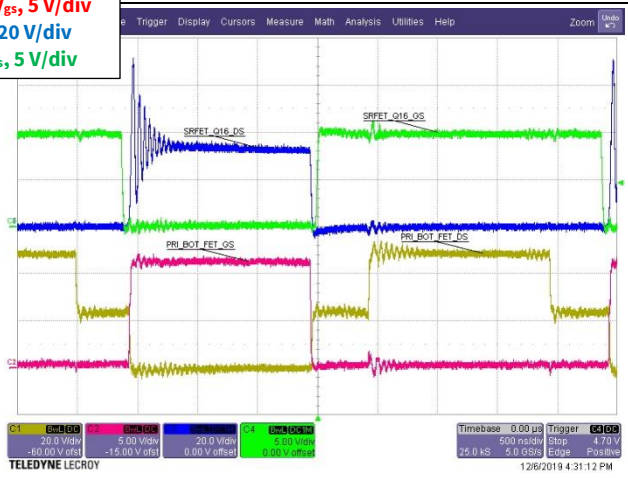
(2)

Ch1 = primary bottom FET V_{ds}, 20 V/div
Ch2 = primary bottom FET V_{gs}, 5 V/div
Ch3 = secondary Q16 V_{ds}, 20 V/div
Ch4 = secondary "Q16" V_{gs}, 5 V/div



48 V, 12 V_{OUT}, 0 A, zoomed in on SR FET falling

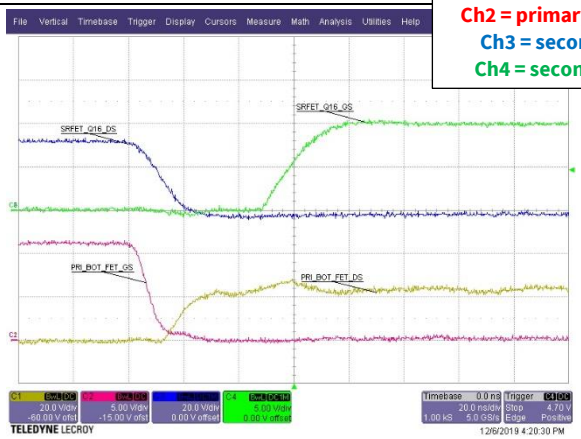
(3)



48 V, 12 V_{OUT}, 10A

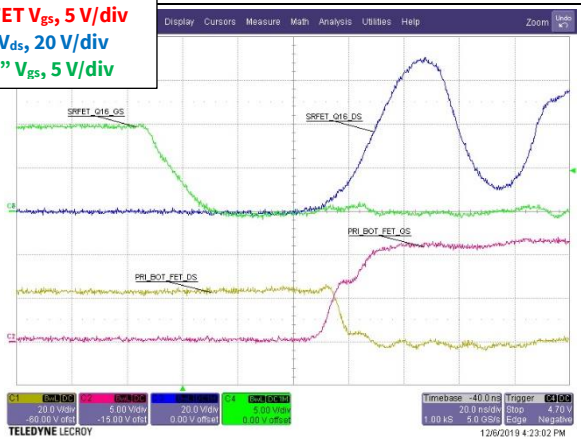
(4)

Ch1 = primary bottom FET V_{ds}, 20 V/div
Ch2 = primary bottom FET V_{gs}, 5 V/div
Ch3 = secondary Q16 V_{ds}, 20 V/div
Ch4 = secondary "Q16" V_{gs}, 5 V/div



48 V, 12 V_{OUT}, 10 A, zoomed in on SR FET rising

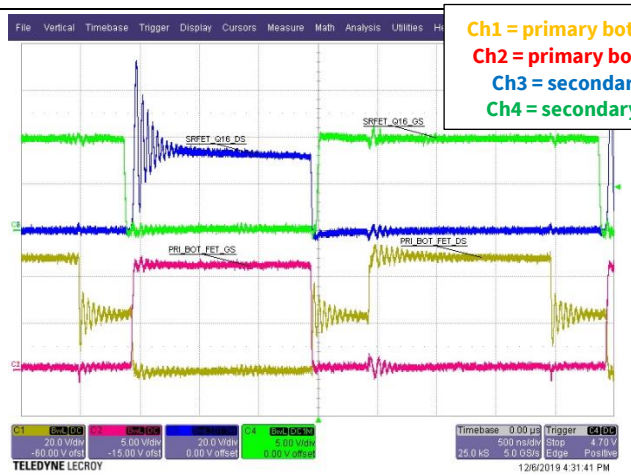
(5)



48 V, 12 V_{OUT}, 10 A, zoomed in on SR FET falling

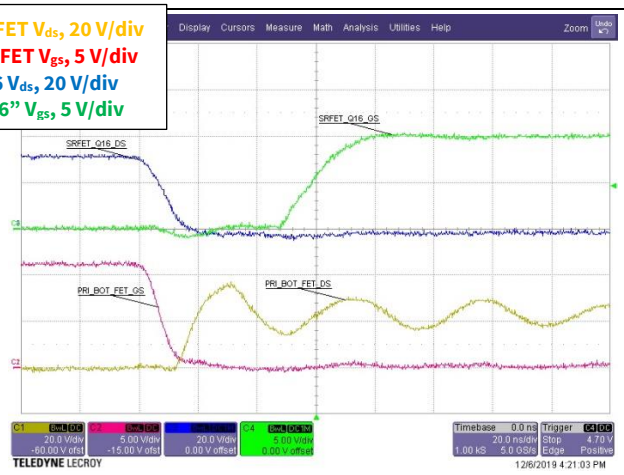
(6)

Operation waveforms



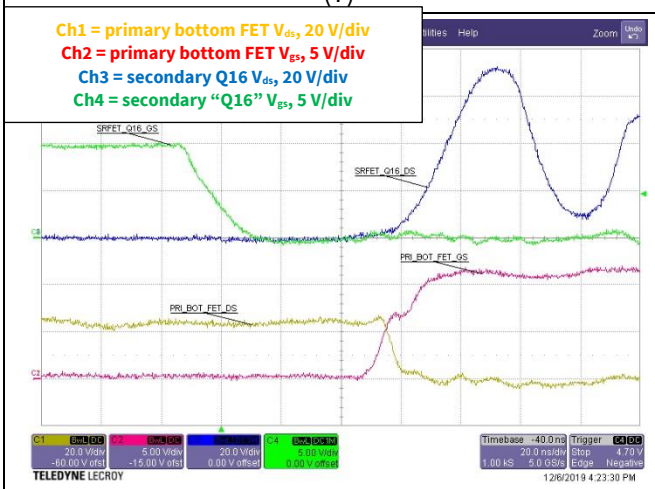
48 V, 12 V_{OUT}, 20 A

(7)



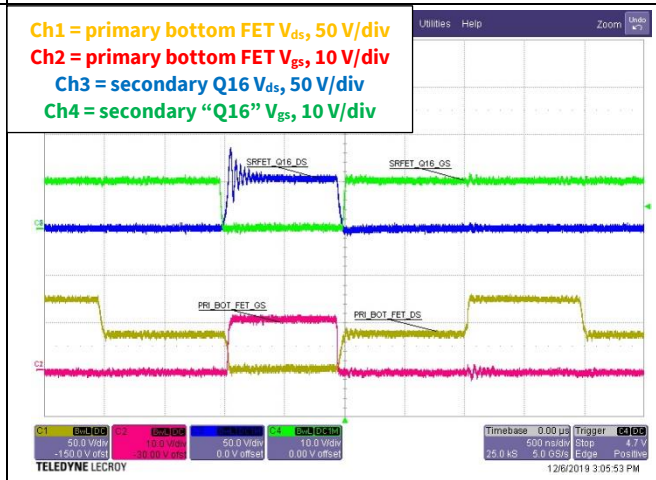
48 V, 12 V_{OUT}, 20 A, zoomed in on SR FET rising

(8)



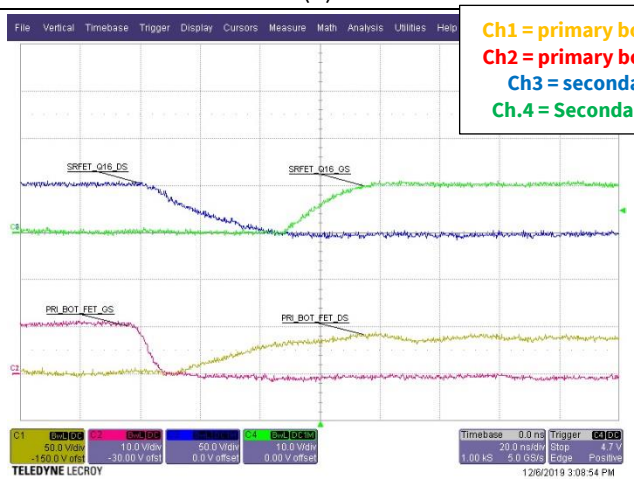
48 V, 12 V_{OUT}, 20 A, zoomed in on SR FET falling

(9)



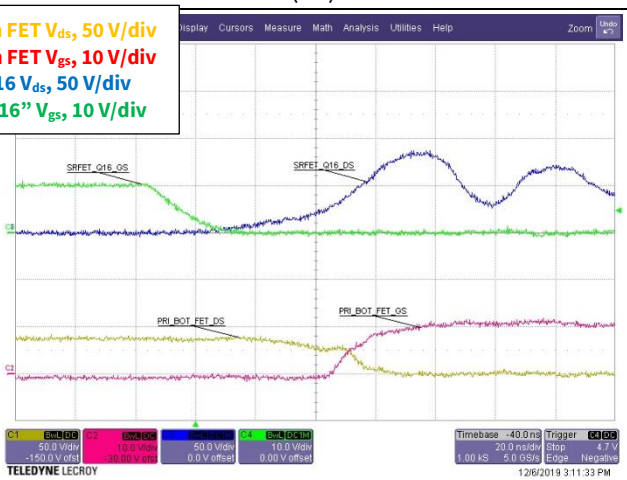
75 V, 12 V_{OUT}, 0 A

(10)



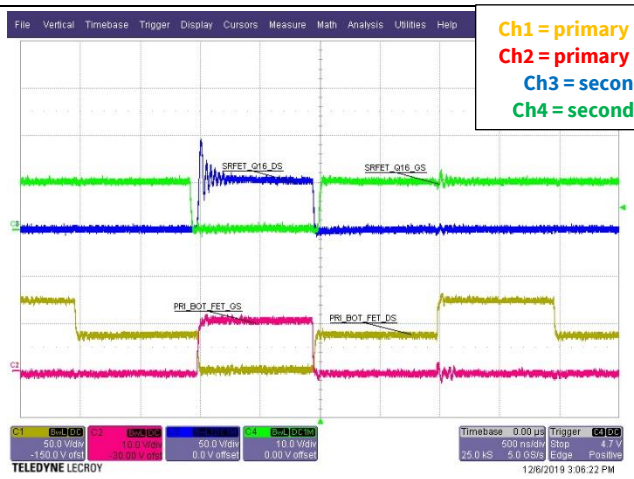
75 V, 12 V_{OUT}, 0 A, zoomed in on SR FET rising

(11)



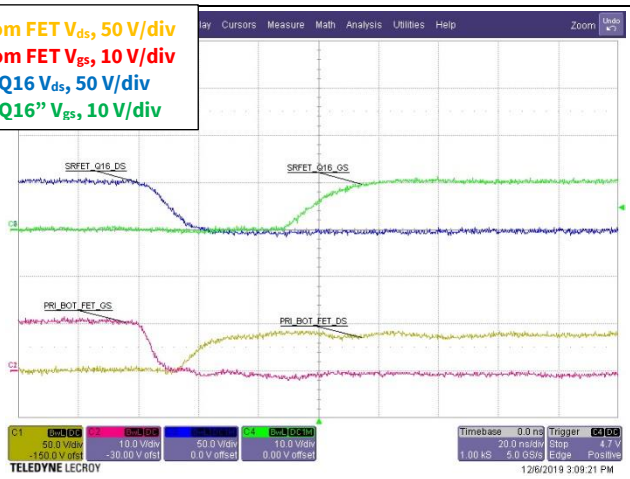
75 V, 12 V_{OUT}, 0 A, zoomed in on SR FET falling

(12)



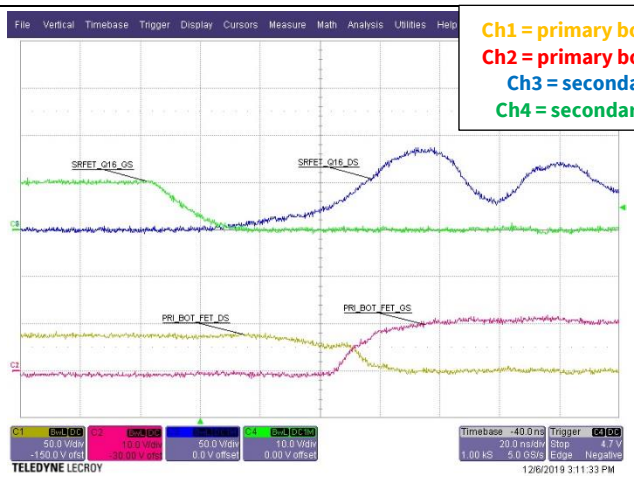
75 V, 12 V_{OUT}, 10 A

(13)



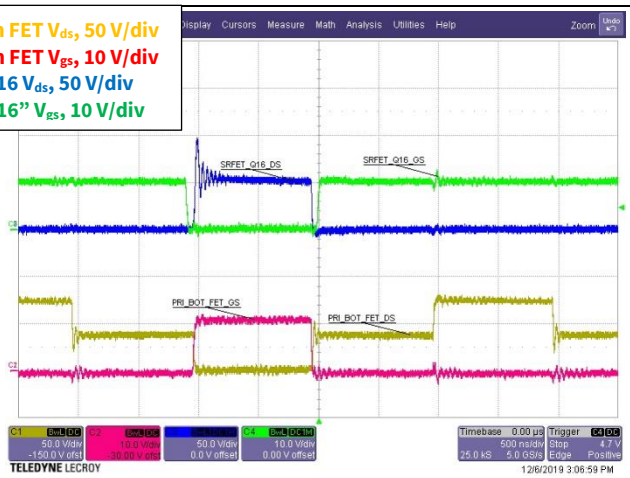
75 V, 12 V_{OUT}, 10 A, zoomed in on SR FET rising

(14)



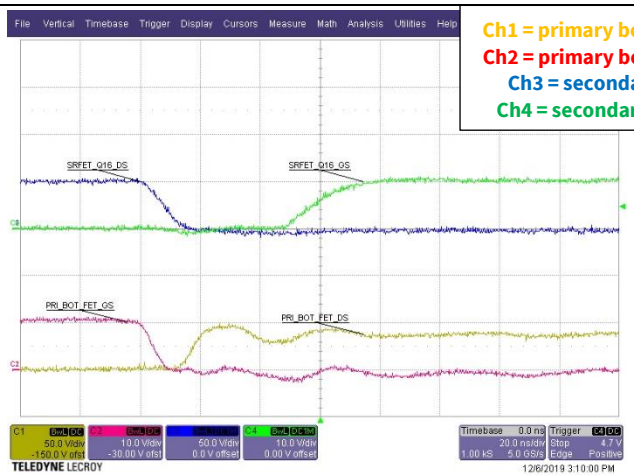
75 V, 12 V_{OUT}, 10 A, zoomed in on SR FET falling

(15)



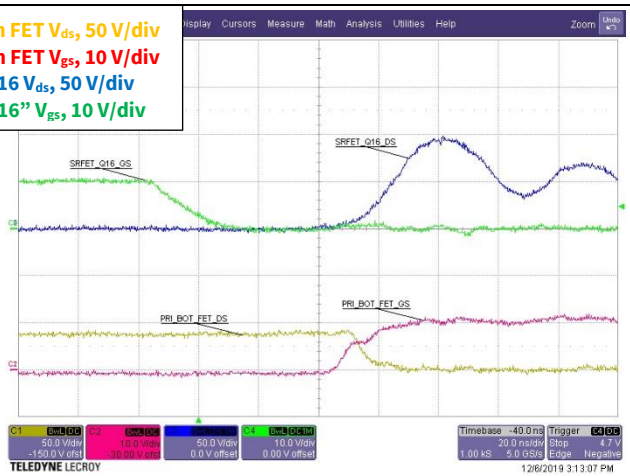
75 V, 12 V_{OUT}, 20 A

(16)



75 V, 12 V_{OUT}, 20 A, zoomed in on SR FET rising

(17)



75 V, 12 V_{OUT}, 20 A, zoomed in on SR FET falling

(18)

Figure 37 Primary and secondary gate-drive waveforms

6.7 Burst mode operation

To increase light load efficiency, the converter enters burst mode to reduce switching losses. When the load current falls below the desired entry current level, the converter enters burst mode operation. The converter stops switching when entering burst (burst-off). Switching is resumed when output voltage drops to a target level. This target level defines output voltage ripple in burst mode. In burst mode, PID output is frozen to the same duty-cycle that the system operates before entering burst mode. Thus during burst-on period, the converter works in constant on-time mode. The SRs are turned off during burst mode. For bridge topologies, the positive and negative half-cycles occur in pairs. After the negative half-cycle, all switches remain off until the output voltage falls to the pre-defined target to restart another burst of PWM pulses.

For in-depth information on burst mode, please refer to the burst mode application note available from the Infineon website.

Primary gate drive with burst mode enabled:
pid0_burst_mode_ith = 7 (2.94 A), pid0_burst_mode_err_thr = 8 (101 mV), and 0x34 POWER_MODE = 0.

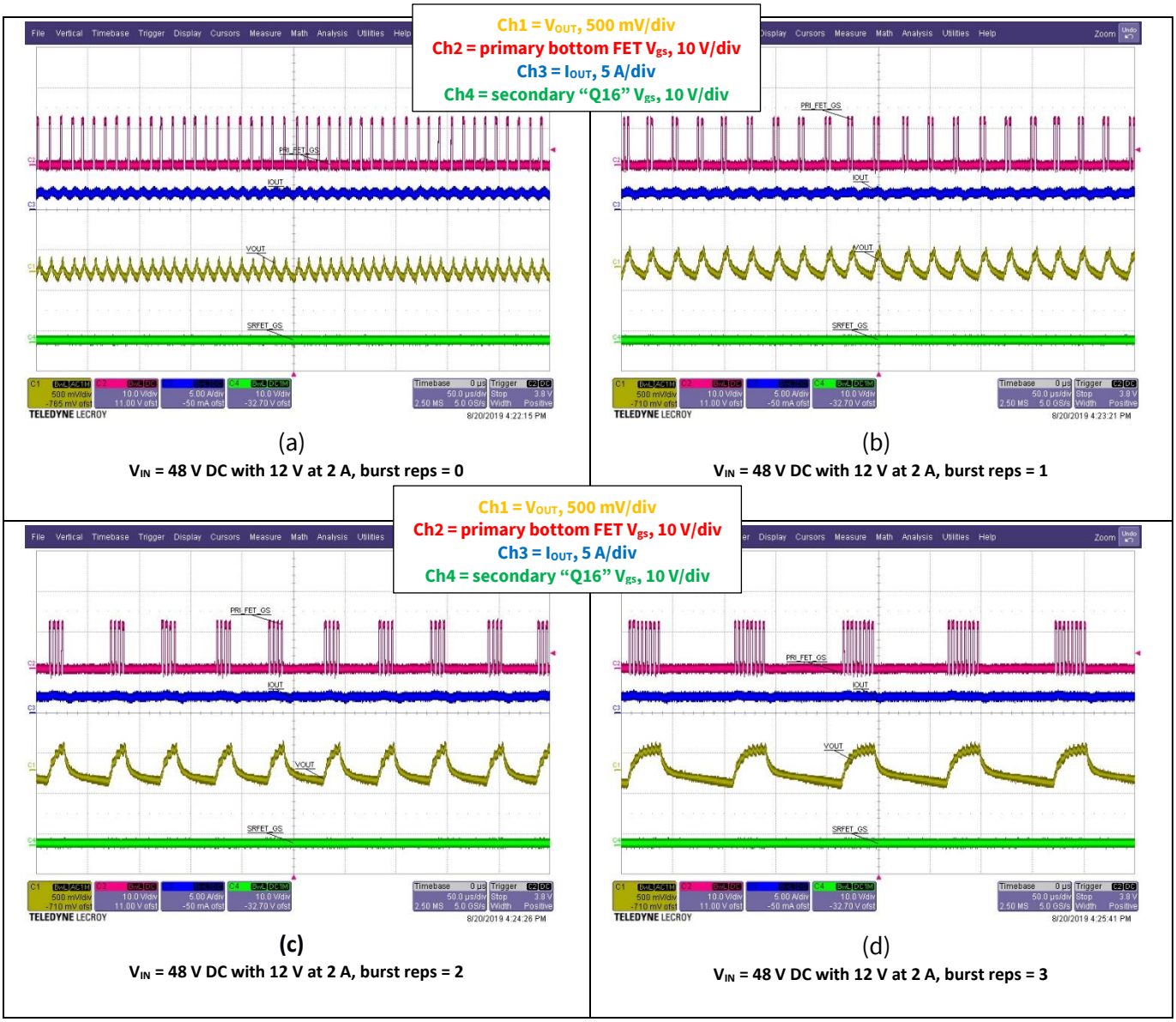


Figure 38 Burst mode operation

Operation waveforms

Figure 39 summarizes the efficiency improvement by comparing the input power drawn in regular mode (POWER MODE = 0) and burst mode (POWER MODE = 3). The burst reps selected for the test was 0, i.e. 1 cycle. The burst reps can be selected from 1 cycle to 8 cycles in powers of 2 for different output choke and capacitor values to achieve the best burst mode efficiency. For this demo board reps = 0 or 1 cycle resulted in the best efficiency.

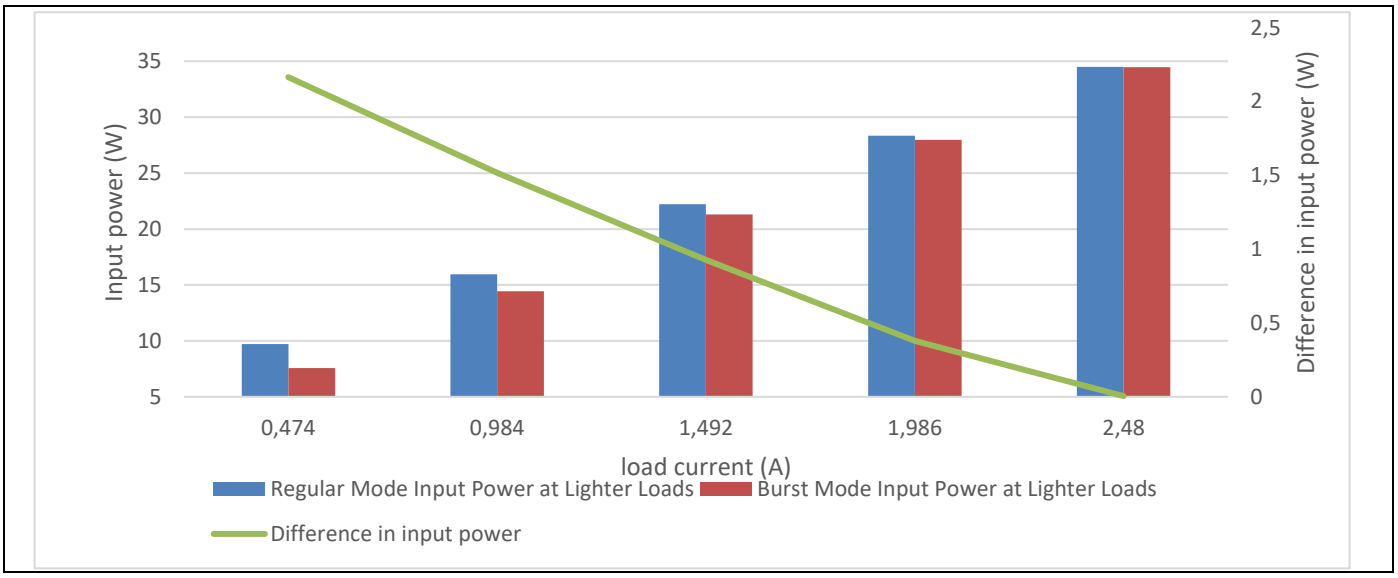


Figure 39 Burst mode input power reduction

7 Protections

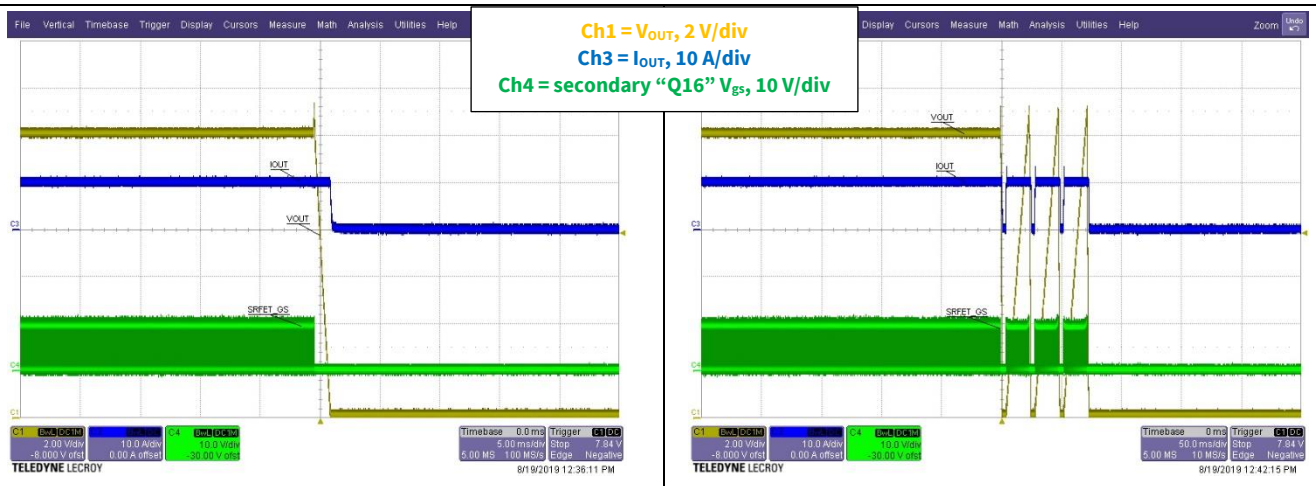
In this section, input and output fault protections are verified with different types of fault response. The default fault thresholds and fault responses of the board are listed below.

Table 8 Default fault protection configuration

Protection type		Typ. (PMBus configurable)	Unit
Output over-voltage	Fault limit threshold	15.6	V
	Warning limit threshold	14.6	V
	Fault response	Disable and retry, no retry	
Output under-voltage	Fault limit threshold	8	V
	Warning limit threshold	9	V
	Fault response	Ignore fault	
Output over-current	Fault limit threshold	27	A
	Warning limit threshold	25	A
	Fault response	Shut down, retry once with 2 ms delay	
Output under-current	Fault limit threshold	-128	A
	Fault response	Disable and retry, no retry	
Over-temperature	Fault limit threshold	125	°C
	Warning limit threshold	90	°C
	Fault response	Disable and resume when OK, fault clears when on-board NTC temperature falls below the warning limit	
Under-temperature	Fault limit threshold	-40	°C
	Warning limit threshold	-30	°C
	Fault response	Ignore fault	
Input over-voltage	Fault limit threshold	80	V
	Warning limit threshold	78	V
	Fault response	Disable and retry, no retry	
Input under-voltage	Fault limit threshold	33	V
	Warning limit threshold	30	V
	Fault response	Ignore fault	
Input over-current	Fault limit threshold	9	A
	Warning limit threshold	8.5	A

Protection type		Typ. (PMBus configurable)	Unit
	Fault response	Disable and retry, no retry	
Max. output voltage turn-on rise time	Fault limit threshold	255	ms
	Fault response	Ignore fault	
Output over-current fast fault or short-circuit	Fault limit threshold	30	A
	Fault response	Shut down and no retry	

7.1 Output OVP



48 V input, 10 A load, disable and no retry

(c)

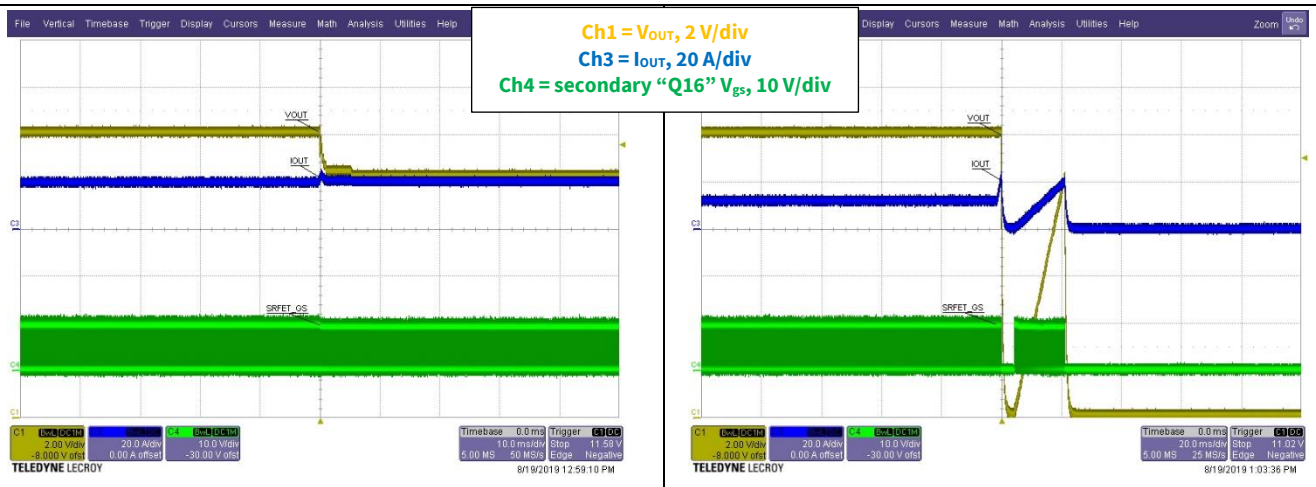
48 V input, 10 A load, disable and three retries

(d)

Figure 40 Output OVP waveform

7.2 Output OCP

Set e-load to CR mode for this test.

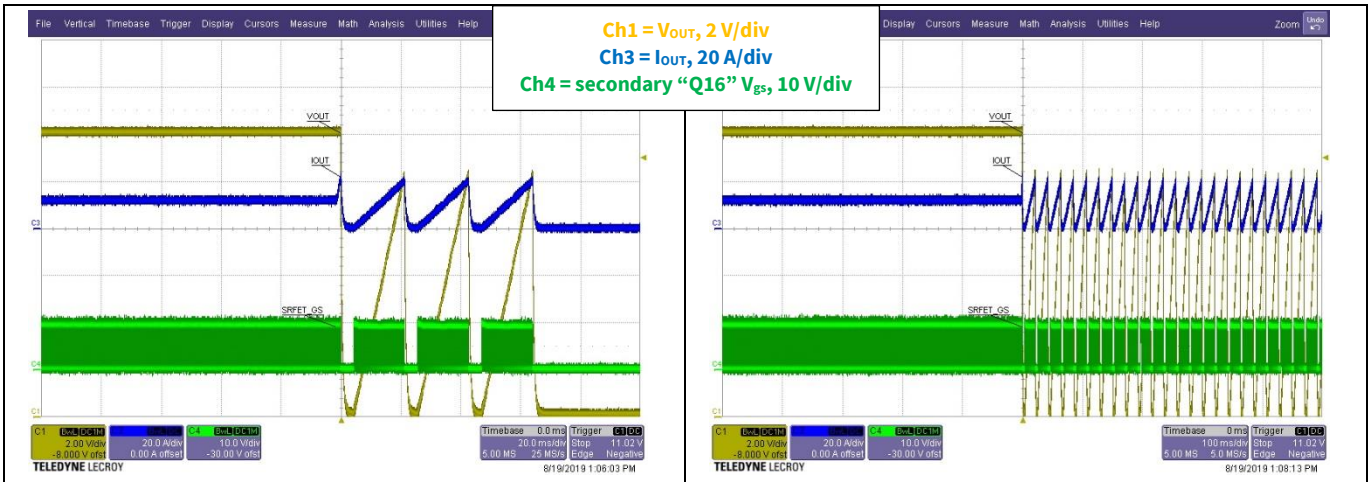


48 V input, 20 A to over-current, constant current

(a)

48 V input, 20 A to over-current, shut down and retry with one retry

(b)



48 V input, 20 A to over-current, shut down and retry with three retries

(a)

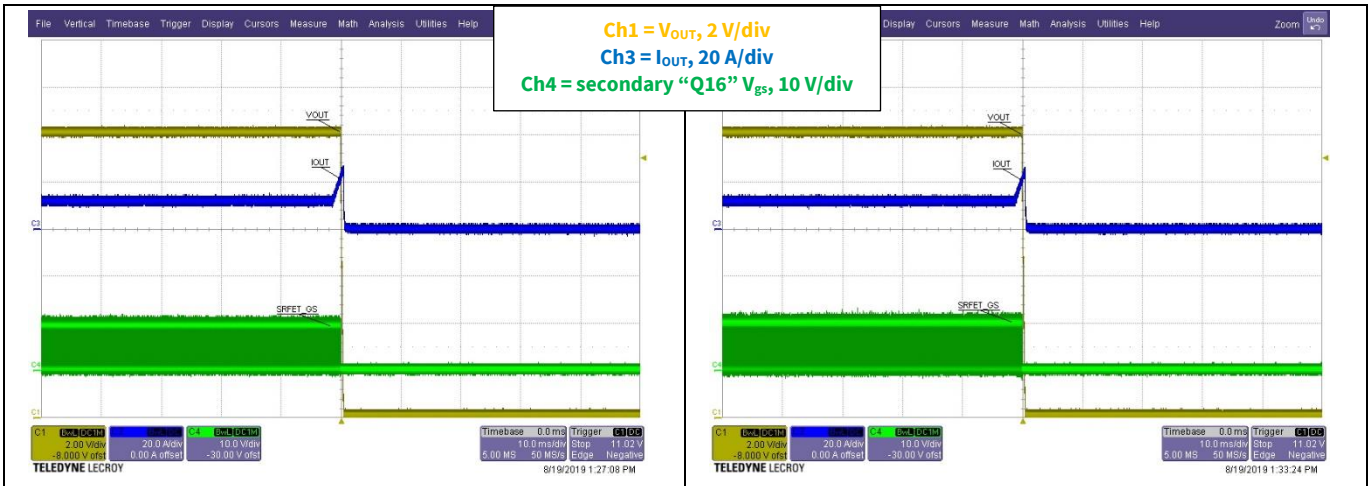
48 V input, 20 A to over-current, shut down and retry with continuous retry

(b)

Figure 41 Output OCP waveforms

7.3 Output short-circuit protection

The output was shorted by using two different methods. The first output over-load was applied with the load bank or e-load short-circuit, and in the second method, the unit was started with a direct short across the converter output terminals.



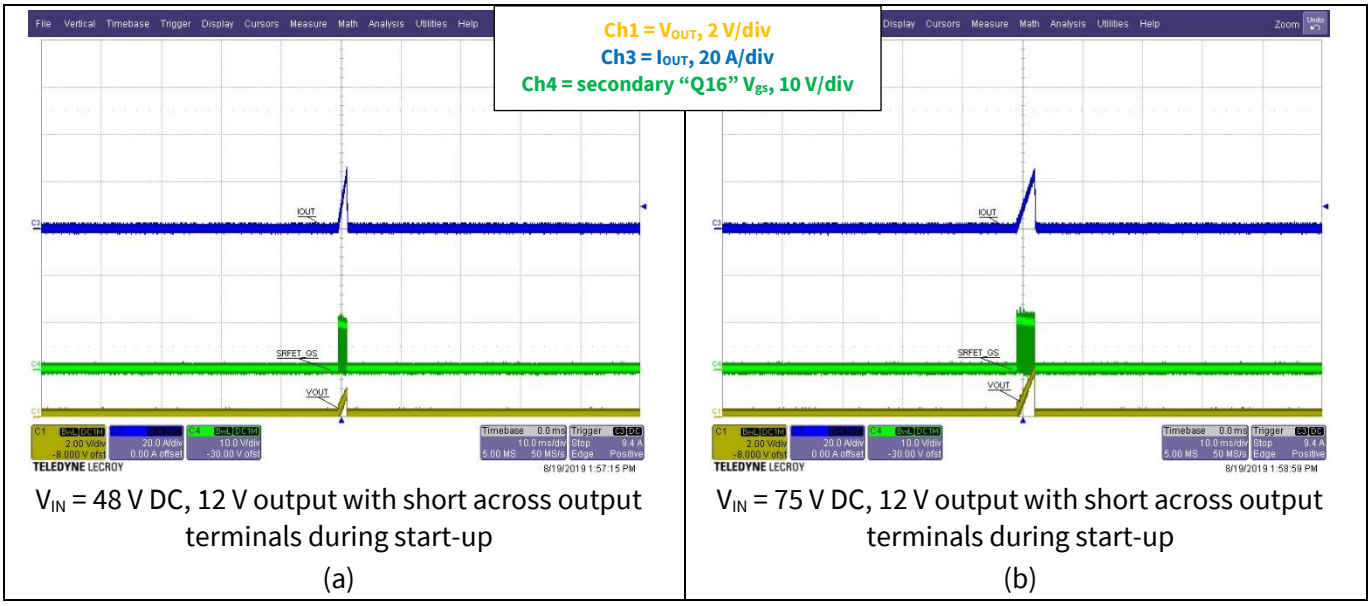
V_{IN} = 48 V DC with 12 V at 20 A, short-circuit with load bank

(a)

V_{IN} = 75 V DC with 12 V at 20 A, short-circuit with load bank

(b)

Figure 42 Output short-circuit waveforms using load bank for short



V_{IN} = 48 V DC, 12 V output with short across output terminals during start-up

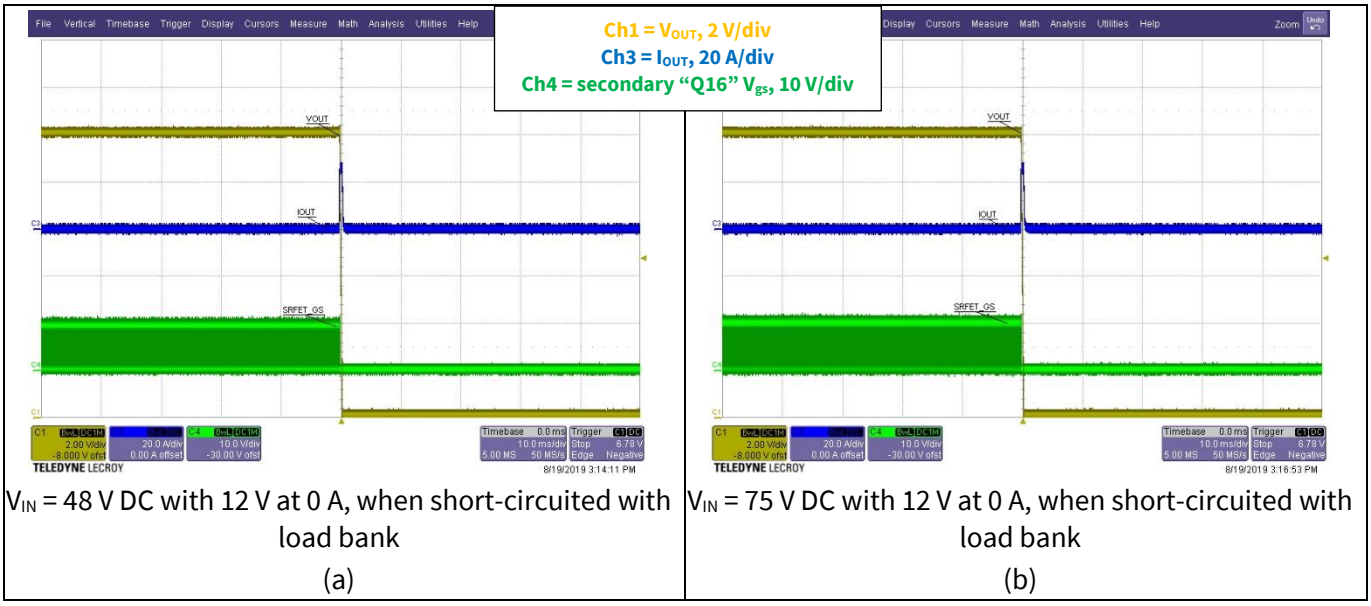
(a)

V_{IN} = 75 V DC, 12 V output with short across output terminals during start-up

(b)

Figure 43 Output short-circuit waveforms using direct short across output

For MFR_IOUT_OC_FAST test, set normal output fault current limit (IOUT_OC_FAULT_LIMIT) to a value higher than the fast-fault response trip-point to make the system respond only to over-current fast fault. The unit was tested at 20 A with a short-circuit event in between regulation over input line range. This triggered I_{OUT} fast fault after the occurrence of the short-circuit event.

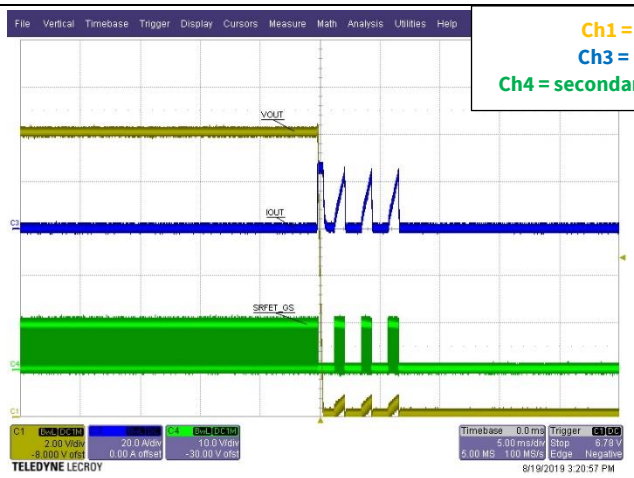


V_{IN} = 48 V DC with 12 V at 0 A, when short-circuited with load bank

(a)

V_{IN} = 75 V DC with 12 V at 0 A, when short-circuited with load bank

(b)



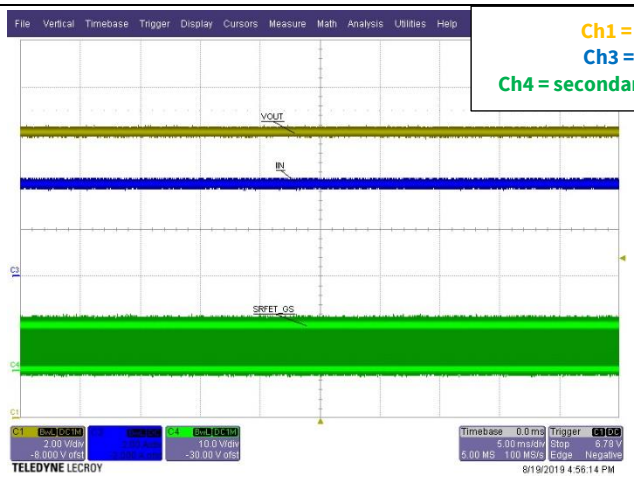
V_{IN} = 48 V DC with 12 V at 0 A, when short-circuited with load bank with three retries

(c)

Figure 44 Output OC fast-fault over-current testing waveforms using load bank

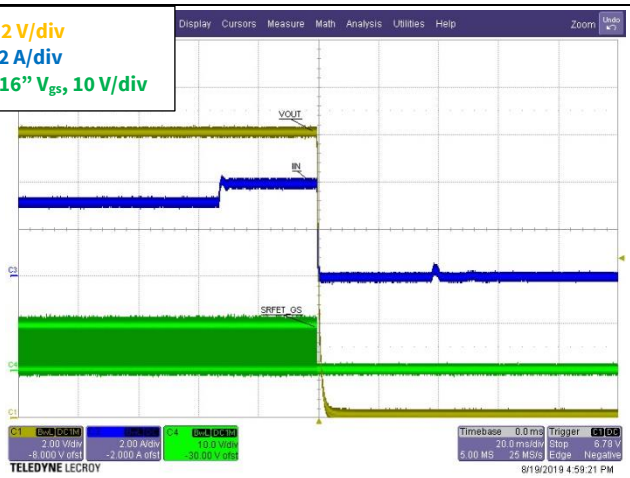
7.4 Input OCP

To carry out this test, input over-current fault and warning thresholds were reduced to 3.5 A and 3.25 A repectively. This was done to avoid interference with output current thresholds.



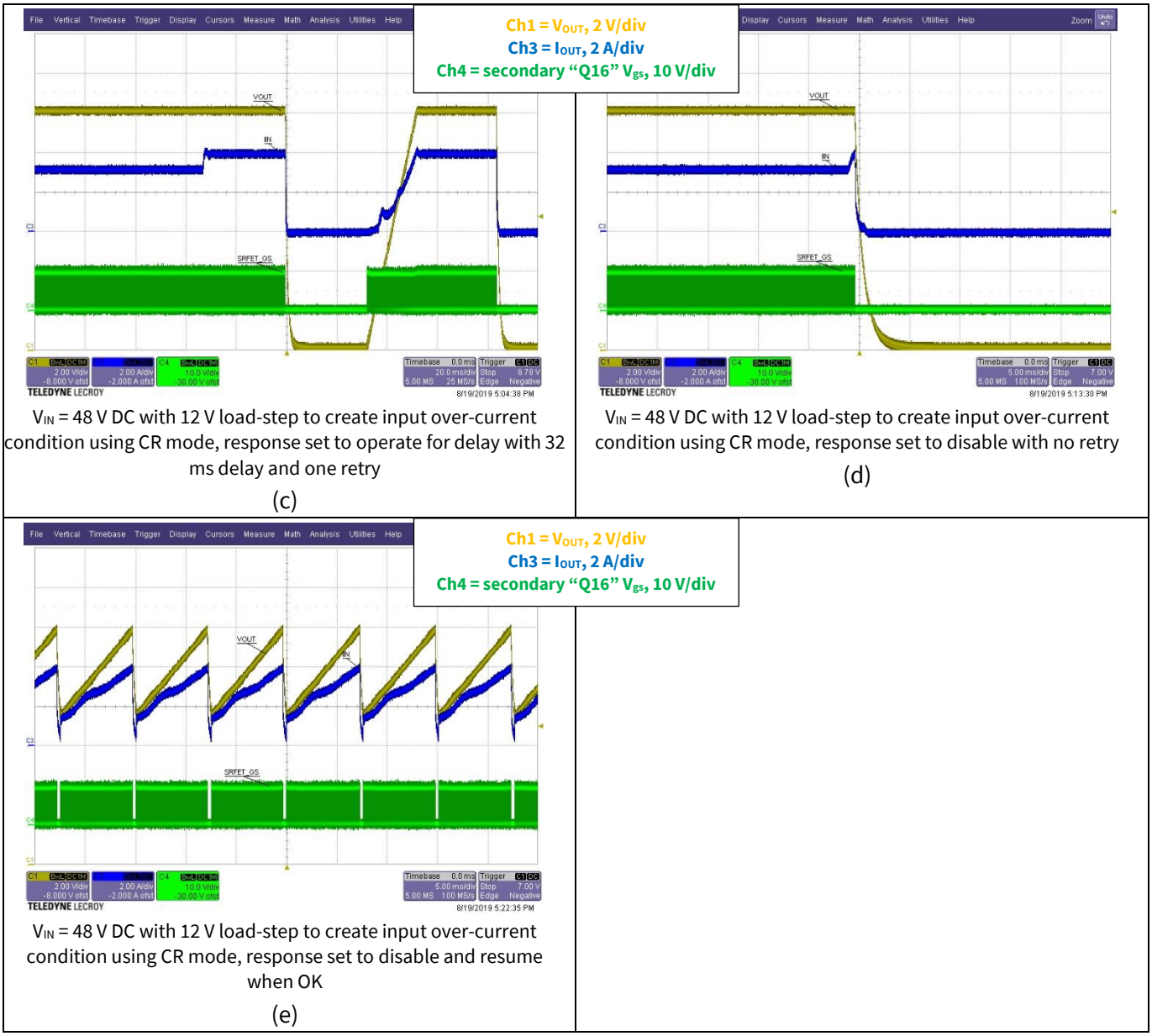
V_{IN} = 48 V DC with 12 V load-step to create input over-current condition using CR mode, response set to ignore

(a)



V_{IN} = 48 V DC with 12 V load-step to create input over-current condition using CR mode, response set to operate for delay with 32 ms delay

(b)



V_{IN} = 48 V DC with 12 V load-step to create input over-current condition using CR mode, response set to operate for delay with 32 ms delay and one retry

(c)

V_{IN} = 48 V DC with 12 V load-step to create input over-current condition using CR mode, response set to disable with no retry

(d)

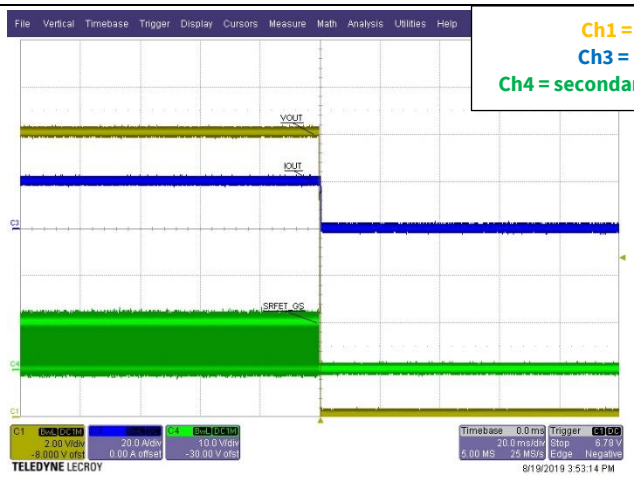
V_{IN} = 48 V DC with 12 V load-step to create input over-current condition using CR mode, response set to disable and resume when OK

(e)

Figure 45 Input over-current limit

7.5 Over-temperature protection

The eighth-brick has a thermistor located next to the CS copper trace. Over-temperature was tested by reducing the airflow to the unit while operating at full load.



V_{IN} = 75 V DC with 12 V at 20 A, over-temperature response set to disable and retry, no retry

(a)

V_{IN} = 75 V DC with 12 V at 20 A, over-temperature response set to disable and resume when OK

(b)

Figure 46 Over-temperature shutdown

8 Active current sharing

Active current sharing involves using a current sharing function, which connects all parallel modules to communicate average current information between modules. The XDPP1100 offers a single-wire active current sharing feature. **Figure 47** shows the active current sharing example with two units in parallel.

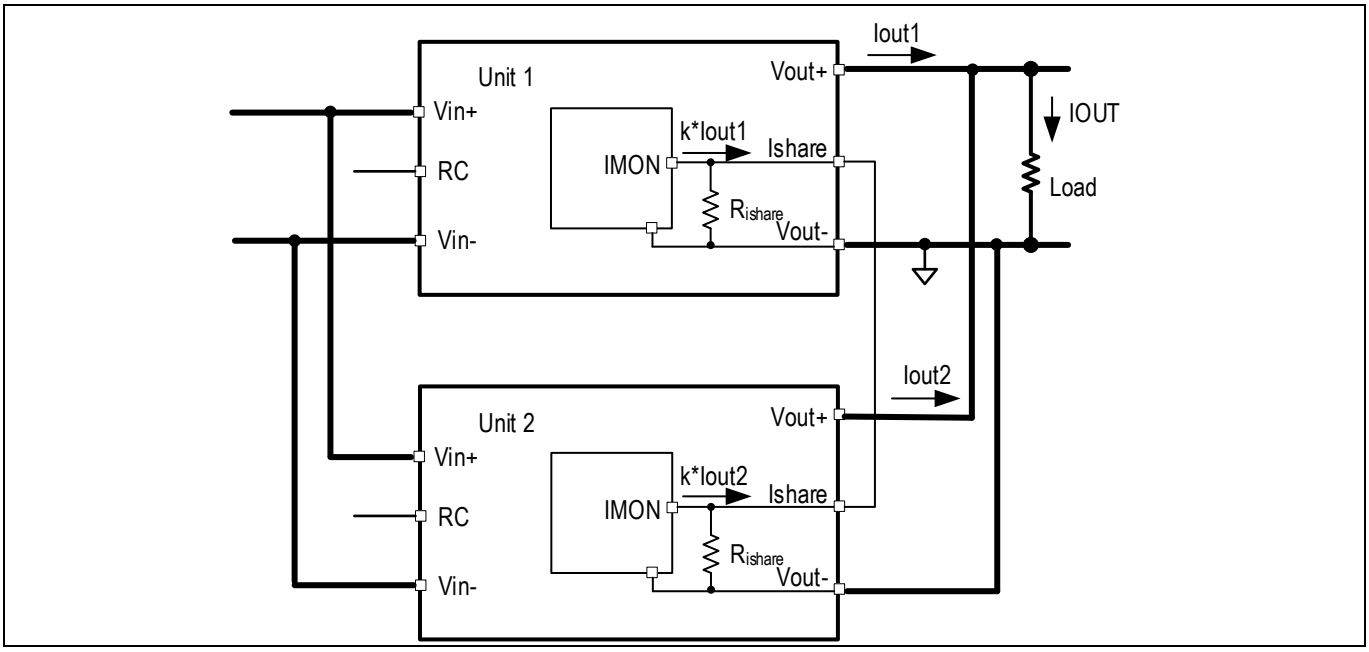


Figure 47 XDPP1100 active current sharing

IMON is an analog DAC output representing the output current. IMON is used for the output current monitor, and for active current balancing between multiple parallel modules. An internal current source proportional to the output current of Loop0 sources current from the IMON pin into the precision sense resistor. The IMON current DAC (IDAC) output current range is 0 to 640 µA. The gain of the current source is configurable, which allows the user to scale the current source per application. At no-load, this source current is 320 µA. IMON source current lower than 320 µA indicates negative current in this module.

A 1.875 kΩ precision resistor (R_{ISHARE}) connected between IMON and ground presents a voltage proportional to the output current of each module. At full load, the IMON voltage will be 1.2 V (640 µA x 1.875 kΩ); and at no-load, IMON voltage is 0.6 V (320 µA x 1.875 kΩ).

Connecting the IMON of each module together allows the XDPP1100 to detect the level of average current.

$$IOUT = Iout1 + Iout2 + \cdots + Ioutn$$

$$V_{IMON} = (k \cdot Iout1 + k \cdot Iout2 + \cdots + k \cdot Ioutn) \times \frac{R_{ISHARE}}{n} = k \cdot R_{ISHARE} \times \frac{IOUT}{n}$$

I_{OUT} is total current supplied to load, *n* is the number of units that are connected in parallel, *k* is the IMON source current scale factor. The voltage of the IMON pin represents the average current.

Each module compares its own output current with the average current, making the corresponding adjustment.

To prevent oscillation on a small error current, a dead-zone applies to the current sharing block. When the error current is less than the dead zone, current sharing is inactive.

The XDPP1100 provides both positive and negative clamps to voltage adjustment under active current sharing.

Active current sharing

The active current sharing configuration can be done with the GUI design tool, under the “Advanced Features”.

Current sharing during start-up is always more challenging than in steady-state. The power supplies could have different start-up delays or different ramp times due to device variation. The voltage difference between units could be much more than the set-point error in the steady-state.

An added droop feature was implemented in the FW patch. The droop is added during start-up ramp. The added droop helps to reduce the error of current sharing at start-up. It is removed once the power supply reaches regulation, thus the maximum output power won’t be sacrificed. It could be configured by the patched PMBus command 0xFC MFR_ ADDED_DROOP_ DURING_RAMP. Use the “Load PMBus Spread sheet” button to import the MFR PMBus command into GUI. The PMBus command spreadsheet can be found in the GUI installation folder.

More details of current sharing can be found in the XDPP1100 application note.

A test fixture that could fit three eighth-bricks is designed for current sharing testing. In this test, two units were placed in parallel to verify the current sharing performance. Output voltage mis-match was set intentionally to check the worst case.

8.1 Steady-state and transient waveform with TON_DELAY and VOUT_COMMAND mis-match

Unit 1, VOUT_COMMAND = 11.95 V, xaddr 0x40, TON_DELAY = 0 ms, TON_RISE = 20 ms
Unit 2, VOUT_COMMAND = 12.05 V, xaddr 0x41, TON_DELAY = 10 ms, TON_RISE = 20 ms

Current sharing register settings: ishr_kp = 0, ishr_ki = 20, ishr_scale = 24 (21 A), ishare_clamp_neg = 40, ishare_clamp_pos = 40, MFR_ISHARE_THRESHOLD = F805 (2.5 A)

Ch1: V_{OUT} (2 V/div), Ch2: I_{OUT} of unit 1 (5 A/div), Ch3: IMON pin (0.5 V/div), Ch4: I_{OUT} of unit 2 (5 A/div)

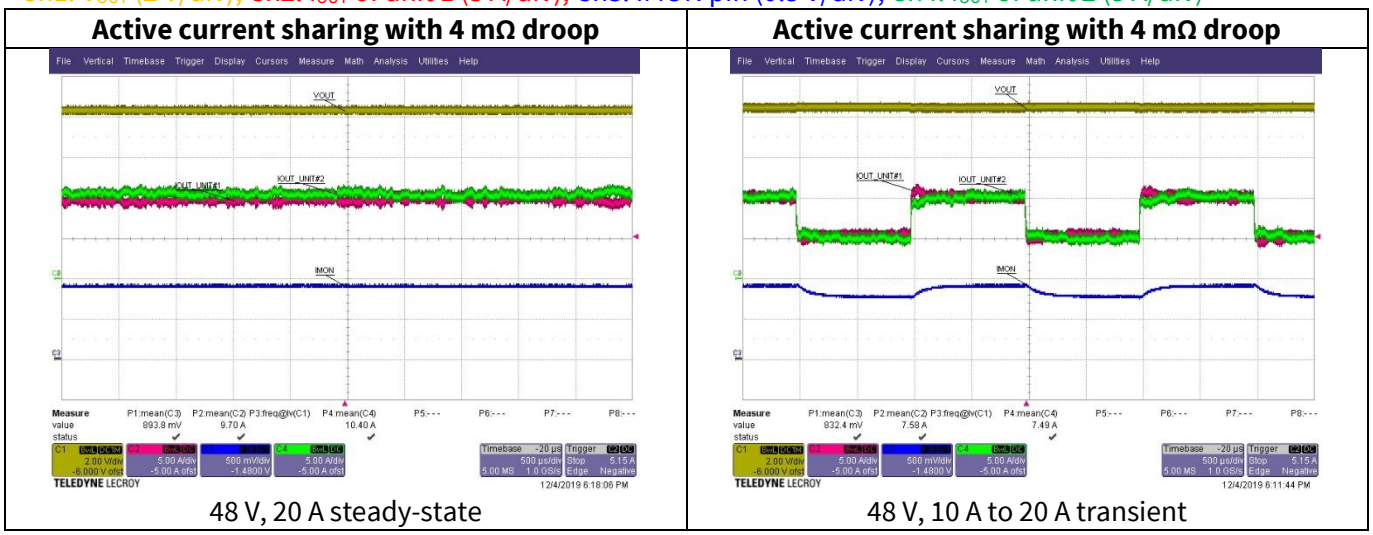


Figure 48 Steady-state and transient waveforms with VOUT_COMMANDand TON_DELAY mis-match

9 Mechanical outline

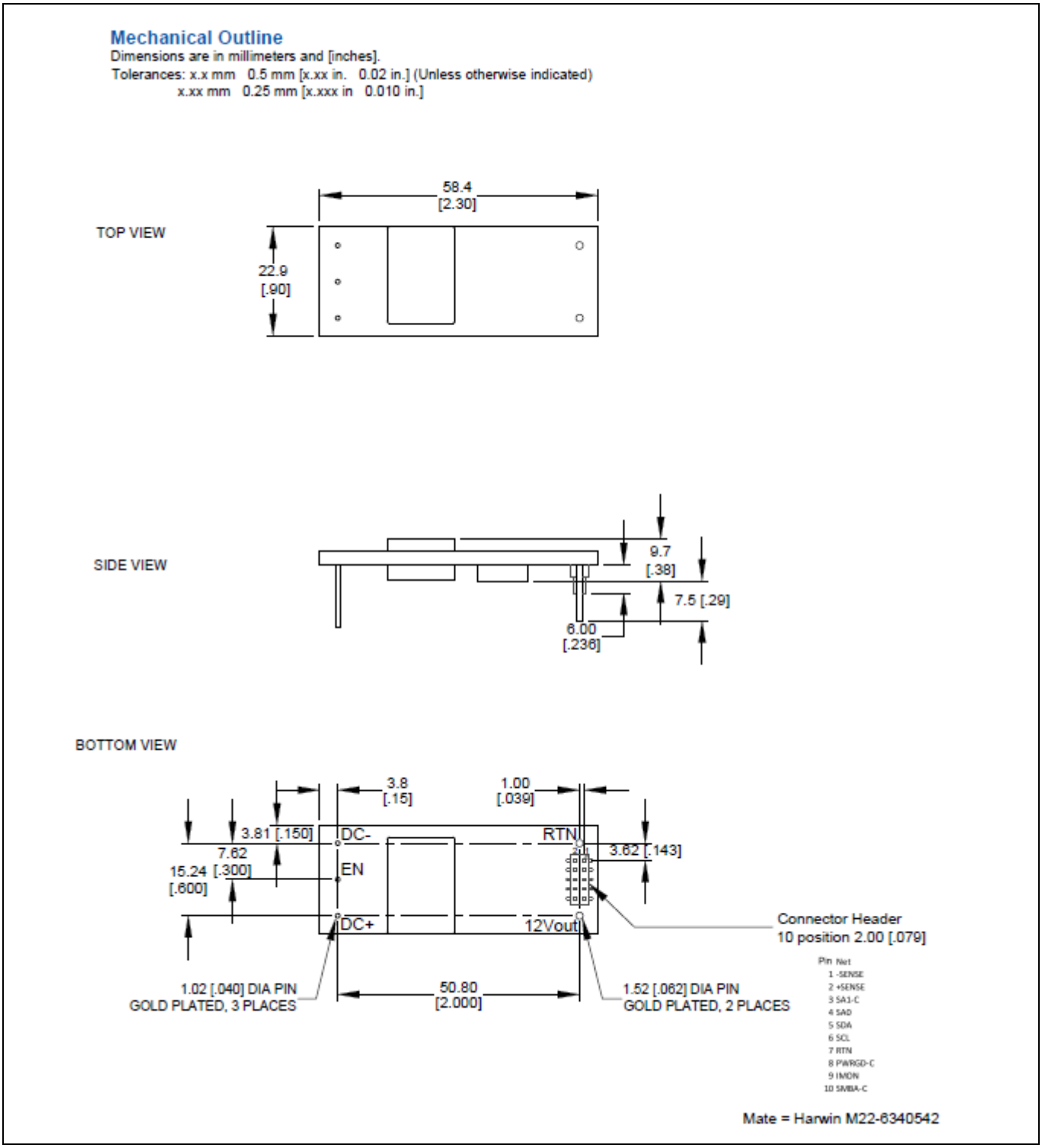


Figure 49 Board mechanical outline

10 Summary

This document introduces a complete Infineon system solution for a telecom 275 W HB-CT isolated DC-DC converter from 36 V DC to 75 V DC, achieving over 95 percent peak efficiency. The achieved power density is in the range of 21 W/cm^3 (350 W/in^3), which is enabled by the use of Infineon's XDPP1100 (XDPP1100 is a digital controller based on a 32-bit, 100 MHz ARM® Cortex™-M0 RISC microprocessor), OptiMOS™ MOSFETs and EiceDRIVER™ gate drivers, an optimized layout and the use of planar magnetics.

The XDPP1100 is a digital power supply controller offering superior levels of integration and performance in a single-chip solution. The flexible nature of the IC makes it suitable for a wide variety of power conversion applications. Multiple peripherals inside the device have been specifically optimized to enhance the performance of isolated DC-DC applications and reduce the solution component count in the IT and network infrastructure space.

Specific power management peripherals have been added to enable high efficiency across the entire operating range, high integration for increased power density, reliability, and lowest overall system cost and high flexibility with support for the widest number of control schemes and topologies. Such peripherals include: light-load burst mode, synchronous rectification, input voltage feed-forward, copper trace current sense with temperature compensation, ideal diode emulation, constant current constant power control, flux balancing, input voltage sensing on the secondary side, soft-start with pre-bias, feedback open-loop or short-circuit protection, as well as several other features. Topology support has been optimized for voltage mode and current mode controlled hard-switched full-bridge and half-bridge, phase-shifted full-bridge, active clamp forward, interleaved active clamp forward, interleaved half-bridge, and interleaved full-bridge. A dual-rail version also supports pre-buck or post-buck configuration.

Infineon's DHP1050N10N5 is used as a primary half-bridge module in this demo board. This is a 100 V integrated power stage and bootstrap driver that offers a combination of low $R_{DS(on)}$ and fast-switching OptiMOS™ technology and the optimized half-bridge driver in a small PQFN package. An 80 V OptiMOS™ 5 BSC040N08NS5 SuperS08 power transistor as SRFET, combined with an optimized layout and an optimized driving circuitry achieves incomparable performance with minimum stress on the devices. The secondary OptiMOS™ FETs are driven from Infineon's 2EDN7524G EiceDRIVER™ gate driver. The EiceDRIVER™ 2EDN is a family of advanced dual-channel MOSFET gate-driver ICs suitable for driving CoolMOS™, OptiMOS™, standard MOSFETs, superjunction MOSFETs, IGBTs and GaN power devices.

11 References

[1] XDPP1100 datasheet

[2] XDPP1100 GUI installation and user guide

[3] XDPP1100 Isolated 48 V to 12 V 600 W quarter-brick converter

Revision history

Document version	Date of release	Description of changes
V1.0	2020-03-02	First release

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