1000 W 400 V phase-shifted full-bridge current-doubler with XDPP1100 and CoolGaN™

Application note

About this document

Scope and purpose

This document describes the reference design (REF_XDP_1000W_GAN_PSFB) of an isolated 400 V DC to 12 V DC phase-shifted full-bridge with current-doubler (PSFB-CDR) solution using the **XDPP1100** digital controller. This reference design provides a fully programmable and configurable power converter with an efficiency of up to 95.36 percent and a power density of 67 W/inch. It has fast line-transient and load-transient performance using a hardware-based PID controller module and best-in-class hardware-based feed-forward (FF) response, which enables superior output voltage regulation under light load conditions. PMBus and I^2C communication are integrated to facilitate system configuration and control as well as telemetry updating and fault monitoring. In addition, this REF_XDP_1000W_GAN_PSFB is equipped with **IGT60R070D1** high-voltage (HV) gallium nitride (GaN) FETs, which enable high switching frequency operation at 350 kHz.

REF_XDP_1000W_GAN_PSFB performance and test results are presented in this document. This design can be used as a basis for further power supply development.

Intended audience

Power supply design engineers, system engineers, embedded power designers.

Table of contents

Abbreviations

PSFB	Phase-shifted full-bridge
CDR	Current-doubler
OCP	Overcurrent protection
OVP	Overvoltage protection
OPP	Overpower protection
FF	Feed-forward
GaN	Gallium nitride
FET	Fieldeffect transistor
FOM	Figure of merit
AFE	Analog front end
SR	Synchronous rectification
SMPS	Switched-mode power supply
ZVS	Zero voltage switching

Important notice

“Evaluation boards and reference boards” shall mean products embedded on a printed circuit board (PCB) for demonstration and/or evaluation purposes, which include, without limitation, demonstration, reference and evaluation boards, kits and design (collectively referred to as “reference boards”).

The evaluation and reference boards and the information presented in this document are solely intended to support designers of applications to evaluate the use of Infineon Technologies products in the intended application.

Environmental conditions have been considered in the design of the evaluation and reference boards provided by Infineon Technologies. The design of the evaluation and reference boards is **tested by Infineon Technologies only as described in this document**. The design is not qualified in terms of safety requirements, manufacturing and operation over the entire operating temperature range or lifetime.

The evaluation and reference boards provided by Infineon Technologies **are subject to functional testing only under typical load conditions**. Evaluation and reference boards are not subject to the same procedures as regular products regarding returned material analysis (RMA), process change notification (PCN) and product discontinuation (PD).

Evaluation and reference boards are not commercialized products and are intended to be used solely for evaluation and testing purposes. They shall, in particular, not be used for reliability testing or production. Hence, the evaluation and reference boards may not comply with CE or similar standards (including but not limited to the EMC Directive 2004/EC/108 and the EMC Act) and may not fulfill other requirements of the country in which they are operated by the customer. The customer shall ensure that each evaluation and reference board will be handled in a way which is compliant with all relevant requirements and standards in the country in which they are operated.

The evaluation and reference boards and any information in this document are addressed **only to qualified and skilled technical staff, for laboratory usage**, and shall be used and managed according to the terms and conditions set forth in this document and in any other related documentation provided with the respective evaluation or reference board.

It is the responsibility of the customer’s technical departments to evaluate the suitability of the evaluation and reference boards for the intended application, and the completeness and correctness of the information provided in this document with respect to such application.

The customer accepts that the evaluation and reference boards are not intended to be used for life-endangering applications such as medical, nuclear, military, life-critical or other applications, where failure of the evaluation and reference boards or any results from the use thereof can reasonably be expected to result in personal injury.

The evaluation and reference boards and any information in this document is provided “as is” and Infineon Technologies disclaims any and all warranties, express or implied, including but not limited to warranties of non-infringement of third-party rights and implied warranties of fitness for any purpose, or for merchantability.

Infineon Technologies shall not be responsible for any damages resulting from the use of the evaluation and reference boards and/or from any information provided in this document. The customer is obliged to defend, indemnify, and hold harmless Infineon Technologies from and against any claims or damages arising out of or resulting from any use thereof.

Infineon Technologies reserves the right to change this document and/or any information provided herein at any time without further notice.

1 Introduction

In recent years, the trend in the SMPS market has been towards increased power density and optimized cost. In achieving this higher power density, high efficiency is also a key parameter. This is important because heat dissipation must be minimized.

To achieve this goal, fully resonant topologies such as LLC are often considered to be the best approach in this power range and voltage class. However, the 1000 W PSFB-CDR is an example of how the improvement in semiconductor technology and control algorithms enable a simple and well-known topology to reach high efficiency levels traditionally considered out of reach.

The following figure shows a typical SMPS architecture available in the market, and the PSFB-CDR topology acting as the DC-DC converter in the respective power supply design.

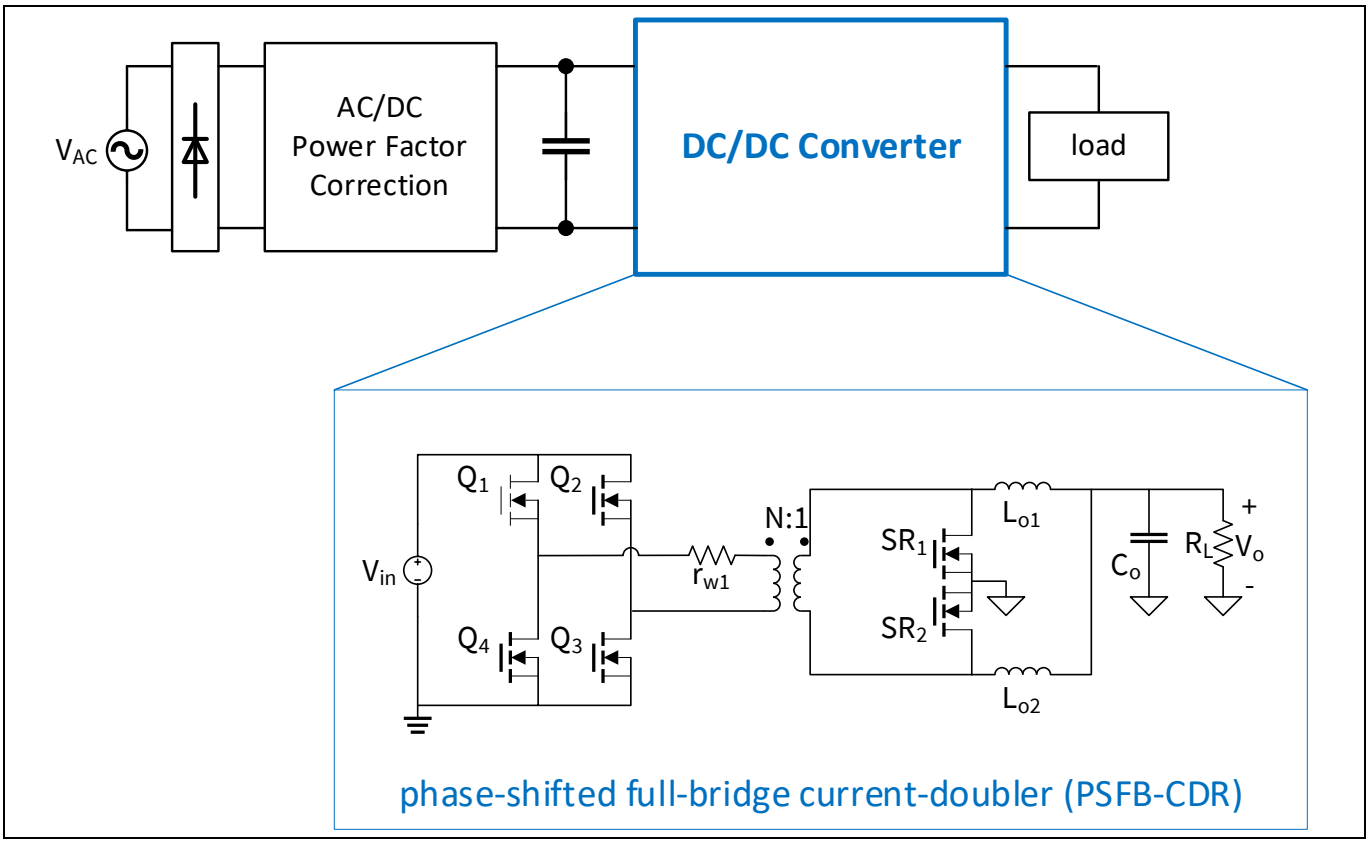

Figure 1 Typical SMPS architecture

1.1 Principle of operation

This section introduces the operating principle of PSFB-CDR by describing the different phases of the current flow through the circuit on a simplified schematic.

As PSFB-CDR uses a transformer, its principle of operation can be understood more easily when it is broken down based on the transformer voltage polarity with respect to its dot convention.

Phase 1 to Phase 4 shows PSFB-CDR operation when the transformer has positive voltage, while Phase 5 to Phase 8 shows PSFB-CDR operation when the transformer has negative voltage.

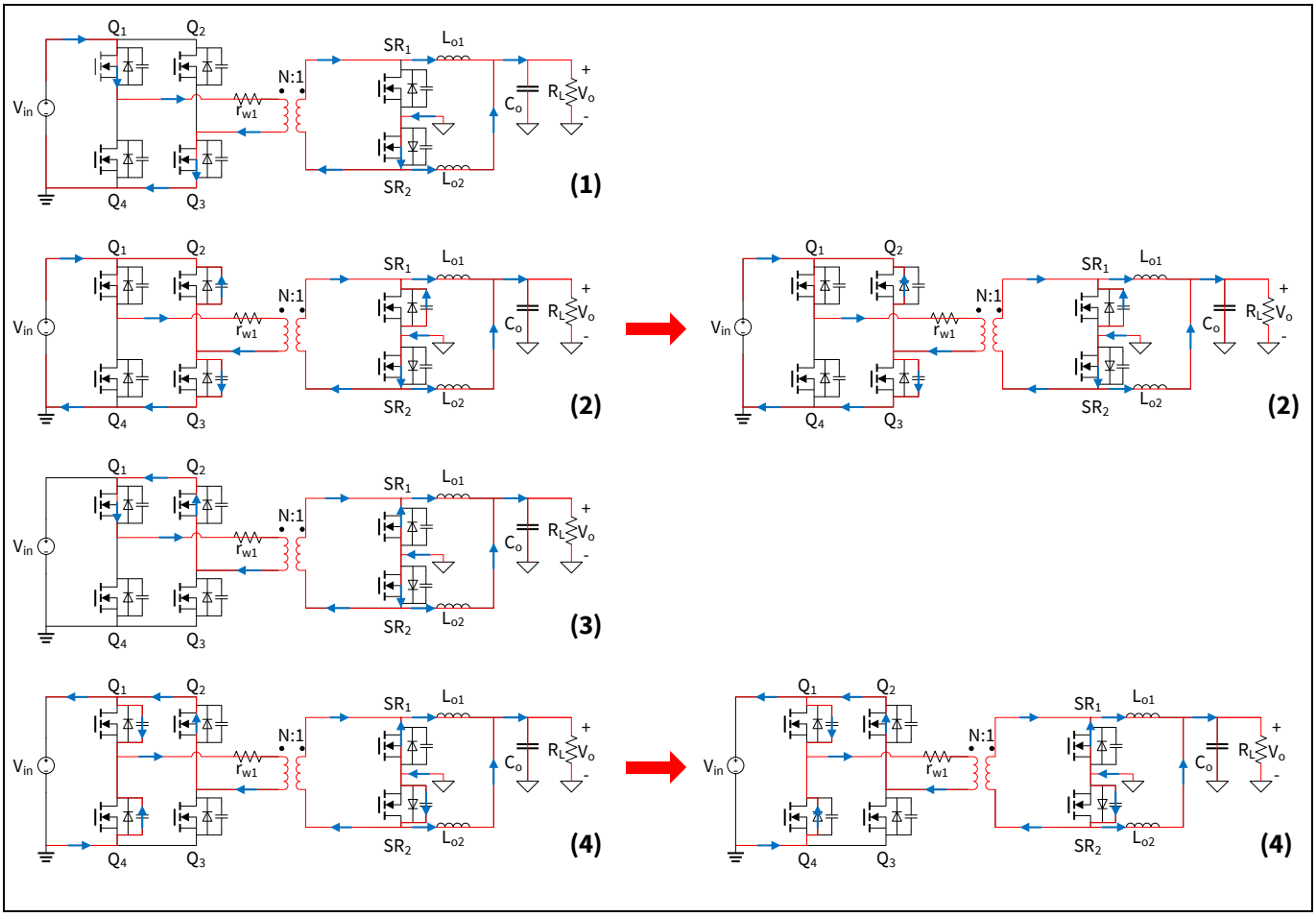

Figure 2 PSFB-CDR operation (Phase 1 to Phase 4)

- **Phase 1**: Power transfer phase

  Q1 and Q3 are turned on and the current is flowing from the primary to the secondary side of the transformer. The transformer secondary voltage V_S is equal to V_{IN} * N_S / N_P. Output inductor L_1 current is charging and output inductor L_2 is discharging.

- **Phase 2**: Switch Q2 ZVS mode

  Q1 stays on but Q3 is turned off. The primary current charges Q3 capacitance and discharges Q2 capacitance. When Q2 capacitance is discharged to zero, its body diode starts to conduct and it achieves the zero voltage switching (ZVS) condition.

- **Phase 3**: Freewheeling mode

  Q2 is turned on as the Q2 body diode conducts and achieve ZVS condition. Q2 is turned on to minimize the loss. The primary current is now freewheeling through Q1 and Q2. The transformer secondary voltage is zero, inductor L1 discharges by the output voltage through SR1 and the inductor L2 discharges through SR2.

- **Phase 4**: Switch Q4 ZVS mode

  Q1 is turned off and the primary current charges Q1 capacitance and discharges Q4 capacitances. When Q4 capacitance is discharged to zero, its body diode starts to conduct and it achieves the ZVS condition.

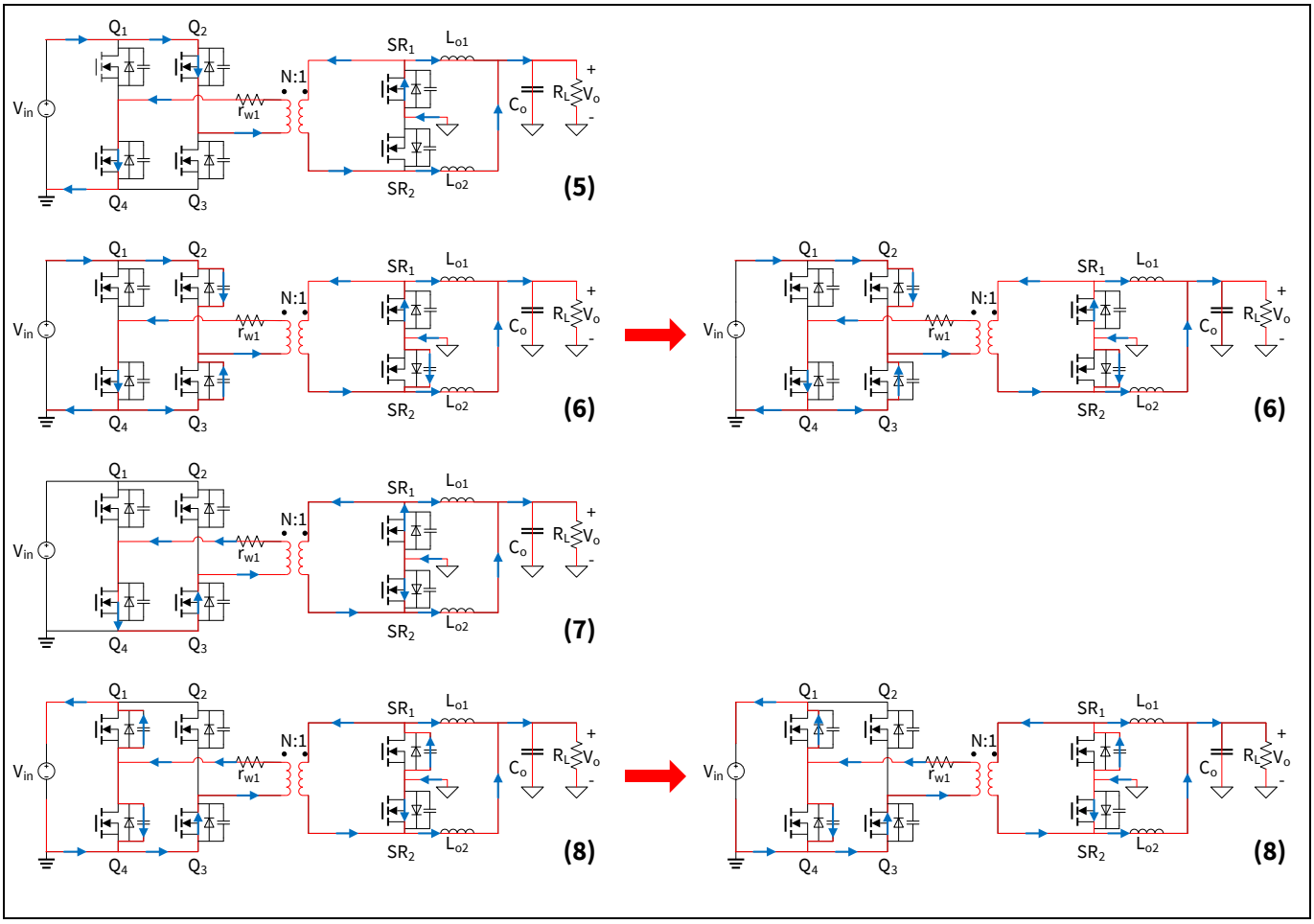

Figure 3 PSFB-CDR operation (Phase 5 to Phase 8)

- **Phase 5**: Power transfer phase

  Q2 and Q4 are turned on and the current is flowing from the primary to the secondary side of the transformer. The transformer secondary voltage V_S is equal to V_{IN} * N_S / N_P. Output inductor L_1 current is discharging and output inductor L_2 is charging.

- **Phase 6**: Switch Q3 ZVS mode

  Q4 stays on but Q2 is turned off. The primary current charges Q2 capacitance and discharges Q3 capacitance. When Q3 capacitance is discharged to zero, its body diode starts to conduct and it achieves the ZVS condition.

- **Phase 7**: Freewheeling mode

  Q3 is turned on as the Q3 body diode conducts and achieve ZVS condition. Q3 is turned on to minimize the loss. The primary current is now freewheeling through Q3 and Q4. The transformer secondary voltage is zero, inductor L1 discharges by the output voltage through SR1 and the inductor L2 discharges through SR2.

- **Phase 8**: Switch Q1 ZVS mode

  Q4 is turned off and the primary current charges Q4 capacitance and discharges Q1 capacitance. When Q1 capacitance is discharged to zero, its body diode starts to conduct and it achieves the ZVS condition.

The complete switching waveforms are shown in the following figure.

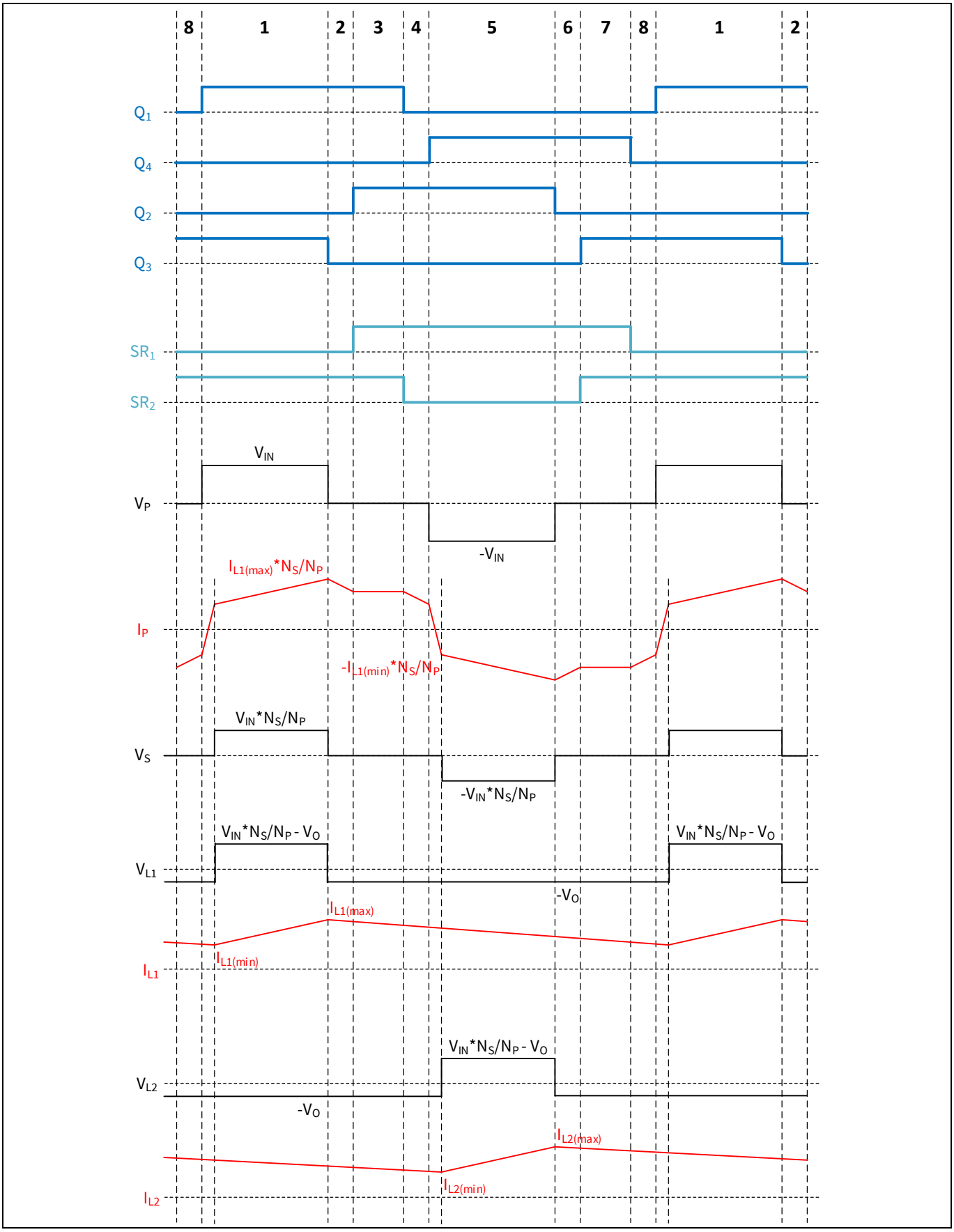

Figure 4 PSFB-CDR switching scheme

1.2 CoolGaN™

Compard to silicon (Si), the breakdown field of Infineon's **CoolGaN™** enhancement mode (e-mode) HEMT is ten times higher, and the electron mobility is double. Both the output charge and gate charge are ten times lower than with Si, and the reverse recovery charge is almost zero, which is key for high-frequency operations.

GaN devices are by nature normally-on devices. The power electronics industry, however, strongly favors normally-off devices. There are two ways to achieve that: the so-called Cascode approach, or by realizing a real monolithic enhancement mode device. Infineon is focusing on the e-mode GaN concept for its CoolGaN™ 400 V and 600 V devices, suitable for all consumer and industrial applications, with the most robust and best-performing concept in the market.

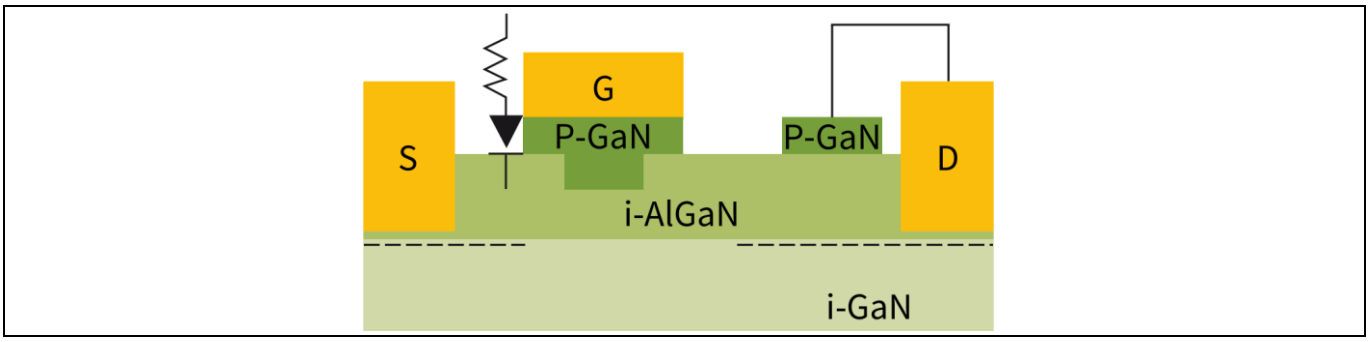

Figure 5 Hybrid drain-GIT, normally-off GaN

REF_XDP_1000W_GAN_PSFB uses IGT60R070D1, which offers several benefits:

- Excellent for hard- and soft-switching topologies
- Optimized turn-on and turn-off
- $R_{DS(on)}$ shift immunity
- Excellent V_{th} stability
- Best FOM
- Longer lifetime proven

1.3 OptiMOS™ 5

Power supply designers face the challenge of improving system efficiency and power density while at the same time reducing system costs. Infineon's **OptiMOS™ 5** product families feature up to 50 percent lower $R_{DS(on)}$ and 31 percent improvement of FOM compared to alternative devices.

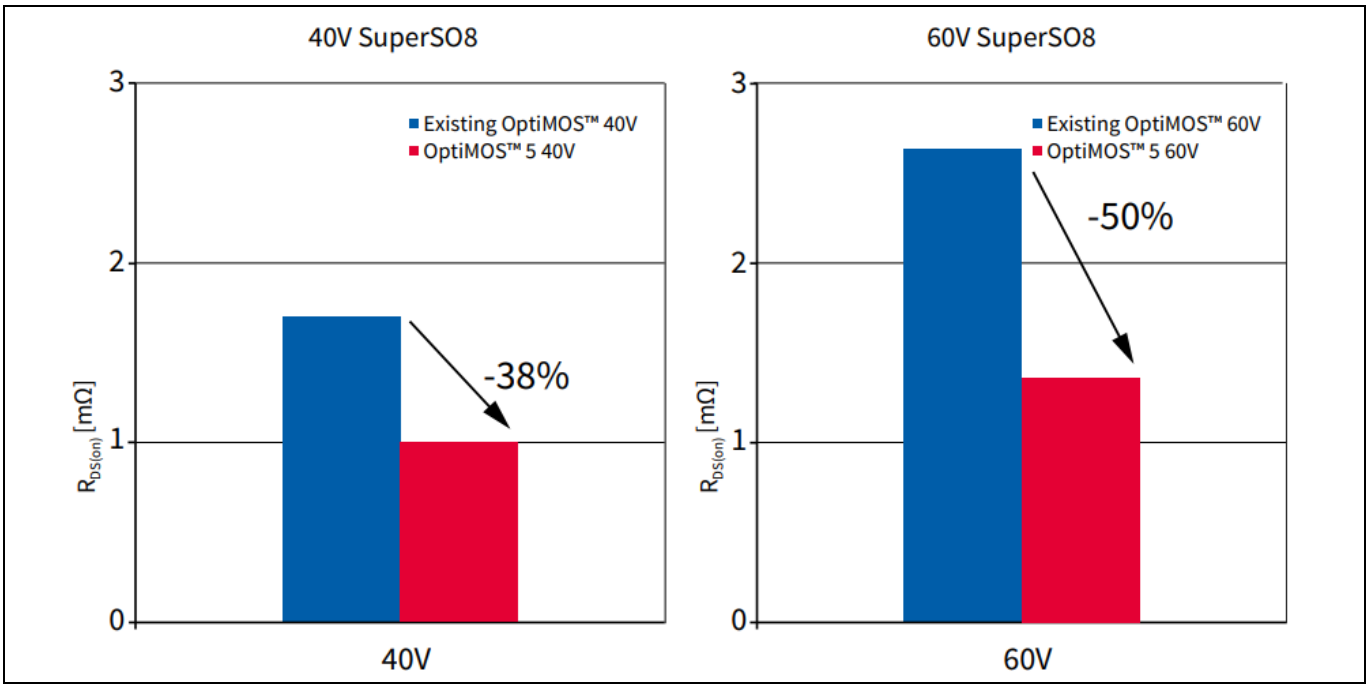

Figure 6 OptiMOS™ 5 $R_{DS(on)}$ comparison

REF_XDP_1000W_GAN_PSFB uses **BSC028N06NS** for the synchronous rectification (SR) MOSFETs. It is rated at 60 V, maximum current at 132 A and $R_{DS(on),max}$ at 2.8 mΩ. It uses the latest SuperSO8 – 5x6 mm^2 to enable high power density implementation as well as enhanced temperature capability. It offers several benefits:

- Highest system efficiency – optimized for SR operation
- 15 percent lower $R_{DS(on)}$ than alternative devices – less paralleling is required
- 31 percent lower FOM ($R_{DS(on)}$ x Q_g) over similar devices – increased power density
- Integrated Schottky-like diode
- Qualified according to JEDEC (J-STD20 and JESD22) for target applications
- Pb-free lead plating, RoHS compliant

1.4 XDPP1100 digital controller

REF_XDP_1000W_GAN_PSFB uses the **XDPP1100** digital controller. XDPP1100 is a highly integrated and programmable digital power supply controller which offers an advanced power control solution for a wide variety of DC-DC power applications in isolated and non-isolated topologies.

A combination of high-performance analog front end (AFE), state machine-based digital control loop and an ARM® Cortex™-M0 integrated in a single chip makes the XDPP1100 a highly integrated, fully programmable and fastest time-to-market technology for modern high-end power systems.

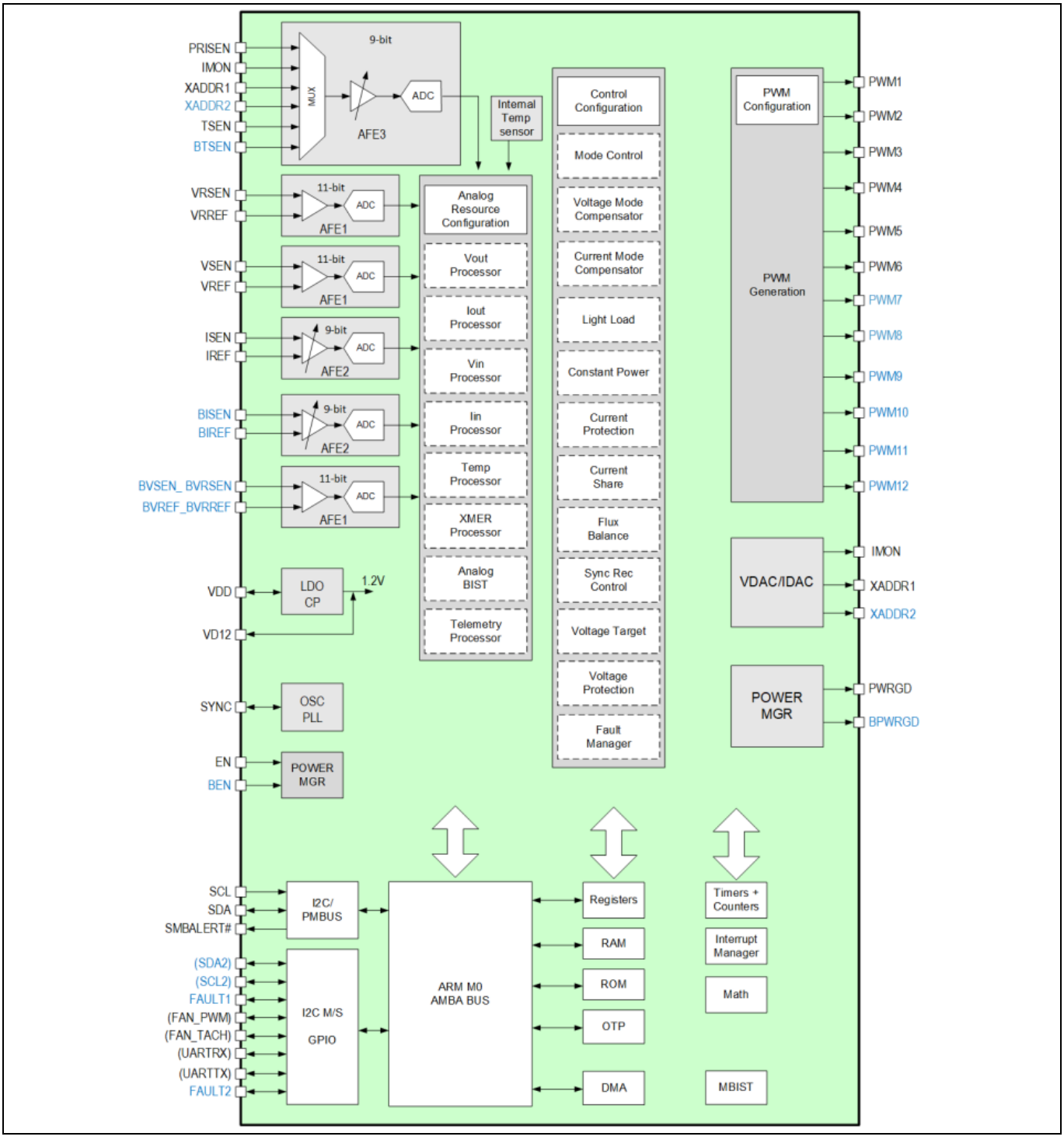

Figure 7 XDPP1100 block diagram

Introduction

XDPP1100 offers several key benefits:

- Pre-programmed peripherals and configurability for faster time-to-market
- Enhanced control and excellent dynamic transient performace
- Integrated V/I sensing capability for best-in-class system performance, significantly reduced BOM size, and low system cost
- Sophisticated system-level fault handling
- System housekeeping, e.g., fan control, LED control, sequencing, P_{GOOD} with configurable GPIOs
- Firmware-based system configuration with GUI support for ease of use and product differentiation

The full control loop diagam of XDPP1100 is shown in the following figure.

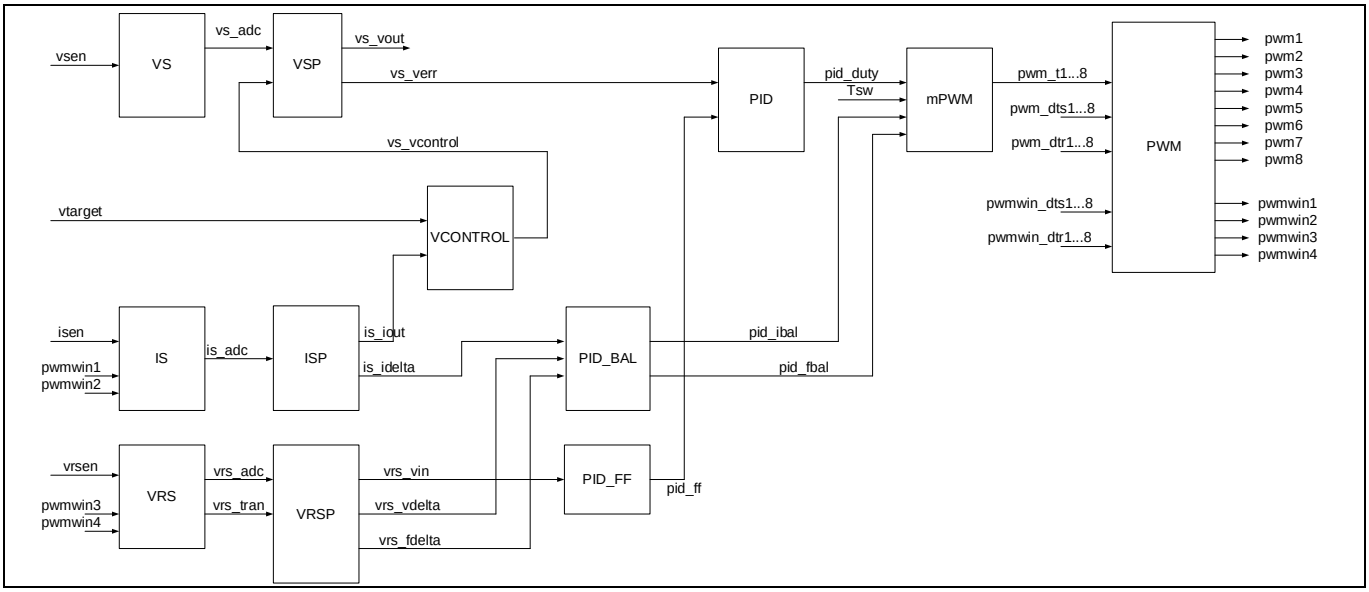

Figure 8 XDPP1100 control loop block diagram

XDPP1100 enables superior output voltage regulation under light load condition, deadtime optimization for higher efficiency, and sophisticated diagnostics and fault management features. This is possible due to the implemented hardware-based PID controller module (**PID**) and best-in-class hardware-based FF (**PID_FF**) filter block. A dedicated flux-balancing (**PID_BAL**) module is available to correct the PWM duty cycle when working with full-bridge topology.

The voltage sense ADC (**VS**) is an 11-bit ADC with 50 MHz sampling rate. The ADC resolution is 1.25 mV and enhanced with 3-bit digital modulation for output voltage regulation. This gives 156 µV resolution at the sense pin and 1.58 mV resolution at the 12 V output with a scale of 0.099. The hardware resolution limits the highest resolution the board can achieve. Hence, setting PMBus command VOUT_MODE to -10 (resolution 0.976 mV), -11 (resolution 0.488 mV) or -12 (resolution 0.244 mV) will give the same result. This design configures VOUT_MODE = -12.

A separate voltage ADC (**VRS**) is also designed to sense a high-frequency switching signal and makes it perfectly suited to sensing the input voltage from the transformer secondary-side at the switching node V_{rect}. This eliminates the use of an isolated op-amp or other types of isolator for input voltage sensing. The input voltage is computed based on the resistor-divider ratio and transformer turns ratio. The information is used for V_{IN} telemetry, protection and FF compensation. When the voltage ADC is configured as V_{rect} sense mode, it senses both the amplitude of the voltage and the duration of the pulse. This feature is used for the volt-second flux-balancing control.

Introduction

The current sense (CS) ADC (**IS**) is a 9-bit ADC with 25 MHz sampling rate. Exceptional noise immunity is achieved by the use of the internal current estimator. Based on the state of the PWM pulse, the controller continuously predicts DC and ripple current. The result of the prediction is combined with the actual measured current to be processed by the controller. Hence, the instantaneous noise in the measurement can be filtered out without losing the valuable ripple current information.

It can also sense input voltage through the telemetry ADC input (PRISEN pin) before switching starts up. In this design, the input voltage information is taken from the bias power supply. The gain and offset of the PRISEN voltage sense can be configured by two registers for accurate V_{IN} telemetry. The telemetry ADC is a 9-bit ADC with a sample frequency of 1 MHz. The telemetry ADC block consists of eight channels and can be configured to digitize voltages, currents, impedance and temperature.

The XDPP1100 has two temperature sense channels. In this design, ATSEN senses PCB shunt resistor temperature and is used for CS temperature compensation. BTSEN senses SR MOSFET temperature and is used for overtemperature protection.

In addition, PMBus and I^2C communication is integrated to facilitate system configuration and control as well as telemetry updating and fault monitoring.

2 System description

The REF_XDP_1000W_GAN_PSFB is a high-voltage DC-DC converter reference design implemented using Infineon's latest digital power controller XDPP1100. It is based on PSFB-CDR topology and is rated at 1000 W, making it an ideal reference for high-power DC-DC applications such as telecom and data center infrastructure.

The REF_XDP_1000W_GAN_PSFB is designed to output 12 V DC and is operating at nominal input voltage of 380 V DC, but ranges from 360 V DC to 420 V DC. The power stage is controlled by Infineon's latest digital power controller, XDPP1100.

XDPP1100 offers pre-programmed firmware for the PSFB topology to kick-start a similar project. In addition, it is also possible to modify the pre-programmed firmware and/or create new features in order to achieve end-product differentiation.

Apart from XDPP1100, the power converter described in this document uses IGT60R070D1 GaN FETs to enable high-frequency switching. This GaN FETs support up to 600 V DC input voltage and are switched at 350 kHz.

The block diagram of the PSFB-CDR implementation is shown in the following figure.

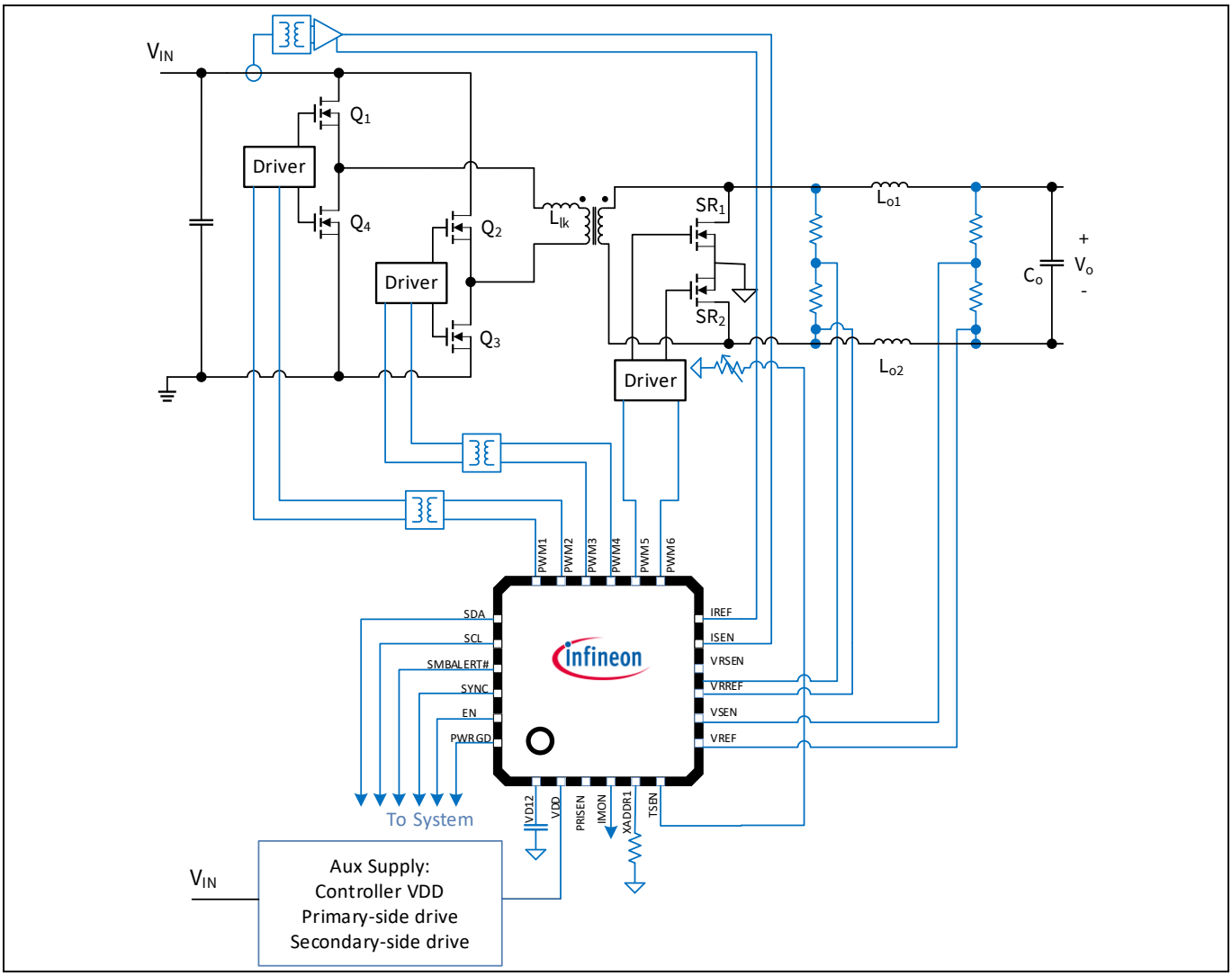

Figure 9 System block diagram

The complete board assembly is shown in the following figure.

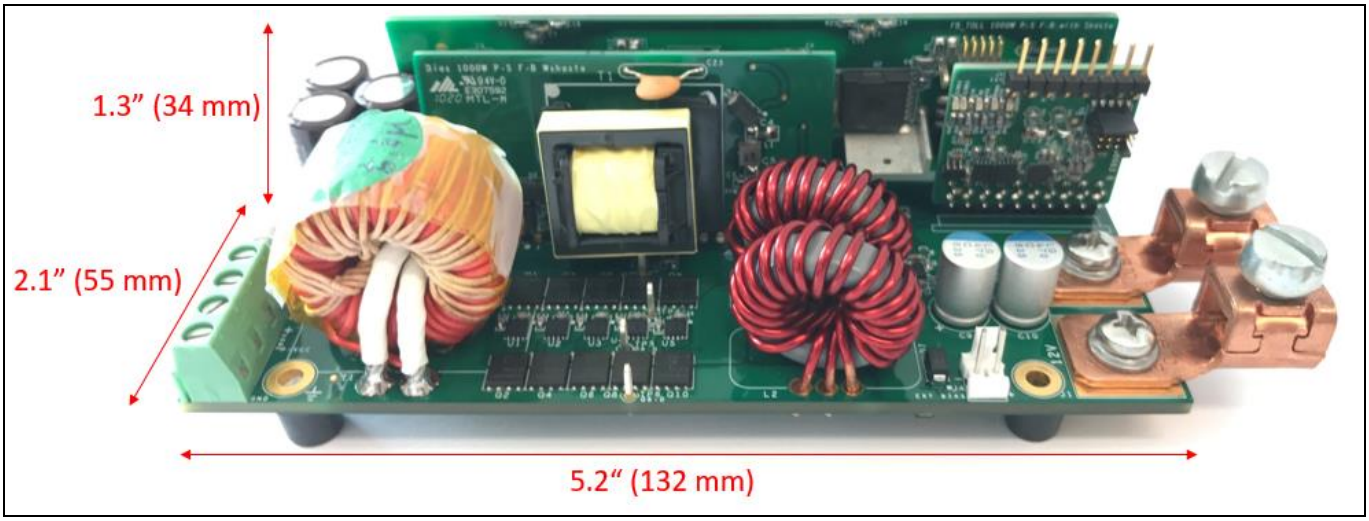

Figure 10 Fully assembled 1000 W PSFB-CDR board

2.1 Specification

The board specification is listed in the following table.

Table 1 Power board specification

Parameter	Symbol	Min.	Typ.	Max.	Unit
Output voltage	V_{OUT}	11.7	12.0	12.2	V
Output current	I_{OUT}			84	A
V_{OUT} overvoltage protection	$V_{OUT,OVP}$		14		V
V_{OUT} undervoltage protection	$V_{OUT,UVP}$		8		V
Input voltage	V_{IN}	360	380	400	V
V_{IN} overvoltage protection	$V_{IN,OVP}$		420		V
V_{IN} undervoltage protection	$V_{IN,UVP}$		350		V
Input current	I_{IN}		2.63	2.8	A
Rated power	P_{OUT}		1000	1024	W
Switching frequency	f_{SW}		350		kHz
Efficiency at 380 V, half load	η		95.36		%
Isolation voltage	V_{ISO}		1500		V
PSFB transformer turns ratio	N_P/N_S		11.0		

2.2 Power stage

The power stage of REF_XDP_1000W_GAN_PSFB comprises two boards: “main board” and “full-bridge board”.

Main board provides the base for other boards to mount. It contains ten OptiMOS™ 5 60 V 2.8 mΩ **BSC028N06NS**s as SR MOSFETs, and gate drivers EiceDRIVER™ **2EDN7524G**s that enable fast dual-channel 5 A driving optimized for driving both MOSFET and GaN power switching devices.

Full-bridge board consists of the full-bridge circuitry which makes use of four CoolGaN™ 600 V 70 mΩ enhancement-mode power transistor **IGT60R070D1**s as well as the dual-channel reinforced isolated gate driver EiceDRIVER™ **2EDS8265H** that allows 4 A/8 A source/sink dual-channel gate driver 150 V/ns common-mode transient immunity. In addition, the full-bridge power stage is also equipped with silicon carbide (SiC) freewheeling diode CoolSiC™ **IDD09SG60C** to enable ZVS operation.

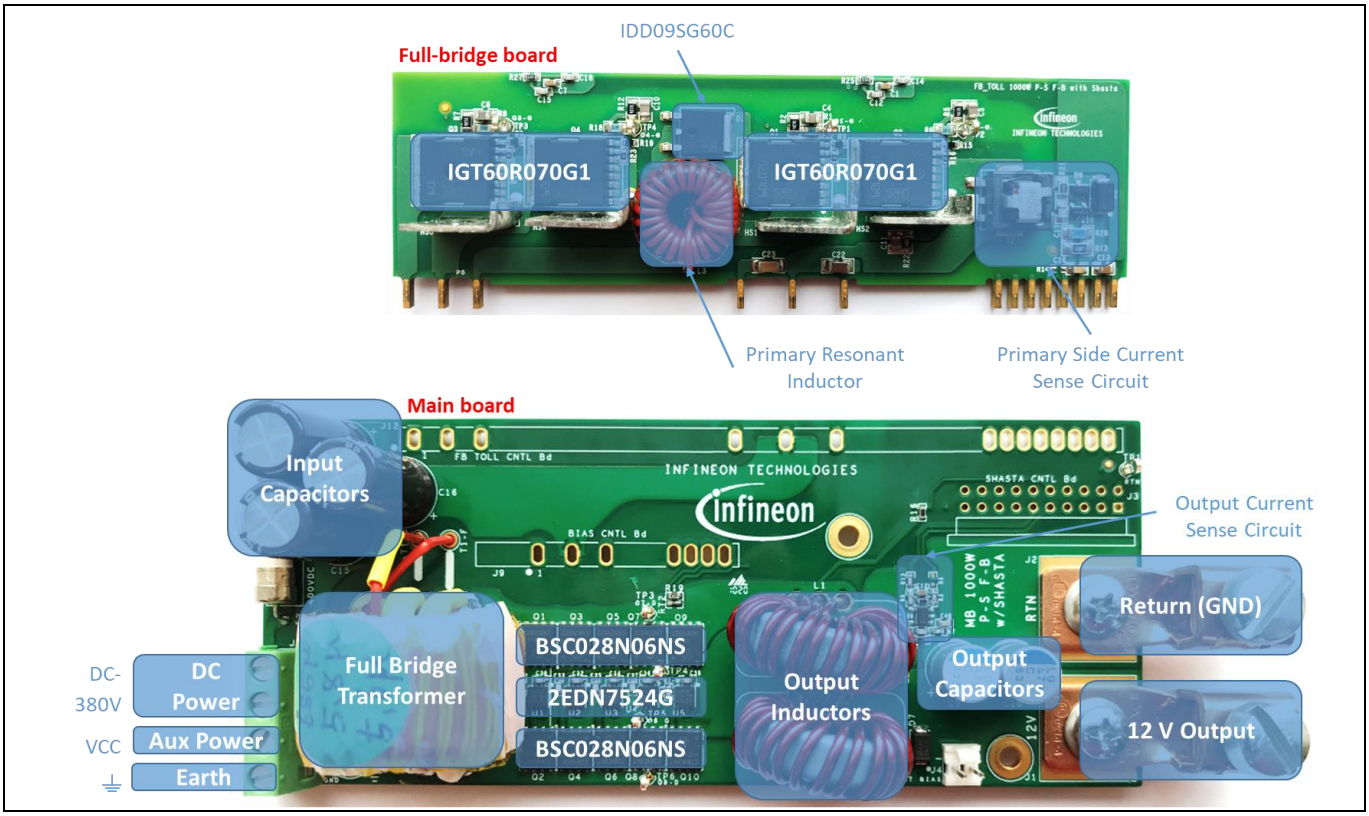

Figure 11 Power stage

2.3 Auxiliary bias board

Auxiliary power supply is required for supplying regulated voltage to the gate drivers, signal-conditioning circuitry and the digital controller. It uses a flyback converter with dual output to provide galvanic isolation between the primary side and the secondary side of the PSFB-CDR board.

The flyback converter is controlled with Infineon's latest fifth-generation fixed-frequency CoolSET™ **ICE5GR2280AG** that offers high performance and integration of the latest generation of 800 V CoolMOS™ P7 superjunction MOSFETs in a DSO-12 package. It is switched at 125 kHz and it can deliver power of up to 22 W with integrated protections. The transformer used in this design is supplied by Wurth Electronics, with a part number of 750344550.

The flyback converter is regulated on the secondary side because the critical circuitries that require tight supply regulation, such as the CS op-amp and the digital controller, are placed on the secondary side. The feedback signals are returned to the controller via the opto-isolator.

The voltage supply to the digital controller is further regulated with Infineon's linear voltage regulator **IFX1117ME V33**.

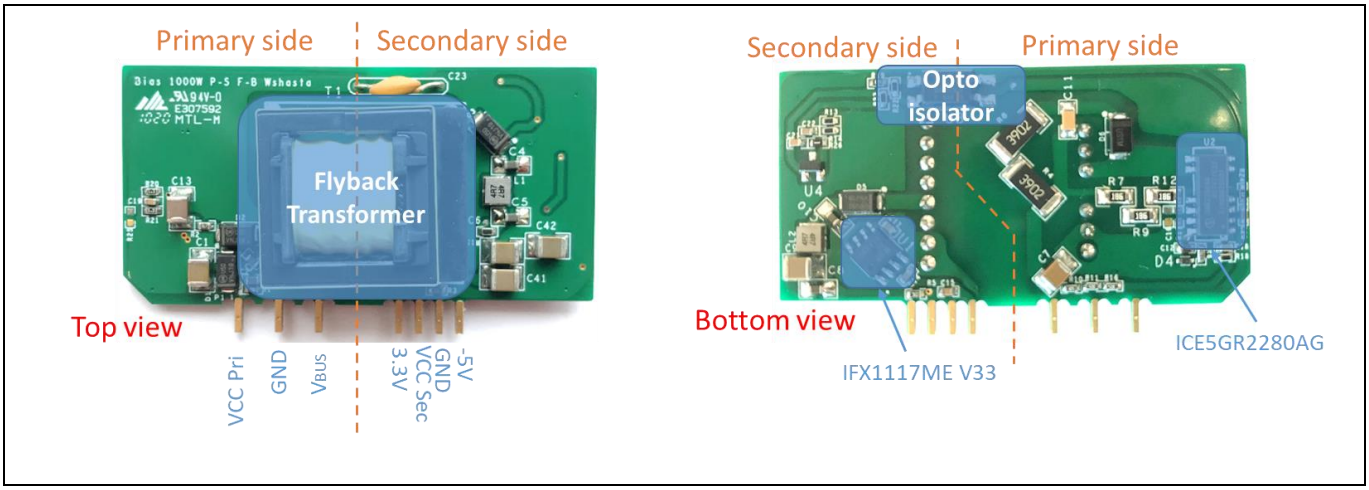

Figure 12 Auxiliary bias board

The auxiliary bias board specification is shown in the following table.

Table 2 Auxiliary bias board specification

Parameter	Symbol	Min.	Typ.	Max.	Unit
Secondary-side output voltage 1	V_{SEC1}	–	12.0	–	V
Secondary-side output voltage 2	V_{SEC2}	–	-5.0	–	V
Primary-side output voltage	V_{PRI}	–	12.0	–	V
Input voltage range	$V_{IN,range}$	350.0	380.0	410.0	V
Switching frequency	f_{SW}	–	125	–	kHz

2.4 Control board

This board contains the **XDPP1100** digital controller that implements the PSFB-CDR topology and its control algorithms. XDPP1100 supports PSFB-CDR topology natively.

The control board is shown in the following figure.

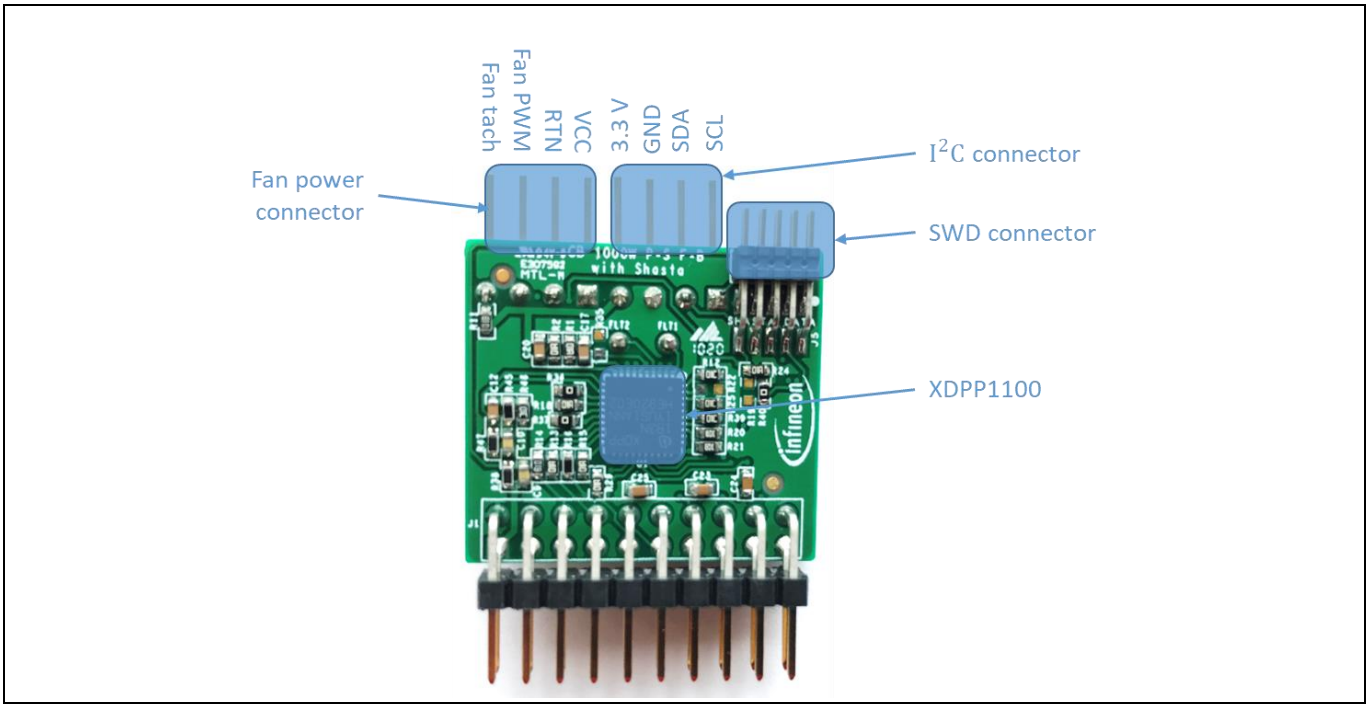

Figure 13 Control board

This board provides three connectors:

- ***I²C connector***. This connector is used for PMBus communication. It consists of standard I²C signals, namely SDA, SCL, GND and 3.3 V. The user performs operations on XDPP1100 on their computer via a PMBus dongle connection.
- ***SWD connector***. This connector is used for advanced firmware debugging via the Lauterbach TRACE32 debugger.
- ***Fan power connector***. This connector is used when external fans are connected. It supports fans with voltages of up to 12 V. The fan speed is controlled via the Fan PWM pin and the fan speed measurement is done via the Fan Tach pin. Fan settings are configurable from PMBus.

3 Configuration

There are two ways to configure XDPP1100:

- ***PMBus setting configuration***. PMBus is a communication protocol that is built on top of another communication protocol called I^2C and is designed specifically for power management applications. It has become the standardized communication protocol for digital power applications. XDPP1100 complies with with PMBus Power System Management Protocol Specification, revision 1.3.1.
- ***Direct register configuration***. Altough PMBus provides convenience and a standardized way to configure power management applications, direct register configuration is also provided in XDPP1100 for advanced users who seek to further optimize the digital control performance.

Both of these configurations can be stored as a file called “Board Design File” for later use on XDPP1100.

Some configurations are highlighted in this section to illustrate the XDPP1100 configuration process.

3.1 PMBus setting configuration

The following table highlights some of the PMBus configurations for the PSFB board. These configurations are easily found in any other PMBus-compliant systems.

Table 3 PMBus configuration

CMD	Name	Value	Description
0x00	PAGE	0	PMBus Page 0. There are two pages in XDPP1100: Loop 0 and Loop 1. This configuration is using Loop 0 and therefore page is set to 0.
0x01	OPERATION	On	Set to “on” to turn-on the system immediately
0x02	ON_OFF_CONFIG	0x1F	Respond to operation and EN pin, EN polarity active high
V_{OUT} configuration			
0x20	VOUT_MODE	-12	Linear format exponent for V_{OUT}
0x21	VOUT_COMMAND	12.000 V	Output voltage command/reference
0x29	VOUT_SCALE_LOOP	0.0986328125	Output voltage sensing resistor-divider ratio
Switching frequency and duty-cycle configuration			
0x32	MAX_DUTY	85 percent	Maximum duty cycle
0x33	FREQUENCY_SWITCH	350 kHz	Switching frequency
Output OVP configuration			
0x40	VOUT_OV_FAULT_LIMIT	14.0000 V	Fault threshold for output overvoltage
0x42	VOUT_OV_WARN_LIMIT	13.0000 V	Warning threshold for output overvoltage
Output UVP configuration			
0x43	VOUT_UV_WARN_LIMIT	9.000 V	Warning threshold for output undervoltage
0x44	VOUT_UV_FAULT_LIMIT	8.000 V	Fault threshold for output undervoltage
Output OCP configuration			
0x46	IOUT_OC_FAULT_LIMIT	85.0 A	Fault threshold for output overcurrent
0x4A	IOUT_OC_WARN_LIMIT	83.0 A	Warning threshold for output overcurrent
Input OVP configuration			

Configuration

CMD	Name	Value	Description
0x55	VIN_OV_FAULT_LIMIT	440.0 V	Fault threshold for input overvoltage
0x57	VIN_OV_WARN_LIMIT	420.0 V	Warning threshold for input overvoltage
Input UVP configuration			
0x58	VIN_UV_WARN_LIMIT	360.0 V	Warning threshold for input undervoltage
0x59	VIN_UV_FAULT_LIMIT	350.0 V	Fault threshold for input undervoltage
Input OCP configuration			
0x5B	IIN_OC_FAULT_LIMIT	3.50 A	Fault threshold for input overcurrent
0x5D	IIN_OC_WARN_LIMIT	2.0 A	Warning threshold for input overcurrent
Output OPP configuration			
0x6A	POUT_OP_WARN_LIMIT	1010.0 W	Warning threshold for output overpower
Input OPP configuration			
0x6B	PIN_OP_WARN_LIMIT	1300.0 W	Warning threshold for input overpower
Transformer and sensing configuration			
0xCD	MFR_VRECT_SCALE	0.33	Secondary-side rectified voltage sensing divider resistor
0xCE	MFR_TRANSFORMER_SCALE	0.091	Transformer scaling (N_{sec}/N_{pri})

3.1.1 Deadtime configuration with 0xCF PWM_DEADTIME

Deadtime selection is important to optimize the efficiency of the system. In XDPP1100, the deadtime is set by adding a delay to the rising edge or falling edge of each PWM output. Deadtime configuration is accessible via PMBus command 0xCF PWM_DEADTIME. The deadtime of PWM rise and fall times can be configured separately. In most situations, only deadtimes at the rising edge need to be set. The maximum deadtime that can be set is 318.75 ns with resolution of 1.25 ns. When setting the deadtimes, please consider the isolator delay that will be added to the primary PWMs, making the real gate waveform shift to the right.

The following figure shows deadtime configuration.

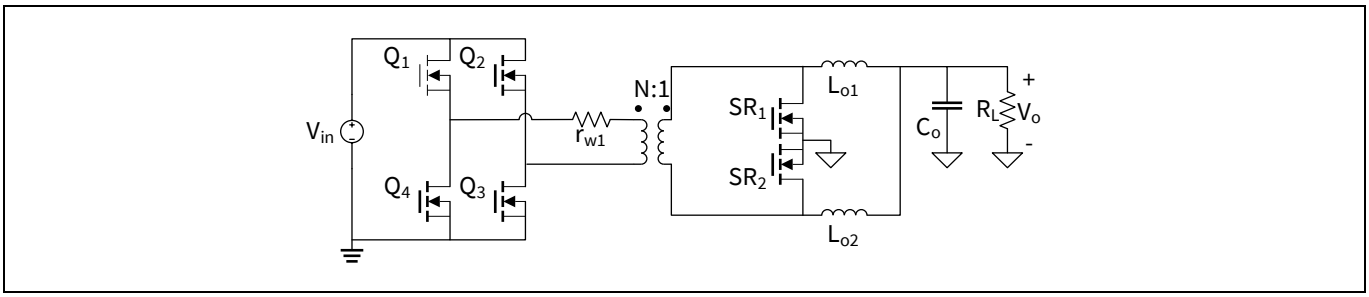

Figure 14 Topology selection and turns ratio

The PSFB-CDR switches and XDPP1100 pin mapping are shown in the following figure.

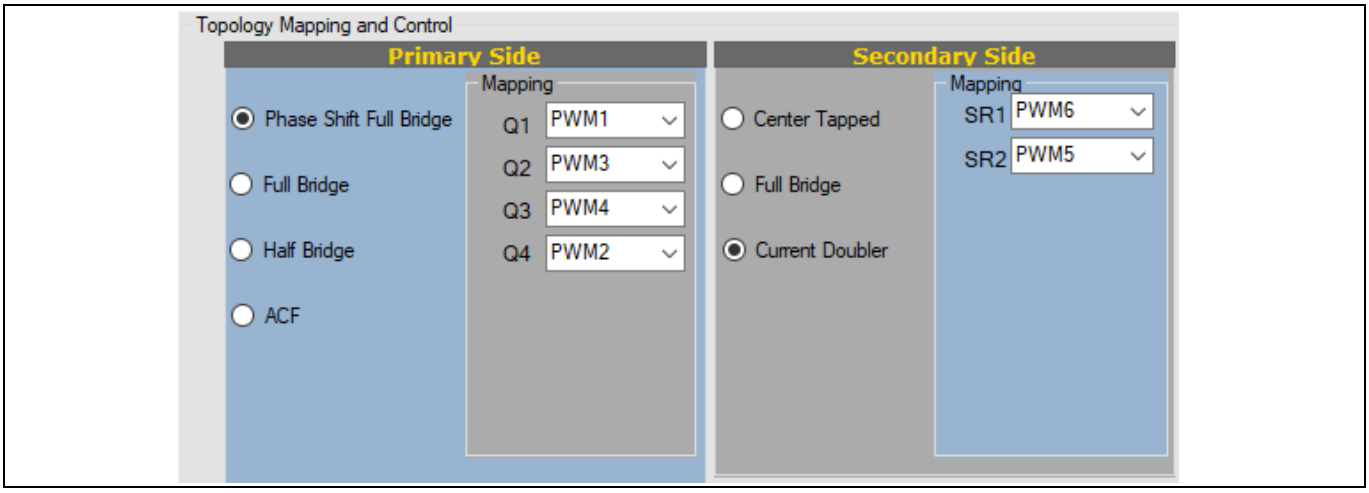

Figure 15 Topology pin mapping and control

Configuration

The deadtime timing diagram is shown in the following figure.

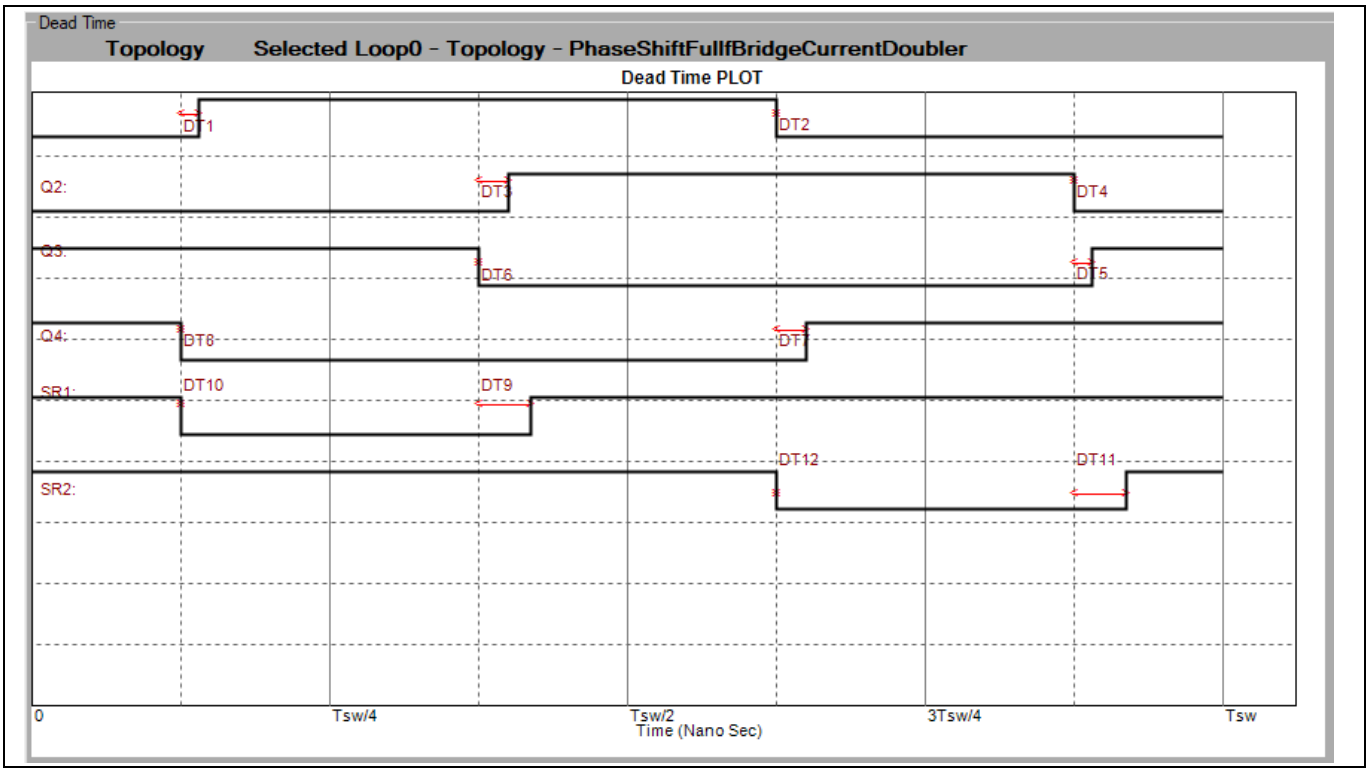

Figure 16 Deadtime configuration

The following table shows the deadtime configuration of REF_XDP_1000W_GAN_PSFB.

Table 4 Deadtime configuration

PSFB switch	XDPP1100 pin	Edge	Label	Value
Q1	PWM1	Rising	DT1	50 ns
		Falling	DT2	0 ns
Q2	PWM3	Rising	DT3	80 ns
		Falling	DT4	0 ns
Q3	PWM4	Rising	DT5	50 ns
		Falling	DT6	0 ns
Q4	PWM2	Rising	DT7	80 ns
		Falling	DT8	0 ns
SR1	PWM6	Rising	DT9	140 ns
		Falling	DT10	0 ns
SR2	PWM5	Rising	DT11	140 ns
		Falling	DT12	0 ns
Isolation delay				100 ns

3.2 Register configuration

XDPP1100 implements two hardware control blocks, namely *PID filter* and *feed-forward filter*, as the control modules:

- PID filter is used to compensate output voltage against sudden load change (load transient).
- Feed-forward filter is used to compensate output voltage against sudden input voltage change (input transient).

The values coming out of both PID filter and feed-forward filter blocks are then added together to make up the output duty cycle that controls the PSFB-CDR. It is also important to clamp the total output of both filters to prevent overflow.

In XDPP1100 implementation, both the PID filter and feed-forward filter reside in a module called *PID block*, as illustrated in the following figure. For more information on other blocks in XDPP1100, refer to [2].

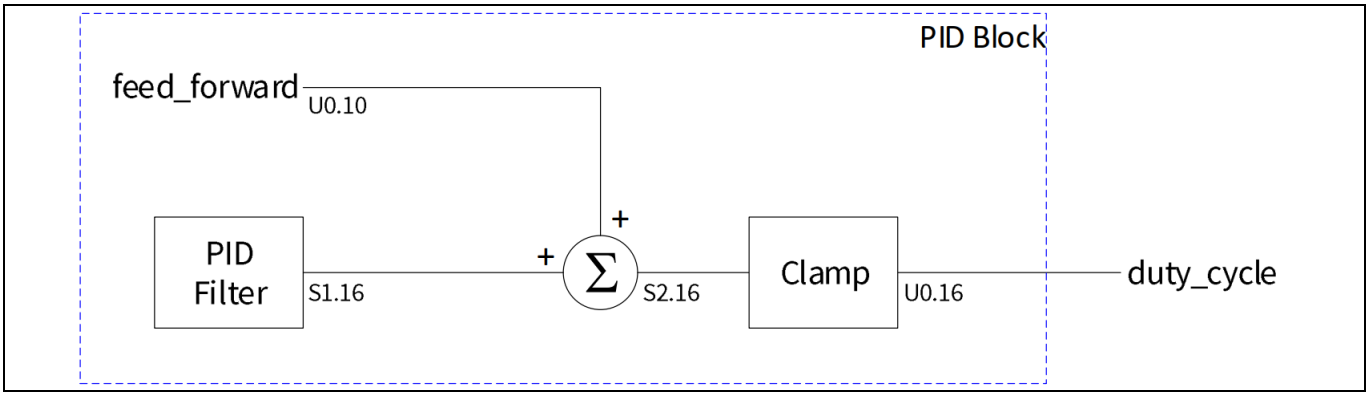

Figure 17 Diagram of PID block

It is noteworthy to mention that the output of PID filter is formatted as S1.16, and the output of feed-forward filter is formatted as U0.10, while the output duty cycle is formatted as U0.16. For more information on number format in XDPP1100, refer to [3].

3.2.1 PID filter register configuration

As is the case with the standard PID filter, the configuration of proportional, integral and derivative coefficients K_P, K_I and K_D are done directly via register, as shown in the following table.

Table 5 PID filter direct register configuration

Register name	Value	Description
pid0_kp_index_1ph	32	PID proportional coefficient index
pid0_ki_index_1ph	28	PID integral coefficient index
pid0_kd_index_1ph	77	PID derivative coefficient index

3.2.2 Feed-forward filter register configuration

Feed-forward filter reads and inverts the input voltage (FF = $1/V_{IN}$) to produce an inverse relationship between input voltage and duty cycle:

- When V_{IN} decreases, feed-forward filter output increases and therefore, duty cycle will increase
- When V_{IN} increases, feed-forward filter output decreases and therefore, duty cycle will decrease

In XDPP1100, the feed-forward filter implementation is shown in the following figure.

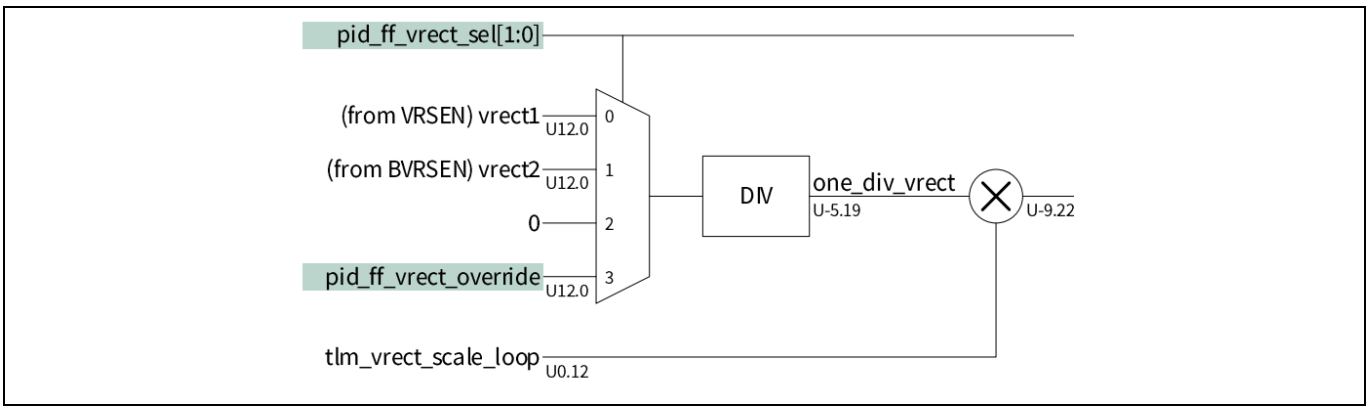

Figure 18 Feed-forward filter in XDPP1100

The two registers highlighted in green are configurable, and are described in the following table.

Table 6 Feed-forward filter register configuration

Register name	Value	Description
pid0_ff_vrect_sel	0	FF V_{rect} source select
pid0_ff_vrect_override	0	FF override value

Since pid0_ff_vrect_sel is set to 0, the multiplexer branch 0 "**(from VRSEN) vrect1**" will be used for FF calculation. VRSEN is the ADC module used for sensing the PSFB transformer's secondary-side voltage, known as rectified sensing. For more information on other modules, refer to [1]. By sensing the transformer's secondary-side voltage and assuming transformer turns ratio is known, the input voltage (V_{IN}) on the primary side can be derived.

The value of vrect1 is then passed through a DIV block, producing **one_div_vrect**. This is the raw feed-forward filter output that will be combined with the PID filter output later on.

Since XDPP1100 uses voltage divider resistors to read the PSFB transformer's secondary-side voltage (VRSEN), **tlm_vrect_scale_loop** register must be updated to cater for the voltage divider ratio.

4 Measurement setup

4.1 Efficiency measurement setup

The efficiency measurement and evaluation is illustrated in the following block diagram.

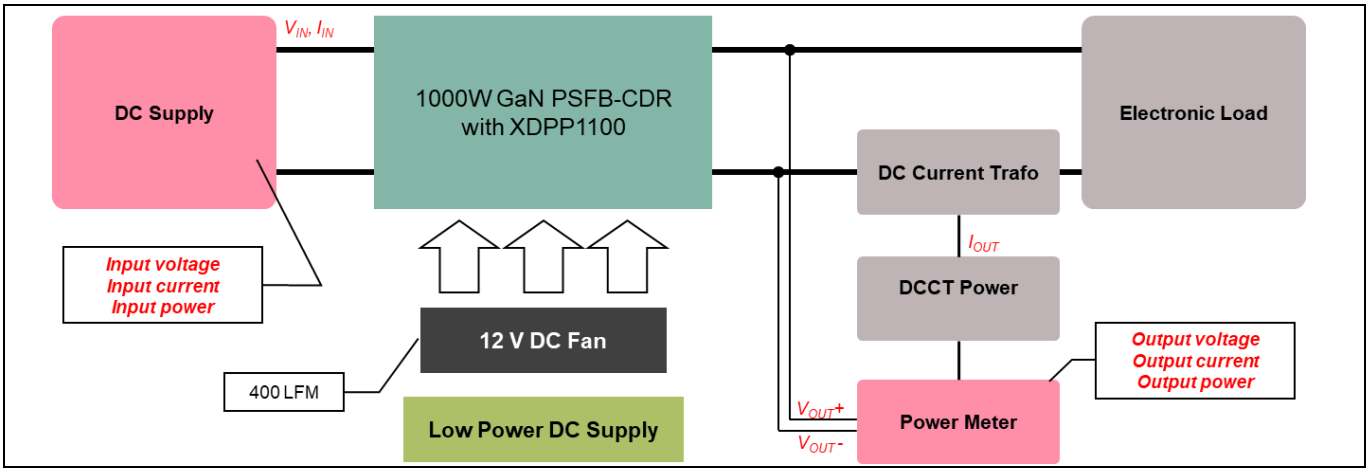

Figure 19 Efficiency measurement setup

4.2 Necessary equipment

The necessary equipment for measurement setup is shown below.

Table 7 Necessary equipment

Equipment type	Description
DC supply	High-voltage DC supply capable of 400 V and rated at least 1200 W
Electronic load	Programmable electronic load that supports CC/CV mode rated at least 1200 W
DC current transformer	Non-invasive I_{OUT} measurement
DC CT power	Power supply for DC current transformer
Power meter	V_{OUT} measurement. Works together with DC current measurement to calculate P_{OUT}
Low-power DC supply	Provide aux. supply if needed. Provide 12 V supply to the cooling fan
Cooling fan	Cool down switching heat. Recommended to use fan that supports ~400 LFM

5 Performance

This section showcases system performance and some waveforms to highlight system behavior.

5.1 Efficiency graph

REF_XDP_1000W_GAN_PSFB efficiency curves at different input voltages are shown below. The efficiency was measured at room temperature of 25°C, with the board cooled using a fan with 400 LFM. There is no external power supply required.

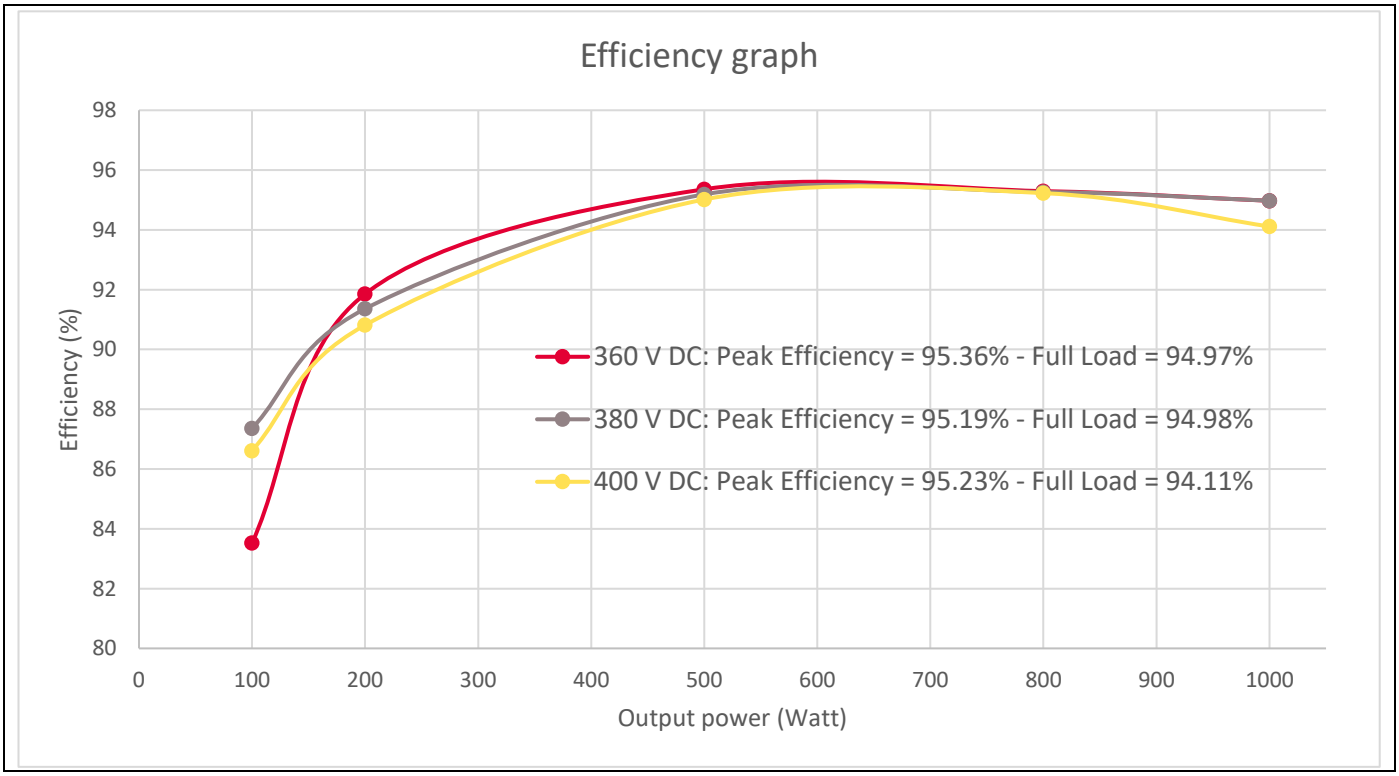

Figure 20 Efficiency graph

Efficiency data are summarised in the following table.

Table 8 Summary of efficiency measurement (in percent)

Load	Efficiency (V_{IN} = 360 V DC)	Efficiency (V_{IN} = 380 V DC)	Efficiency (V_{IN} = 400 V DC)
10%	83.52	87.36	86.61
20%	91.85	91.36	90.81
50%	95.36	95.19	95.02
80%	95.29	95.27	95.23
100%	94.97	94.98	94.11

5.2 Waveforms

This section showcases the selected waveforms across different operations.

5.2.1 Steady-state

The waveforms showcasing PSFB modulation signals when operating in steady-state are shown in this section.

The probing points are illustrated in the following figure.

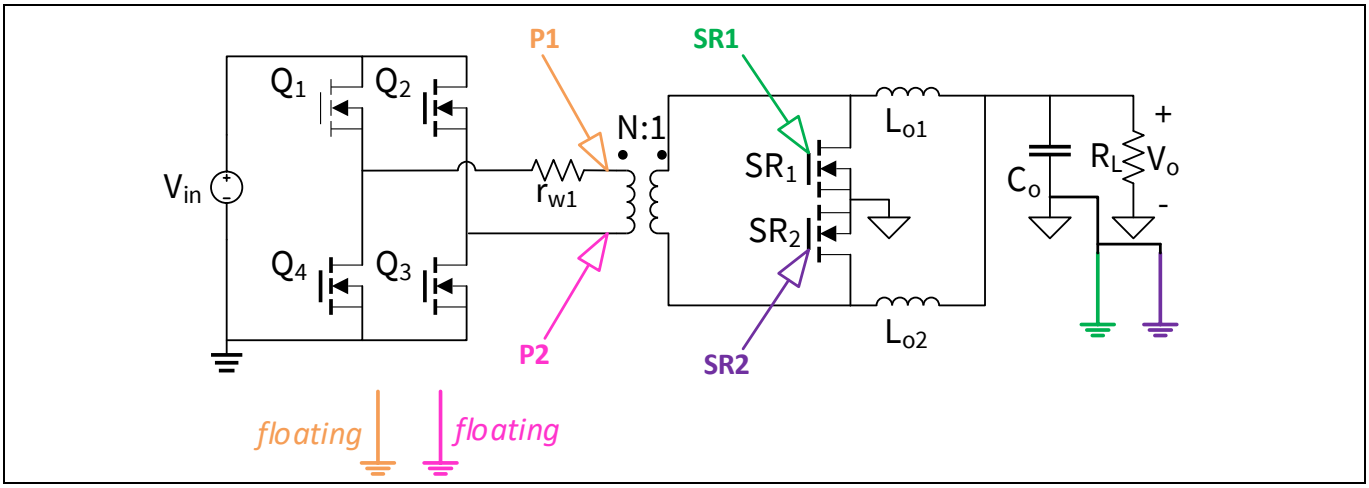

Figure 21 Probing points for steady-state waveforms

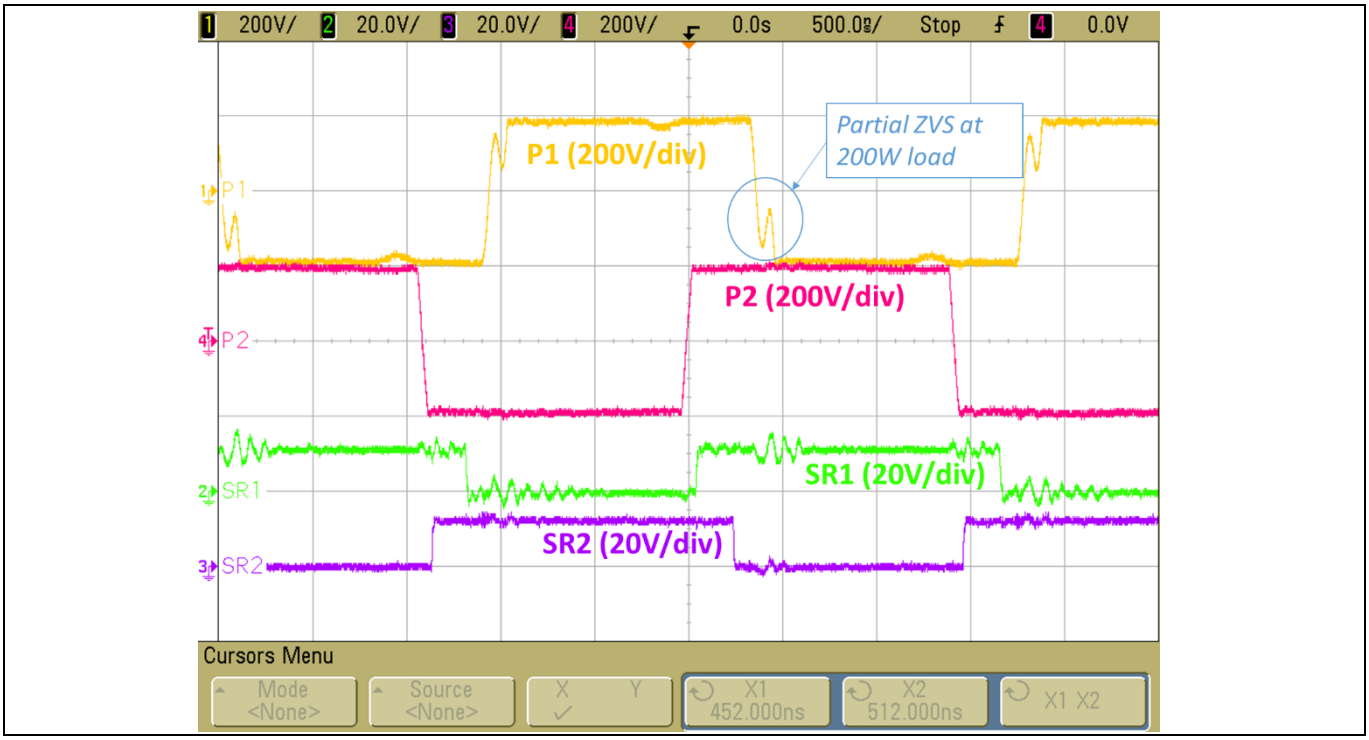

Figure 22 Steady-state waveforms at load = 200 W, V_{IN} = 380 V DC

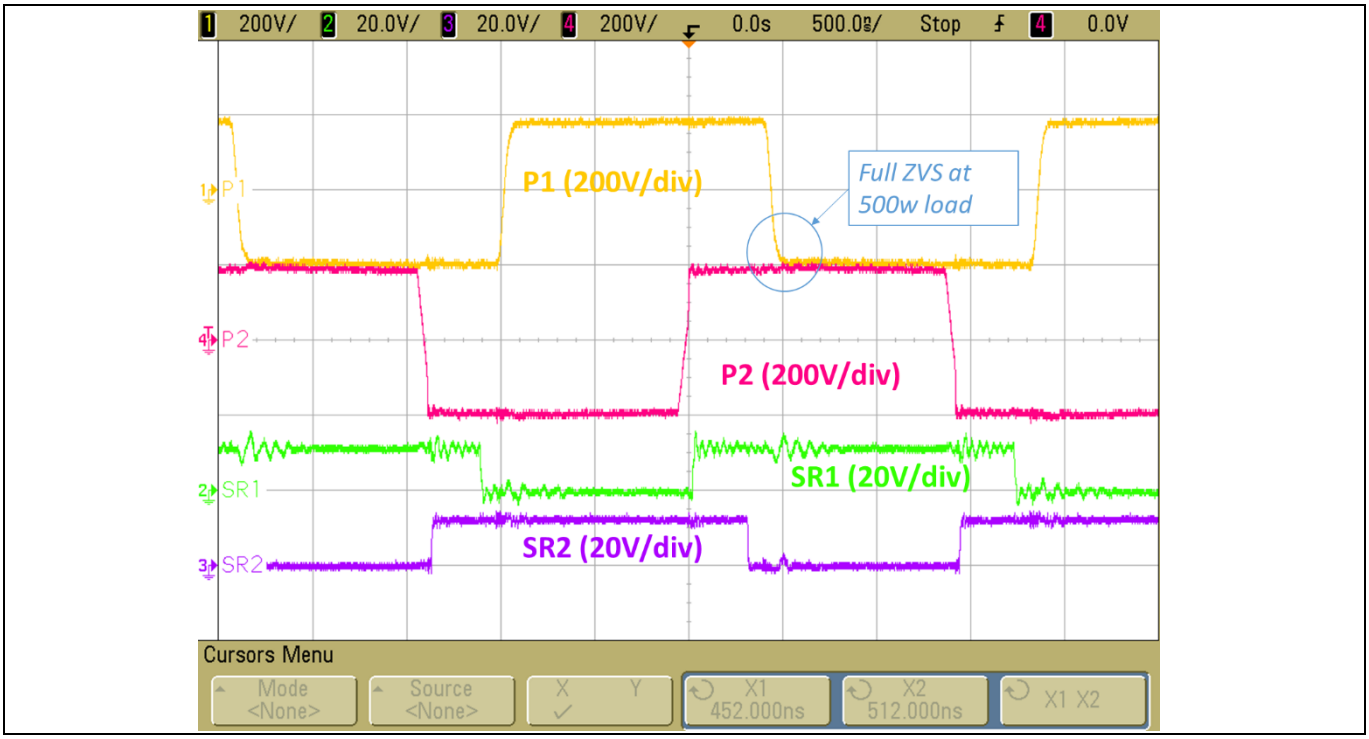

Figure 23 Steady-state waveforms at load = 500 W, V_{IN} = 380 V DC

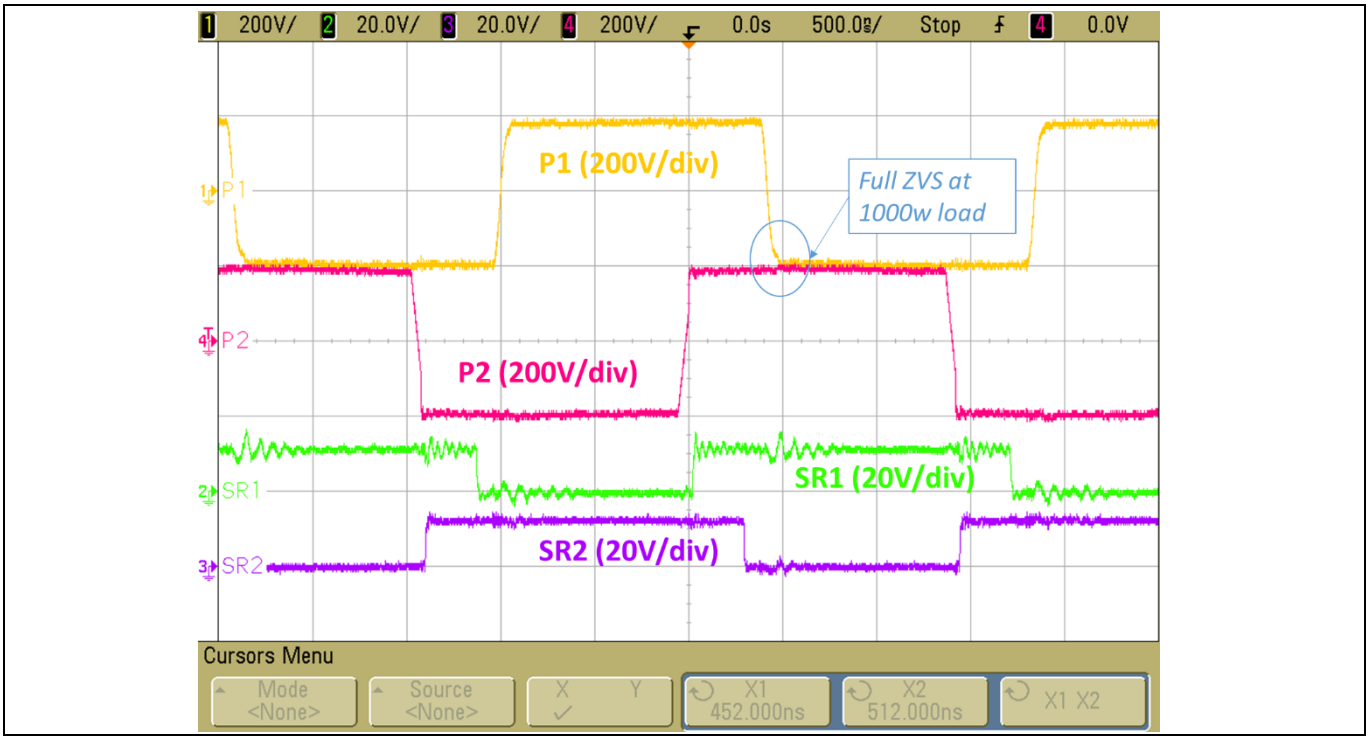

Figure 24 Steady-state waveforms at load = 1000 W, V_{IN} = 380 V DC

5.2.2 Load regulation

The waveforms showcasing PSFB load-transient are shown below. There is minimal impact on the output voltage transient on either large load step-up or large load step-down.

The probing points are illustrated in the following figure.

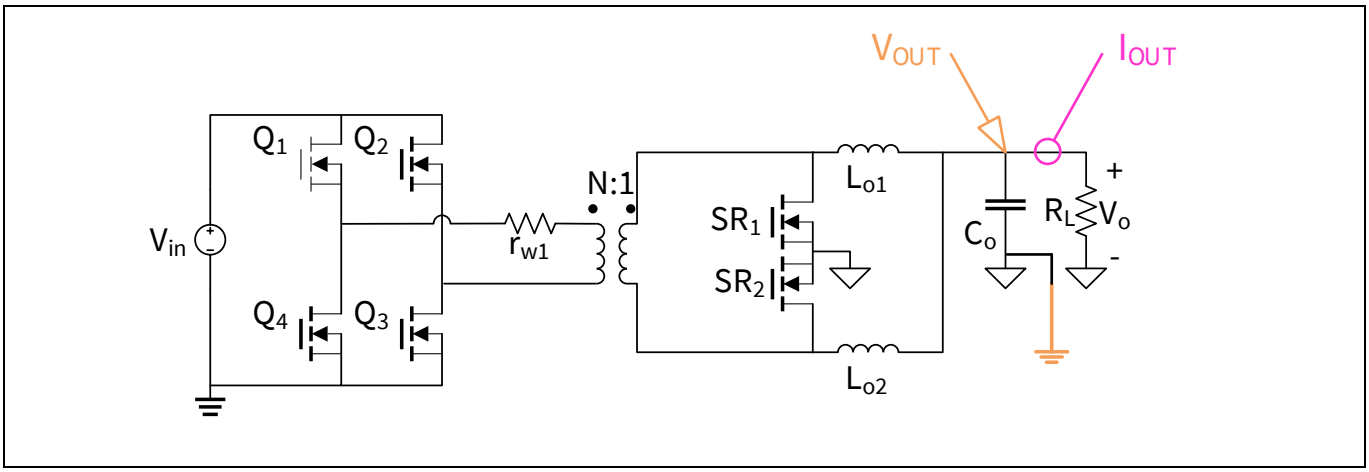

Figure 25 Probing points for load regulation

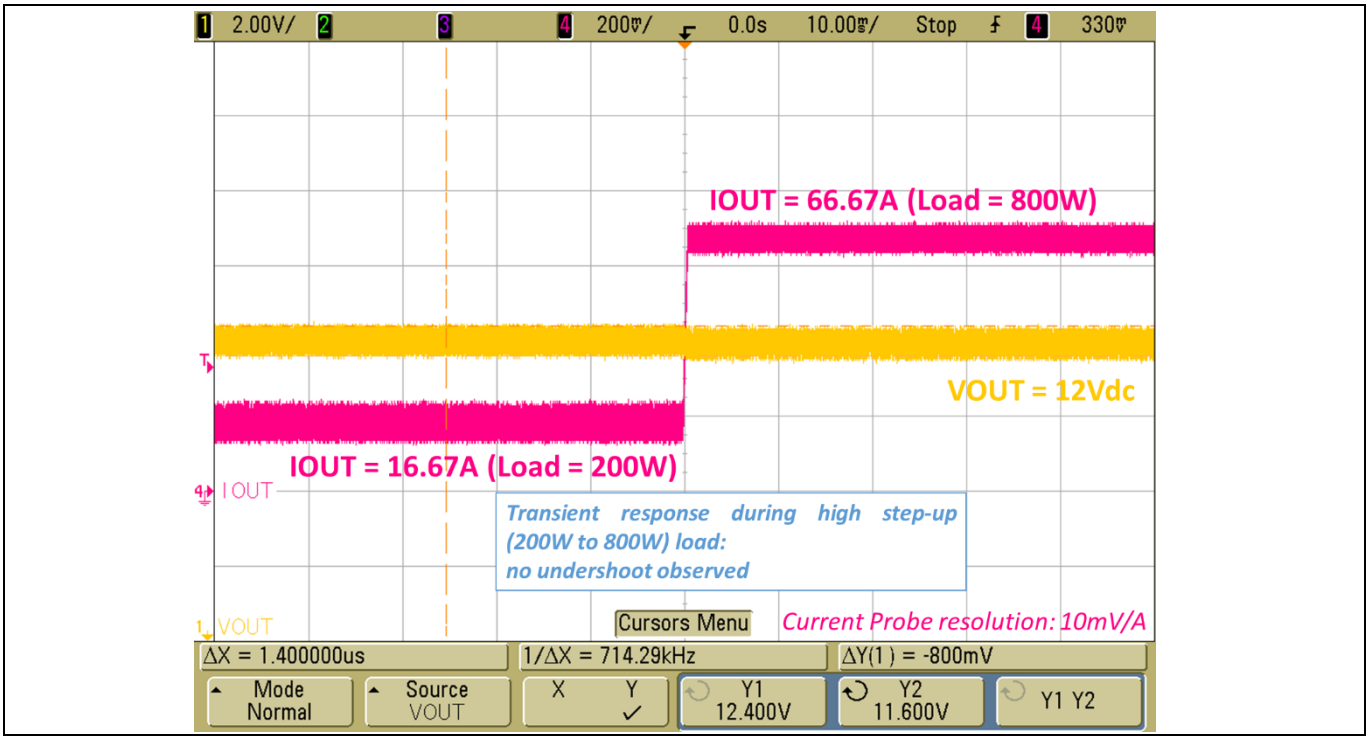

Figure 26 Load-transient waveforms between 200 W and 800 W, V_{IN} = 380 V DC

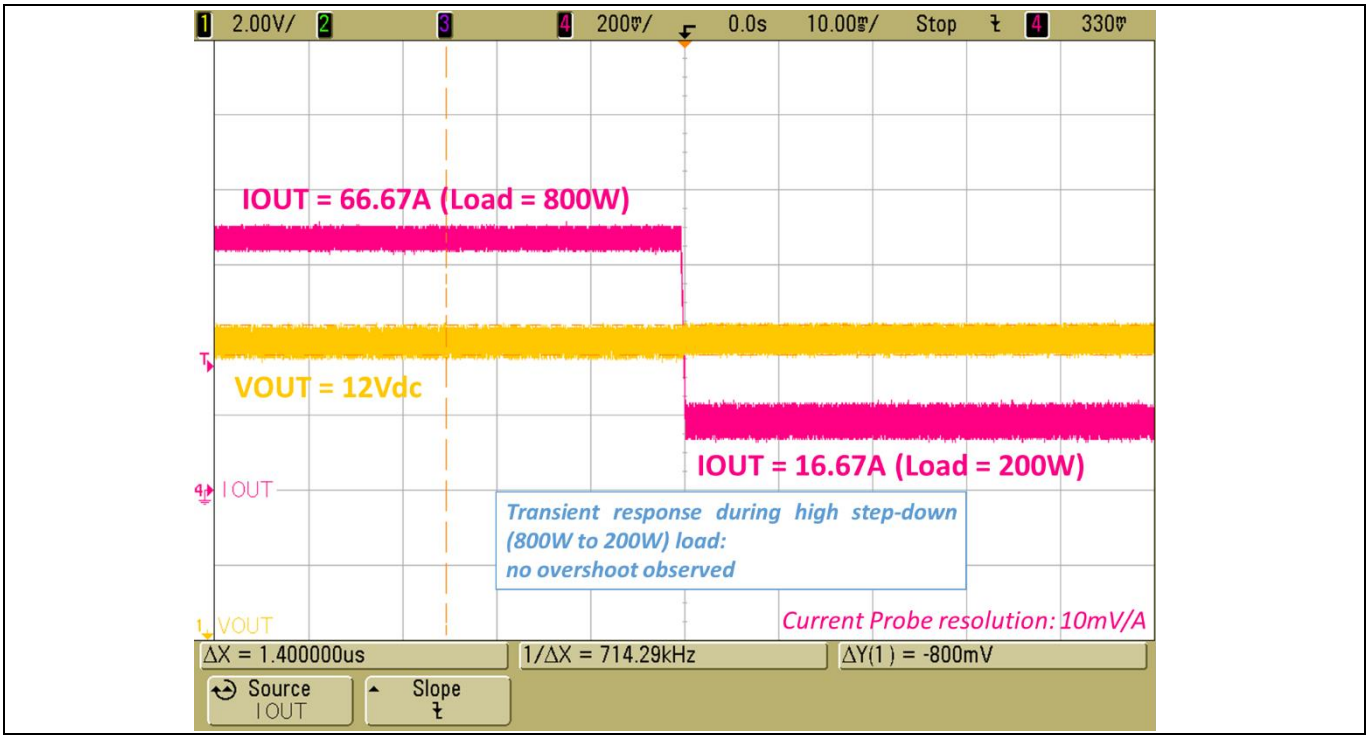

Figure 27 Load-transient waveforms between 800 W and 200 W, V_{IN} = 380 V DC

5.2.3 Input voltage transient

The waveforms showcasing PSFB input voltage transient are shown below. There is minimal impact on the output voltage transient on either input voltage step-up or step-down.

The probing points are illustrated in the following figure.

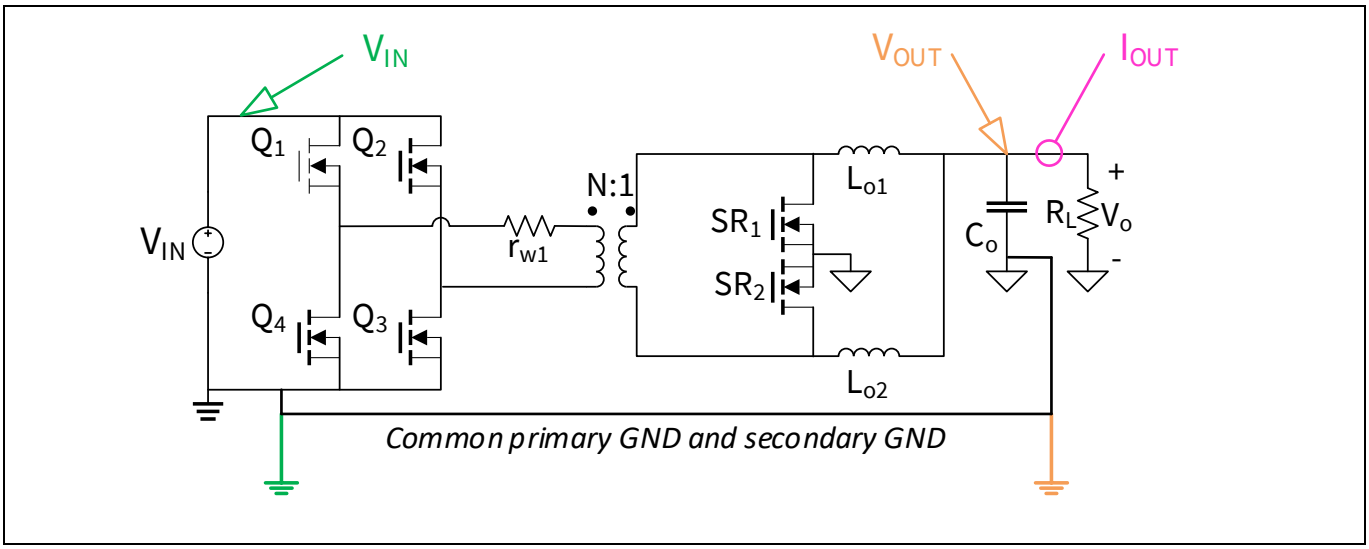

Figure 28 Probing points for input voltage transient

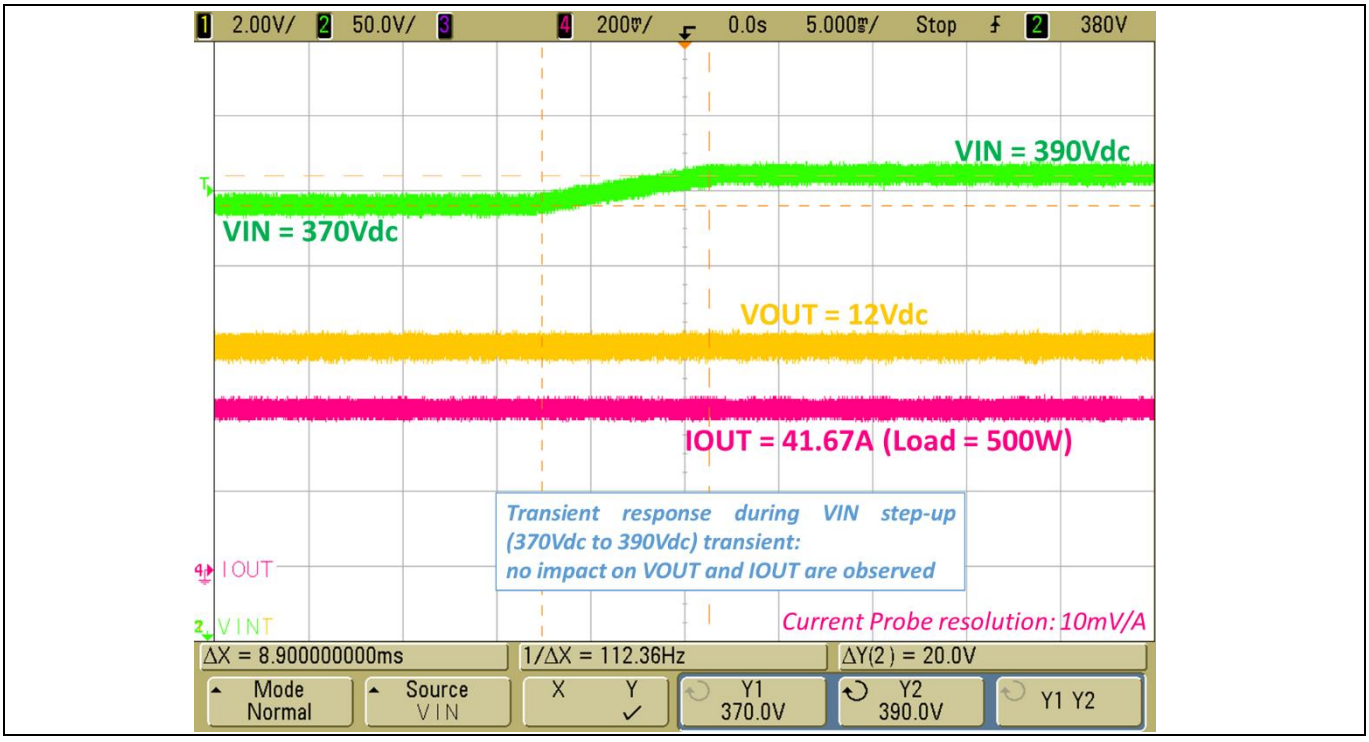

Figure 29 Input voltage transient waveforms between 370 V DC and 390 V DC, load = 500 W

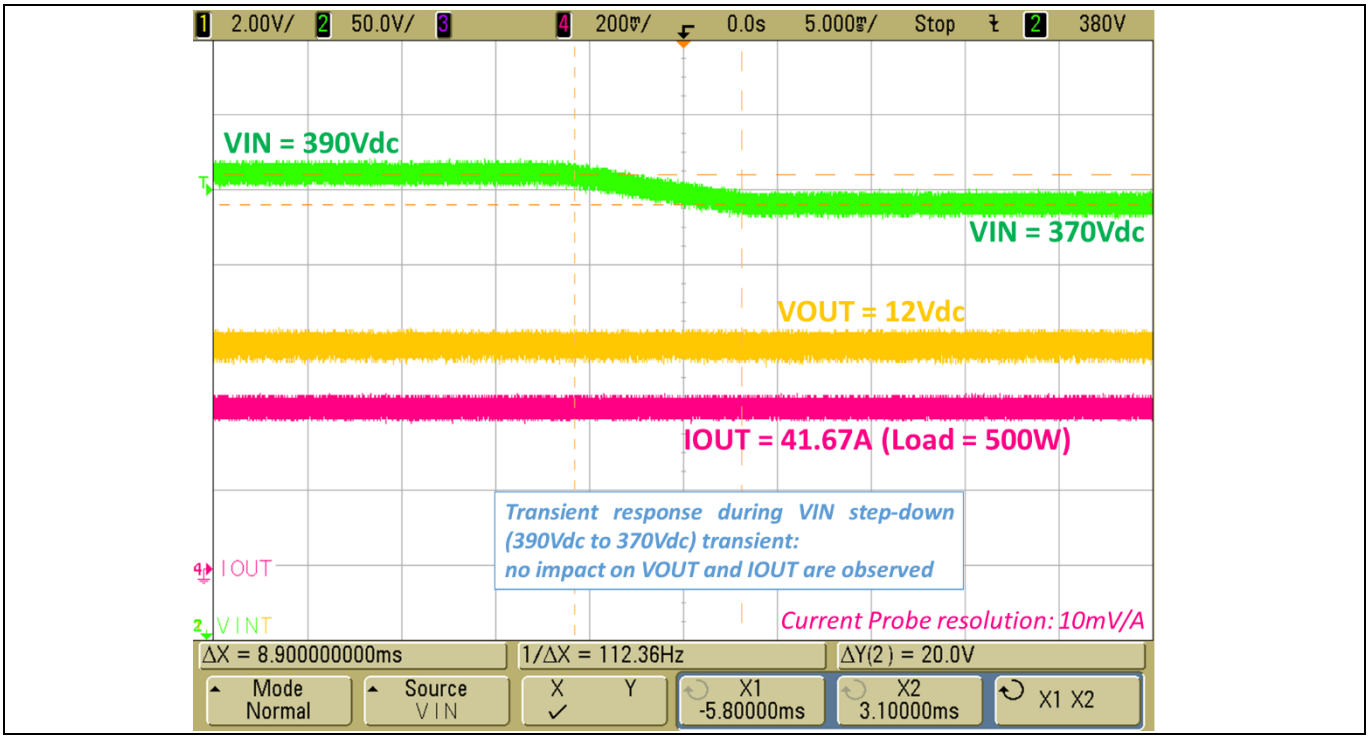

Figure 30 Input voltage transient waveforms between 390 V DC and 370 V DC, load = 500 W

5.2.4 Start-up regulation

A soft-start function minimizes large inrush current to the load during start-up by gradually increasing the switching current limit during the start-up process, therefore slowing down the output voltage rise time.

The probing points are illustrated in the following figure.

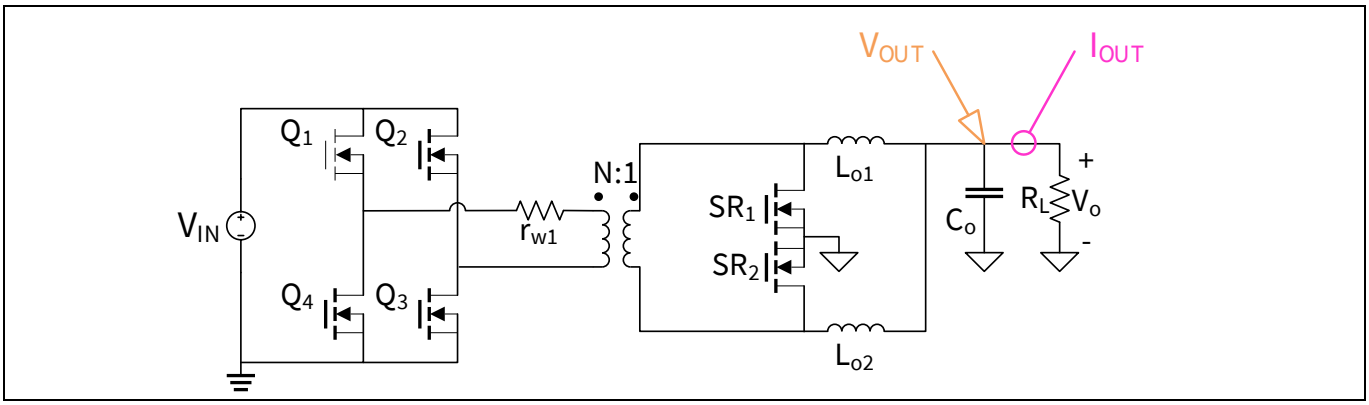

Figure 31 Probing points for start-up regulation

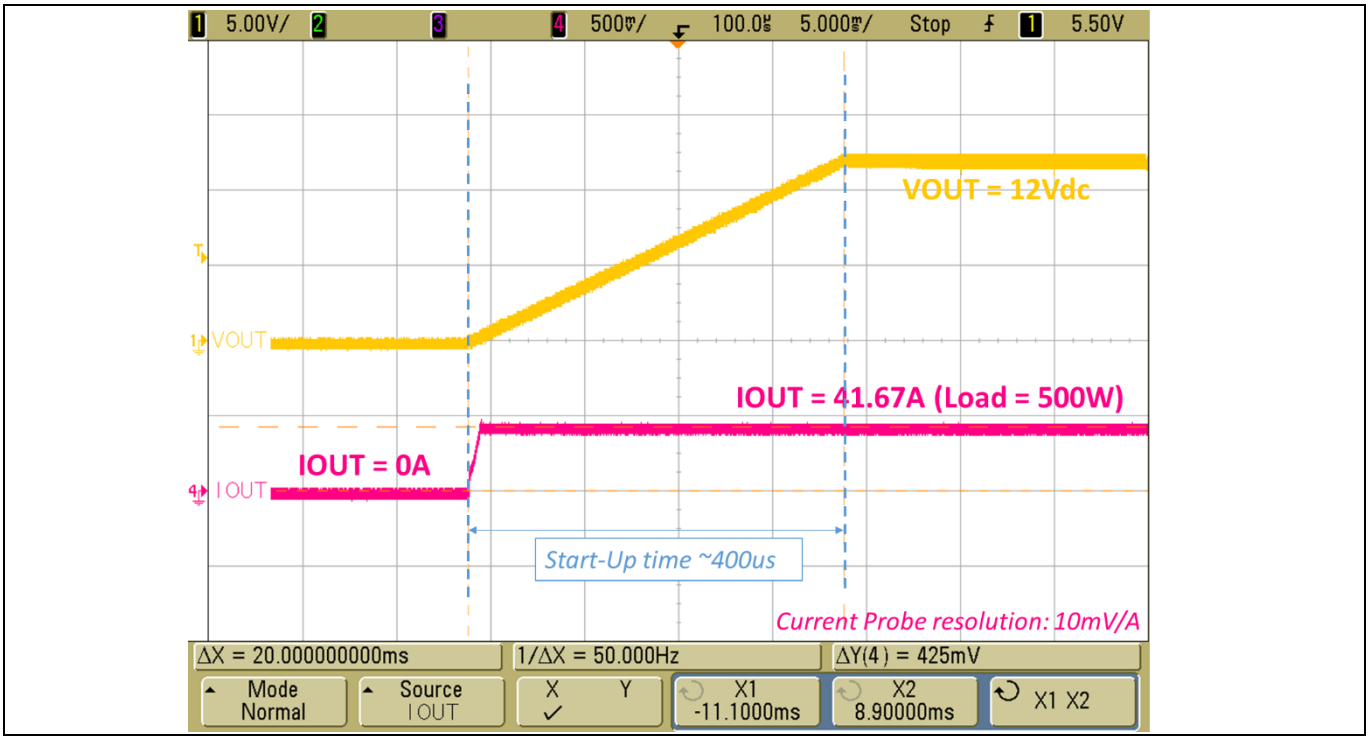

Figure 32 Start-up waveforms at 500 W

The following waveforms show shutdown at 500 W.

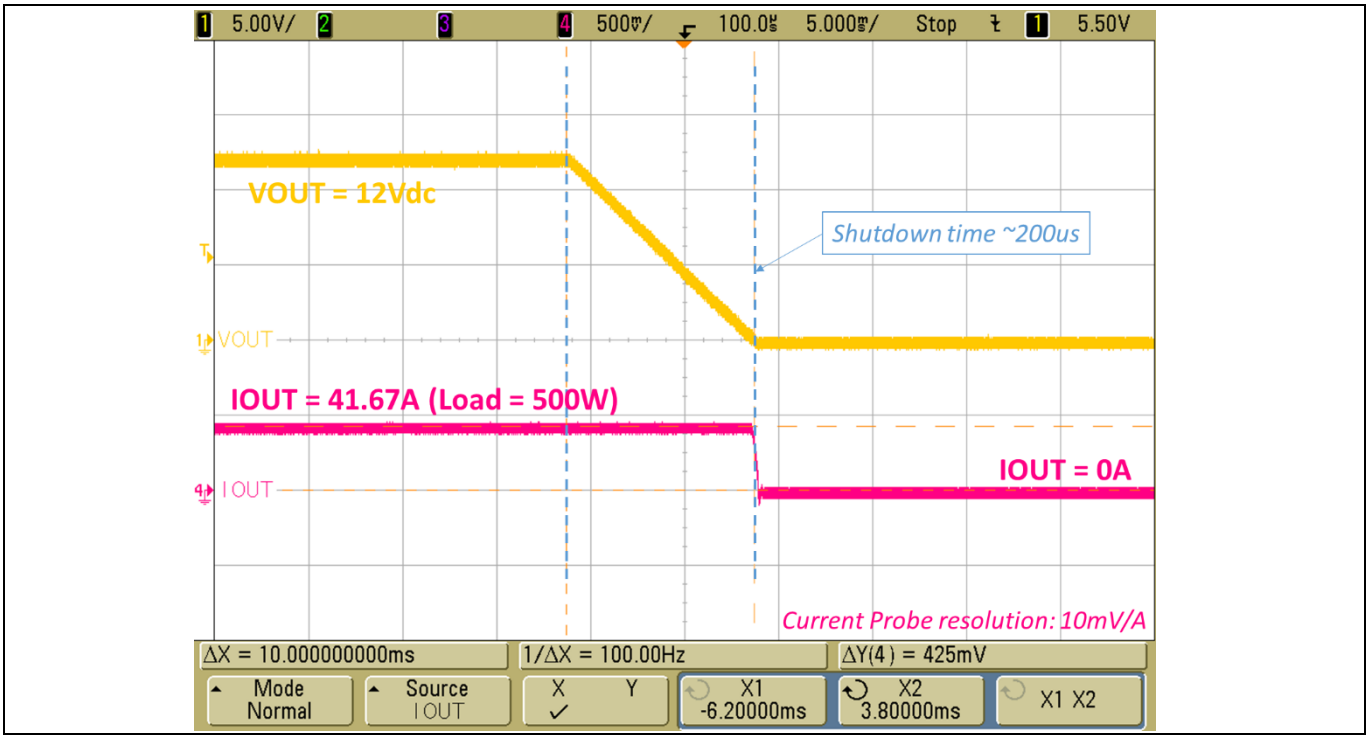

Figure 33 Shutdown waveforms at 500 W

5.3 Telemetry accuracy

5.3.1 Output voltage telemetry

The voltage sense ADC is an 11-bit ADC with 50 MHz sampling rate. The ADC resolution is 1.25 mV and enhanced with 3-bit digital modulation for output voltage regulation, which gives 156 µV resolution at the sense pin. The output voltage is sensed via voltage divider resistors with scaling factor of 0.11 and then routed to VSEN/VREF pins.

The output voltage telemetry measurement is tested at 360 V, 380 V and 400 V input at 100 W incremental load step ranging from 100 W to 1000 W. The following chart shows the output voltage telemetry performance that is able to achieve below ±0.5 percent accuracy.

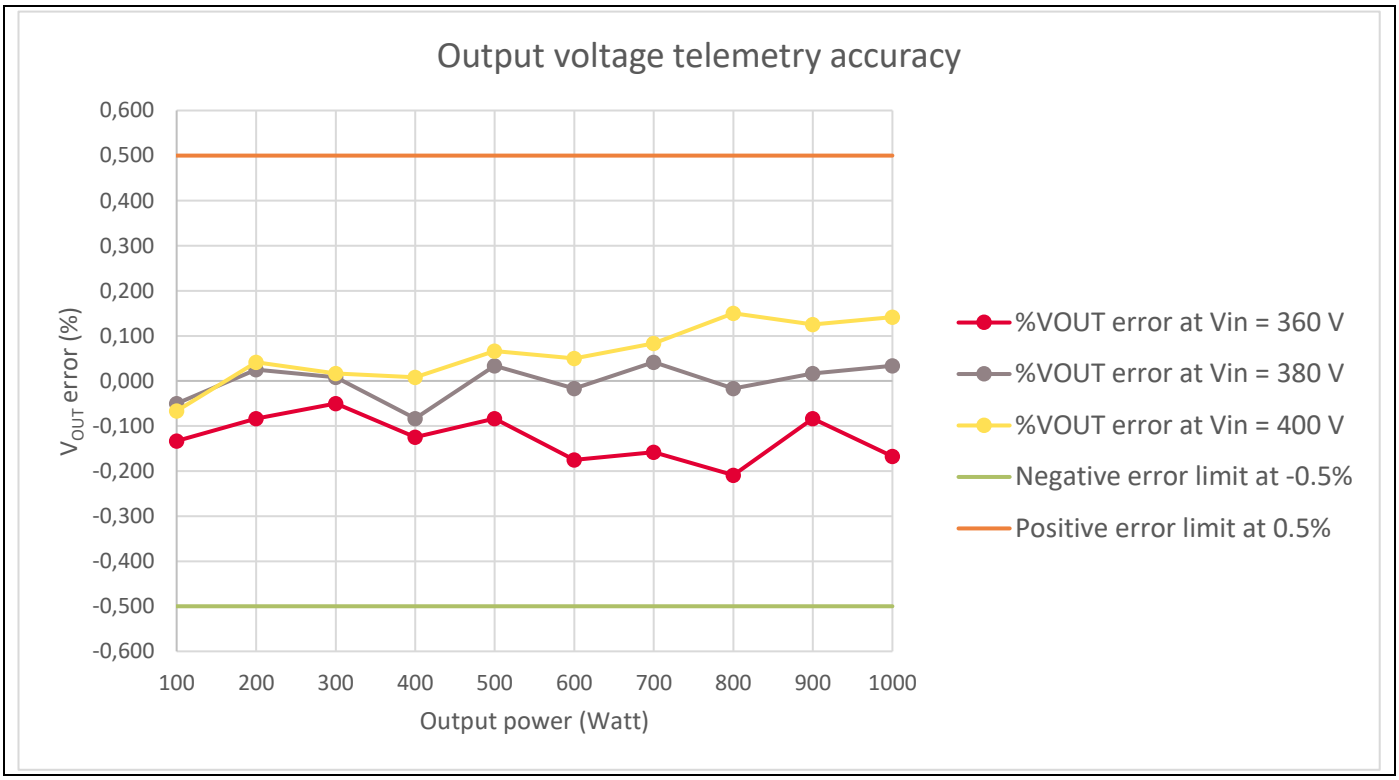

Figure 34 Output voltage telemetry accuracy

5.3.2 Output current telemetry

The CS ADC is a 9-bit ADC with 25 MHz sampling rate. Noise immunity is further improved by the use of an internal current estimator. This design uses PCB shunt trace at 0.2 mΩ. The output current signal from the shunt trace is amplified via external op-amp to improve signal-to-noise (SNR) ratio. The op-amp output signal is routed to BISEN/BIREF pins.

The output current telemetry measurement is tested at 360 V, 380 V and 400 V input at 100 W incremental load step ranging from 100 W to 1000 W. Output current telemetry performance shows that is able to achieve less than ±4 percent accuracy.

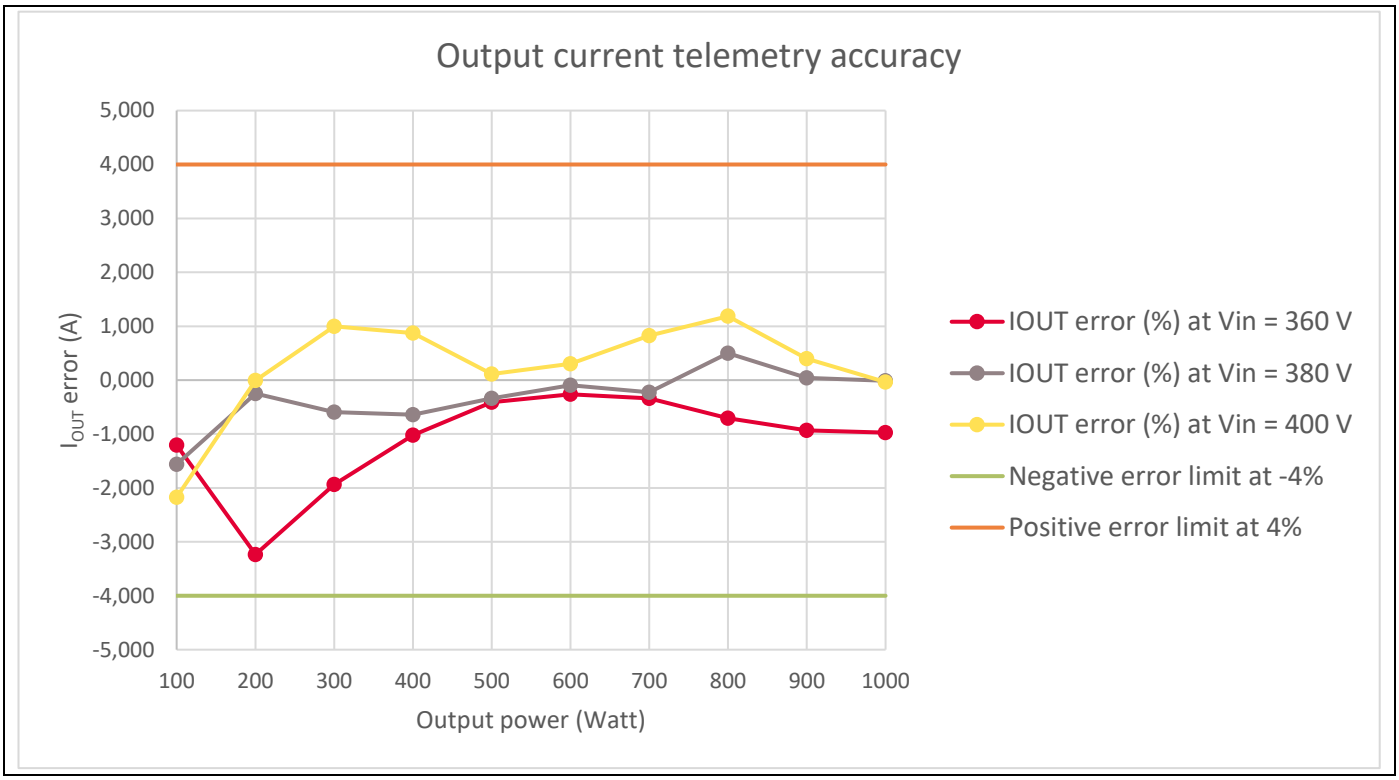

Figure 35 Output current telemetry accuracy

5.3.3 Input voltage telemetry

XDPP1100 senses input voltage from the secondary side by an indirect measurement method called V_{rect} sensing.

V_{rect} sensing measures the rectified voltage on the secondary side of the transformer. This measured voltage is scaled through the voltage divider circuit and then routed to VRECT/VREF pins. Since both transformer turns ratio and voltage divider ratio are known, the input voltage on the primary side can then be derived.

The following chart shows the input voltage telemetry measurement tested at 360 V, 380 V and 400 V input at 100 W incremental load step ranging from 100 W to 1000 W. Input voltage telemetry via V_{rect} sensing shows that it is able to achieve less than ±4 percent accuracy.

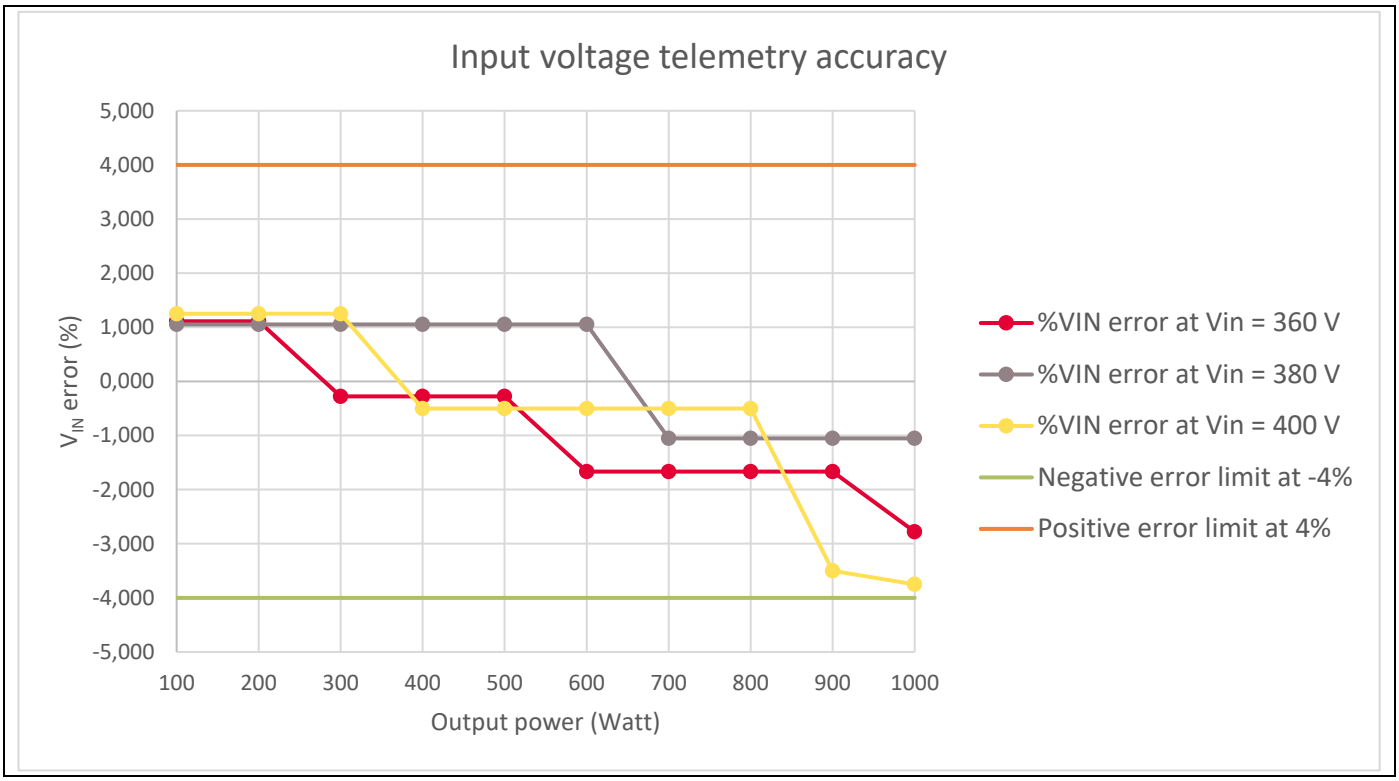

Figure 36 Input voltage telemetry accuracy

5.3.4 Input current telemetry

Input current I_{IN} is estimated based on V_{OUT}, I_{OUT} and V_{IN}. Both V_{OUT} and I_{OUT} are directly measured via VSEN/VREF and BISEN/BIREF pins respectively, while V_{IN} are measured indirectly via V_{rect} sensing. Given these parameters, I_{IN} can be approximated with the $I_{IN} = V_{OUT} * I_{OUT} / V_{IN}$ relationship. This approximation is done internally with a hardware module in XDPP1100.

The following chart shows the input current telemetry measurement tested at 360 V, 380 V and 400 V input at 100 W incremental load step ranging from 100 W to 1000 W. Input current telemetry shows that it is able to achieve less than ±1.0 A accuracy.

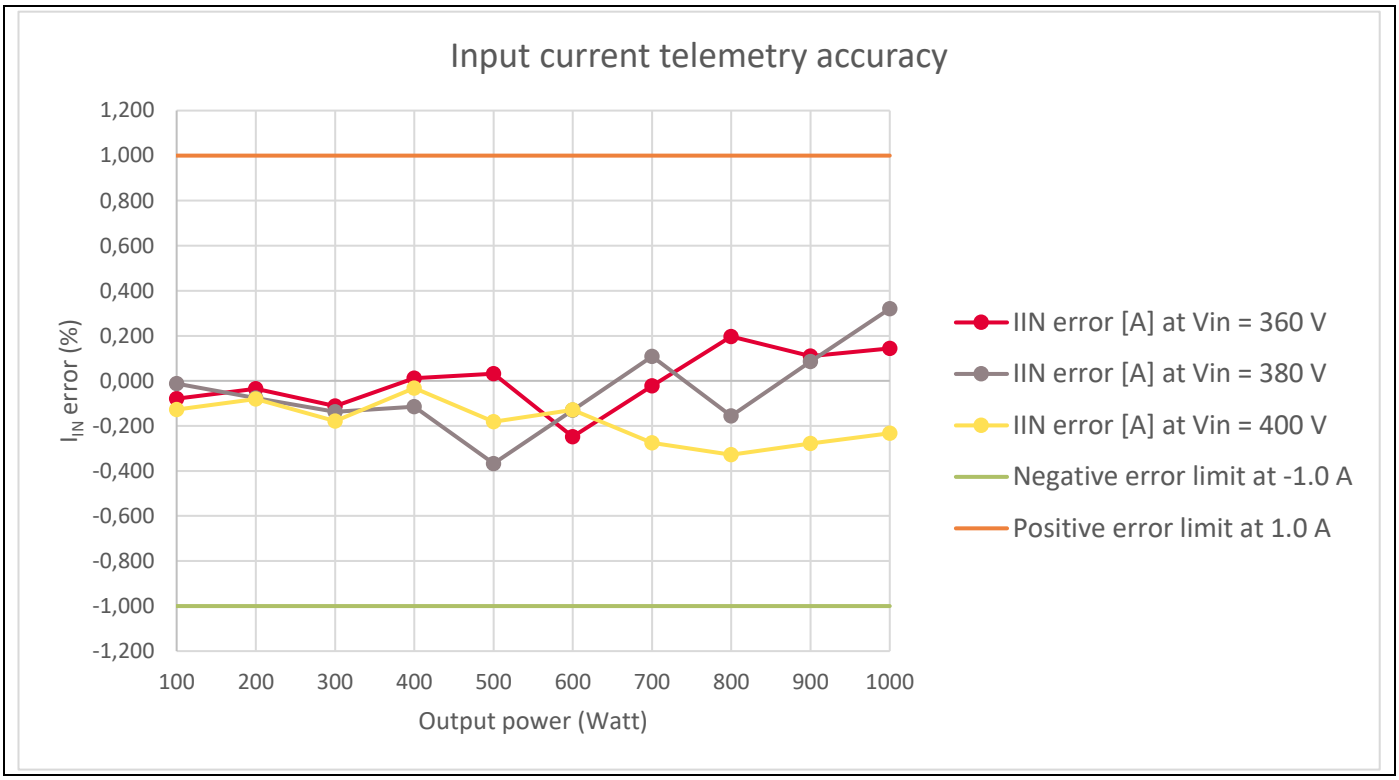

Figure 37 Input current telemetry accuracy

5.4 Protection

Fault performance is shown in the figures below. For instance, OCP and OVP/UVP are presented as major protection faults.

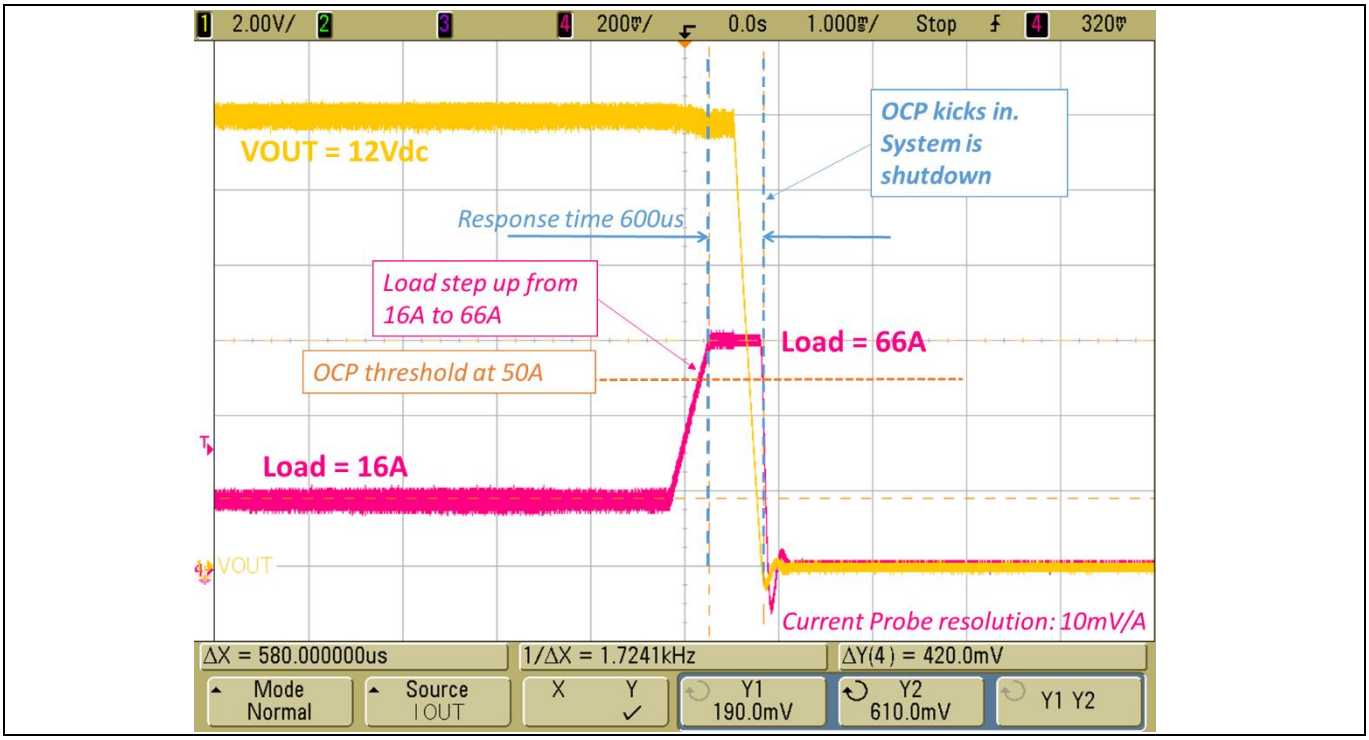

Figure 38 Output current protection (OCP) with threshold set at 10 A

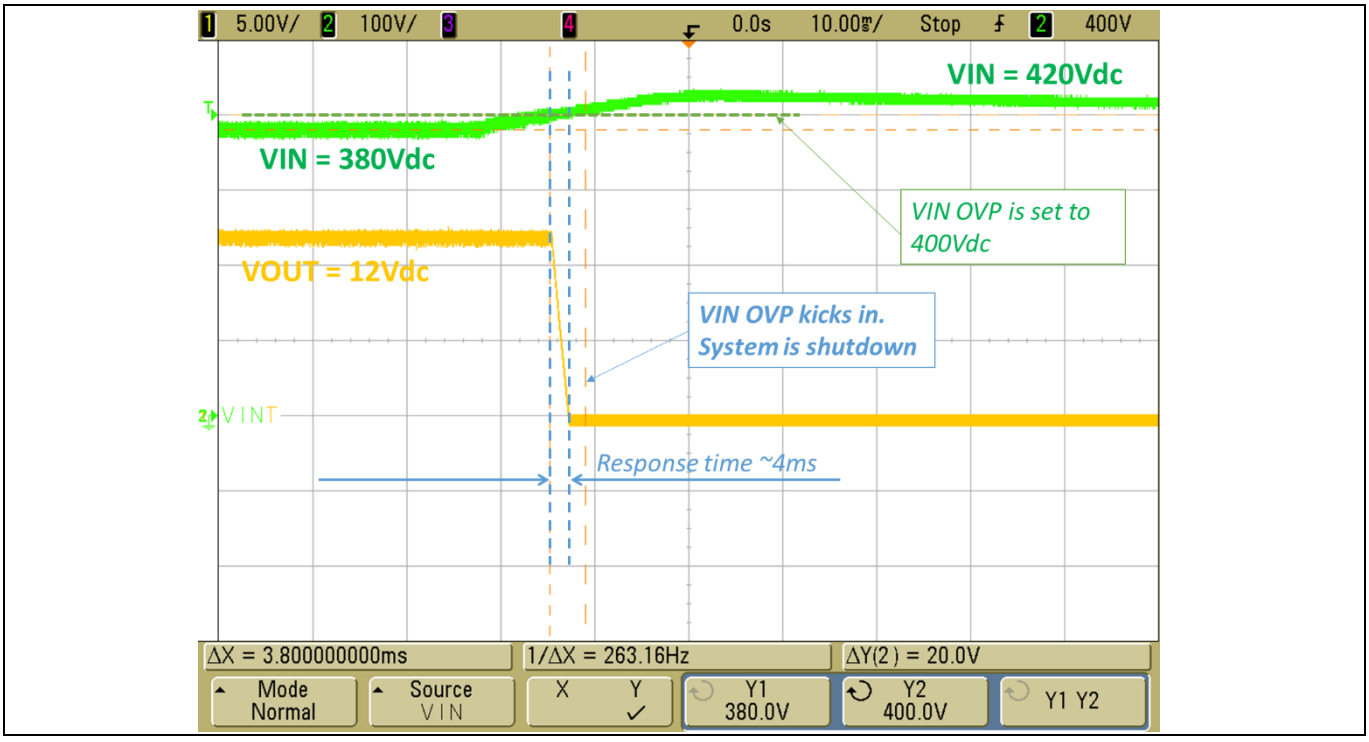

Figure 39 Input voltage overvoltage protection (V_{IN} OVP) with threshold set at 400 V DC

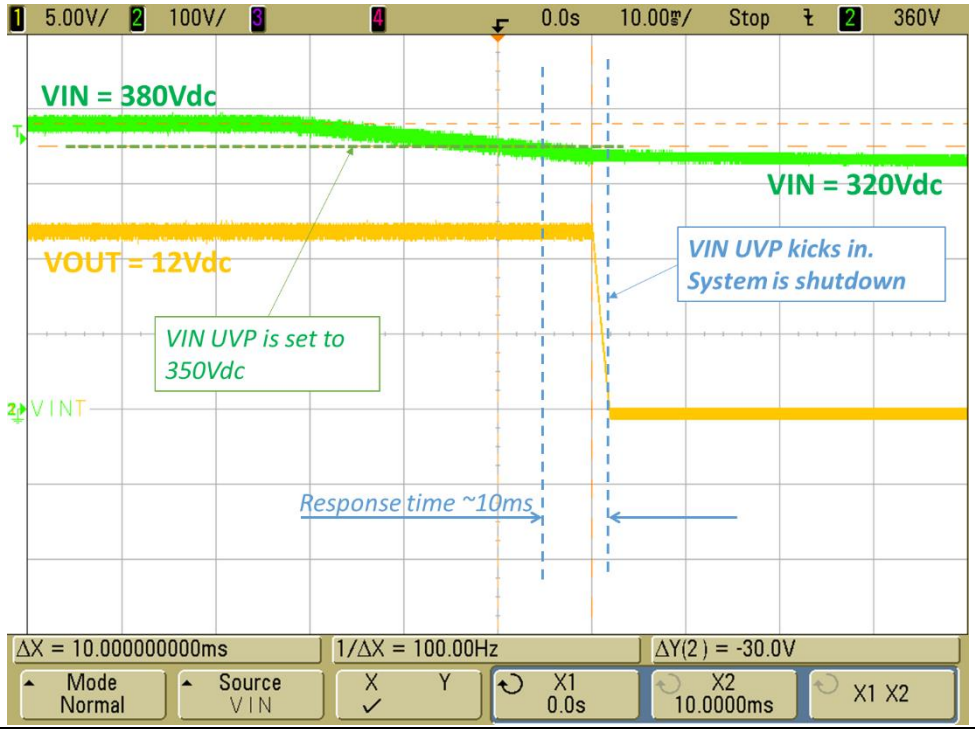

Figure 40 Input voltage undervoltage protection (V_{IN} UVP) with threshold set at 350 V DC

6 Schematics

6.1 Main Board

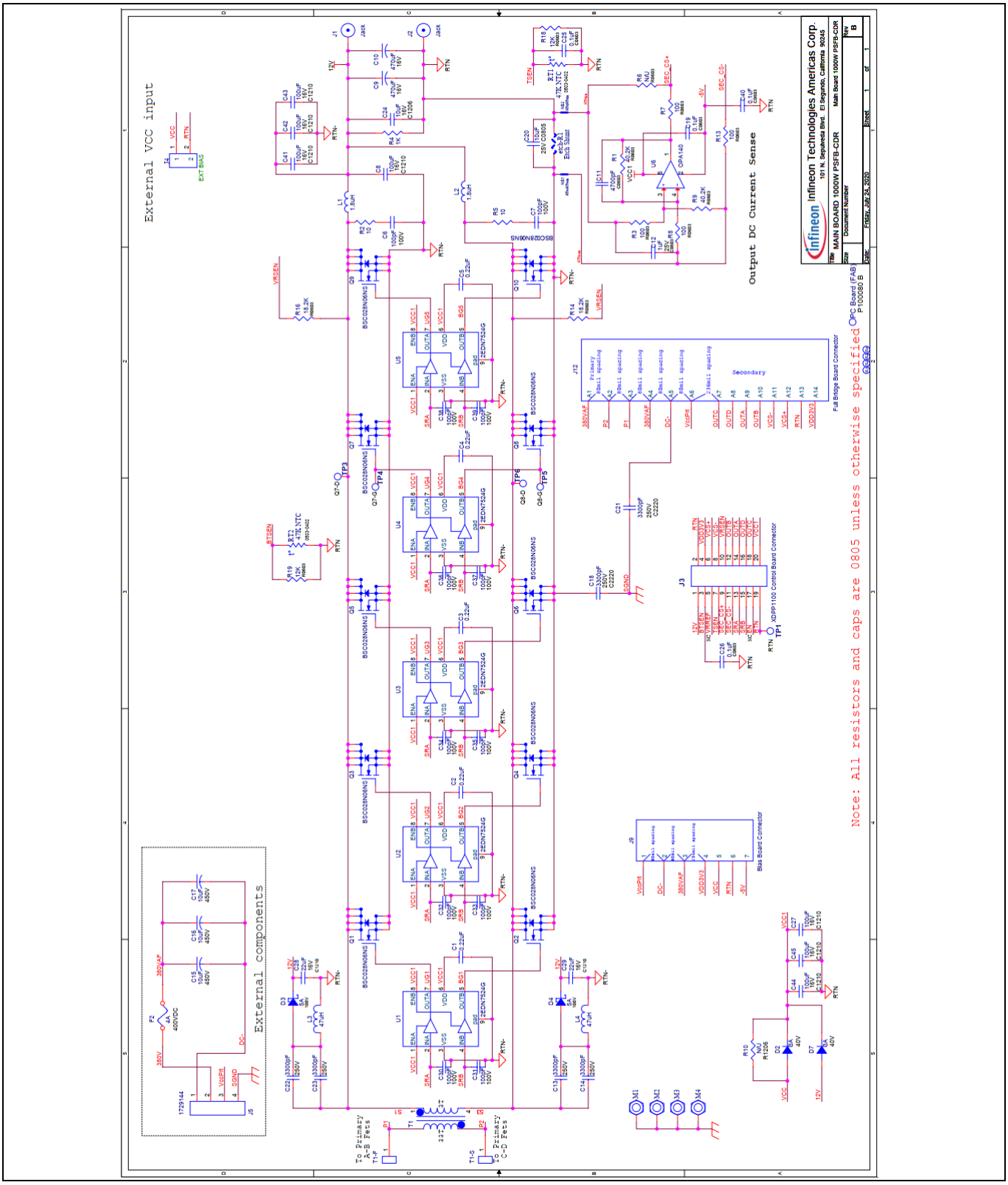

Figure 41 Main Board Schematic

6.2 Full Bridge Board

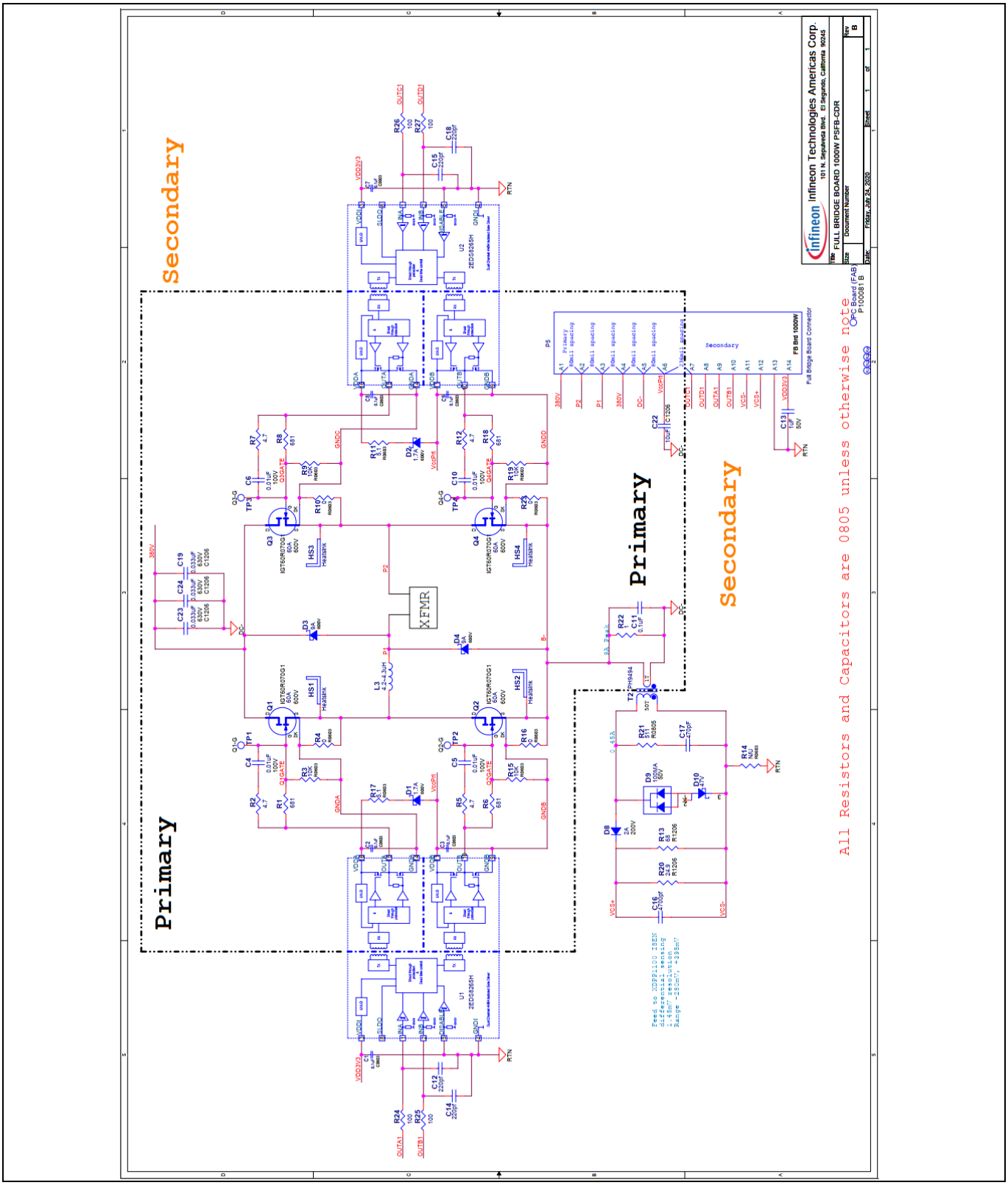

Figure 42 Full Bridge Board Schematic

6.3 Auxiliary Bias Board

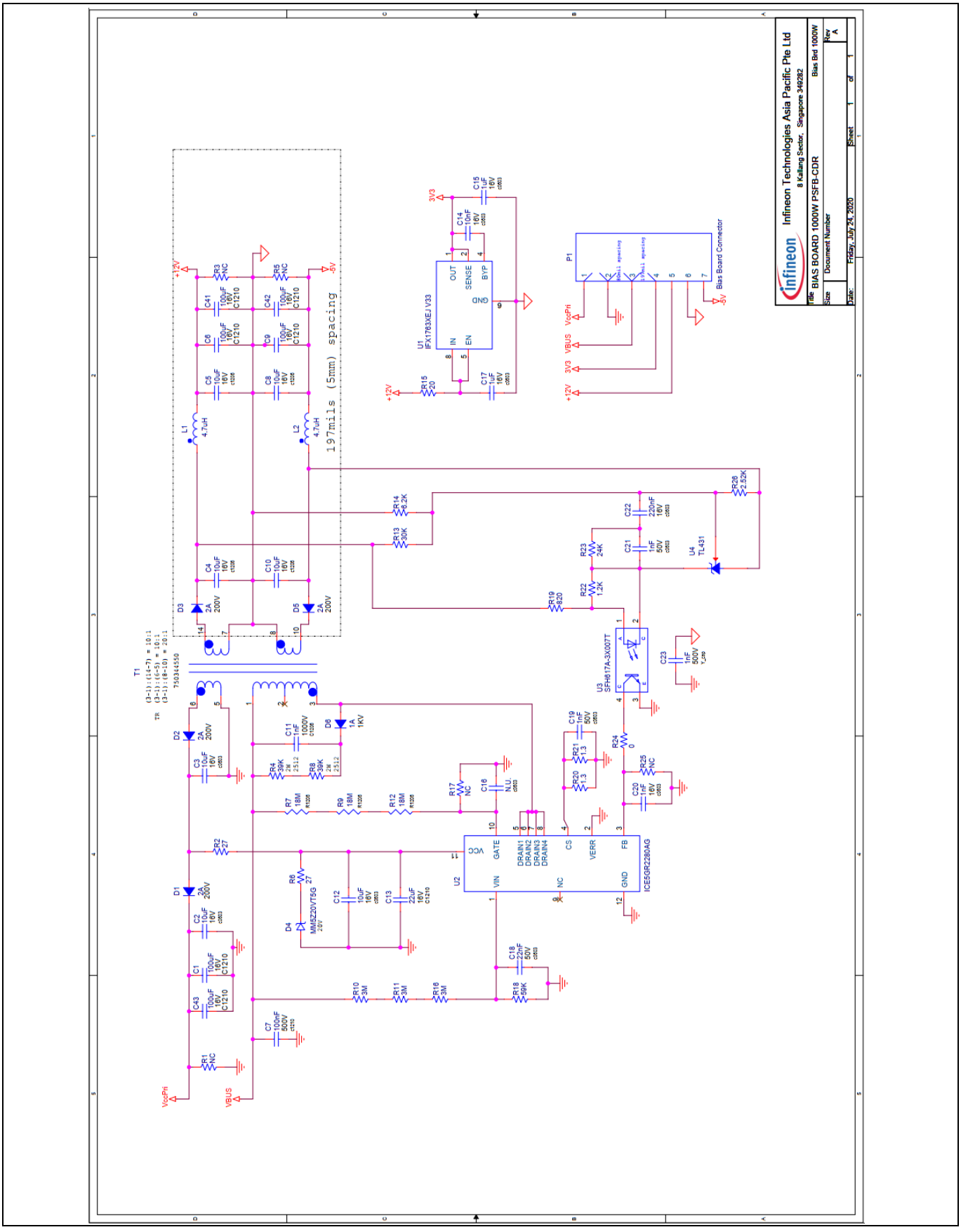

Figure 43 Auxiliary Bias Board Schematic

6.4 Control Board

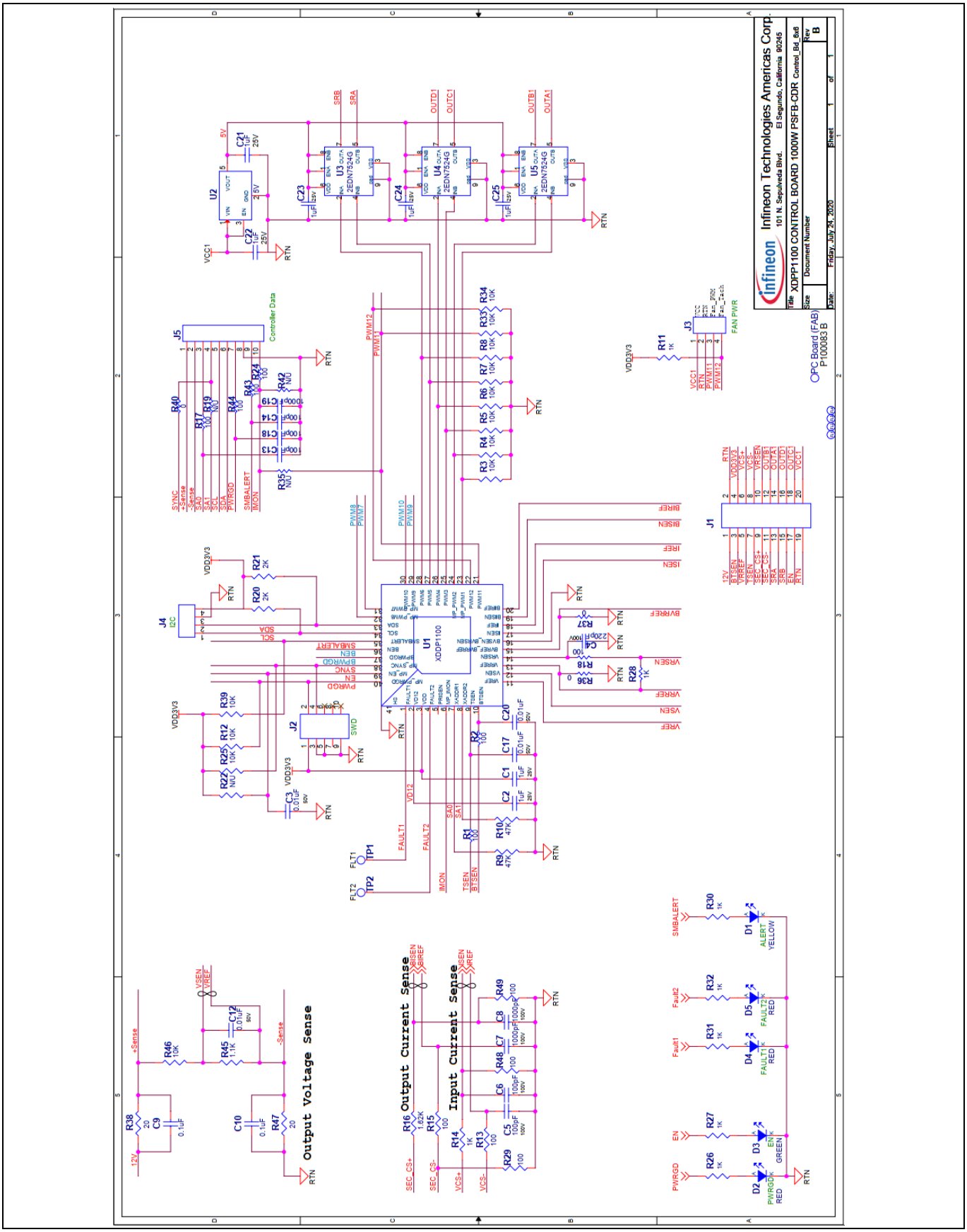

Figure 44 Control Board Schematic

7 Magnetics

7.1 Main board

7.1.1 Full-bridge transformer

Table 9 Main transformer material

Item	Description	Manufacturer	Part Number
1	Core # TN 26 / 15 / 15 – 3F36 material with 12mil (0.3mm) gap	FERROXCUBE	TN26/15/15-3F36
2	Triple insulated LITZ wire. (230 strands of 44 gauge wire)	RUBADUE	TXXL230/44F3XX-2
3	MWS# 75/41 SPNSN litz wire. (75 strands of 41 gauge wire)	MWS	100141 SPNSN LITZ WIRE
4	3M™ 56 Polyimide Film Electrical Tape 0.25” wide, 3 mil	3M	1218 1/4” x 36 YD
5	Teflon sleeve 10ga diameter	3M	FP301-1/8-48-Yellow
6	Label	AVERY	1/2” LABEL 5418
7	KAPTON polyimide film tape 0.5” wide, 3 mil thick	3M	1218 1/2” x 36 YD

The electrical drawing and mechanical drawing are shown in Figure 45 and Figure 46. It has 33 turns in primary, and two secondary windings each has 3 turns.

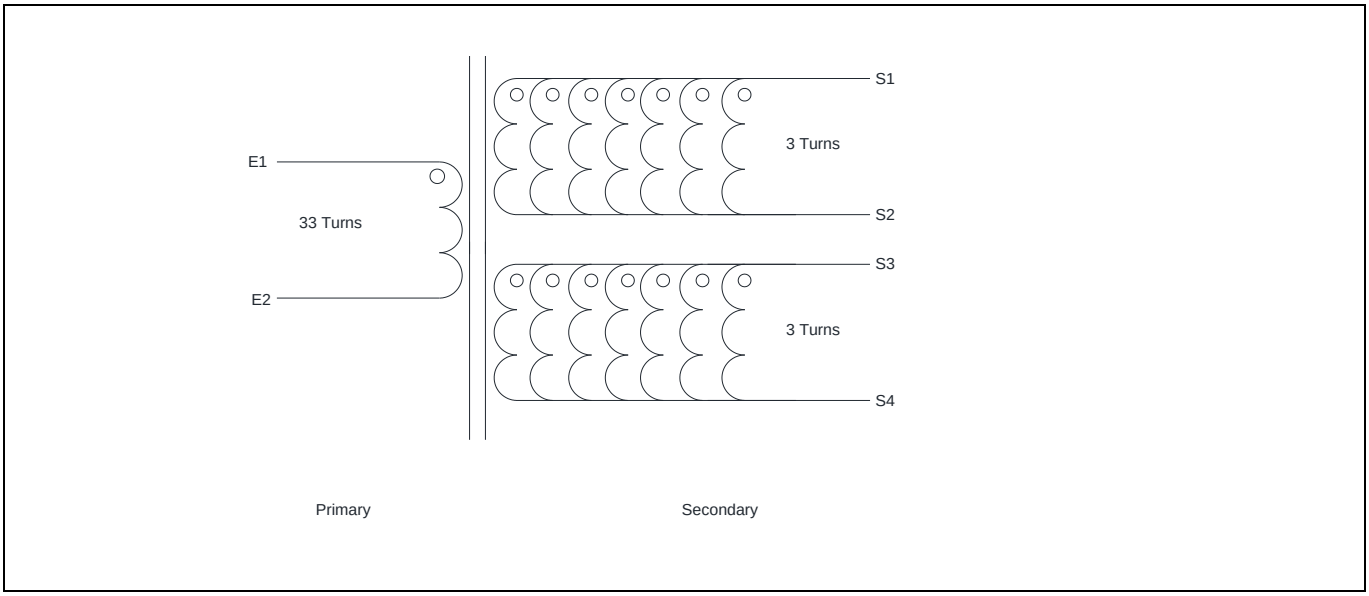

Figure 45 Main transformer schematic

Core prep Instructions:

1. Stack 10 layers of tape, Item 4, on top of each other 1.8 inches long.
2. Apply a 2.3 ” long piece of tape, item 7, over 10 layer tape bundle to help secure it to core.
3. Apply the 10 layers of stacked tape bundle and wrap over the cut gap on core, item 1, as shown. Use the 0.5 inch wide piece of applied Kapton wrapper tape, item 7, to help secure tape bundle to core.

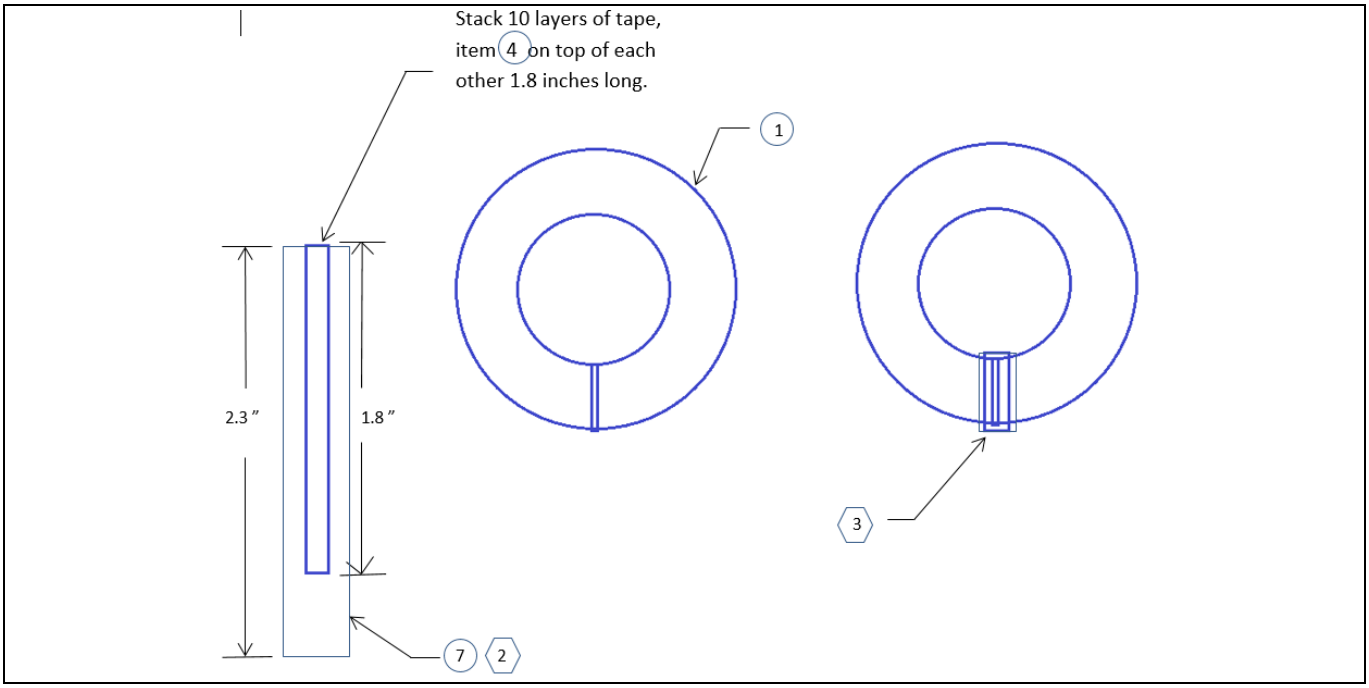

Figure 46 Core preparing

Winding instruction:

1. Wind W1, W2 and W3 evenly across the entire toroid, item 1.
2. Identify start of the winding with a flag, item 4.
3. Strip start and finish lead 0.25” from the end and tin leads. See Diagram next page.
4. Twist start and finish flying leads 2 turns per inch. See Diagram next page.
5. Twist individual start and finish flying leads S2, S3 at 4 turns per inch before tinning leads 0.75” long to bottom of core as shown. Apply 10 ga teflon sleeving, item 5, as shown. See Diagram next page.
6. Secure label using tape around entire circumference as shown, item 4.

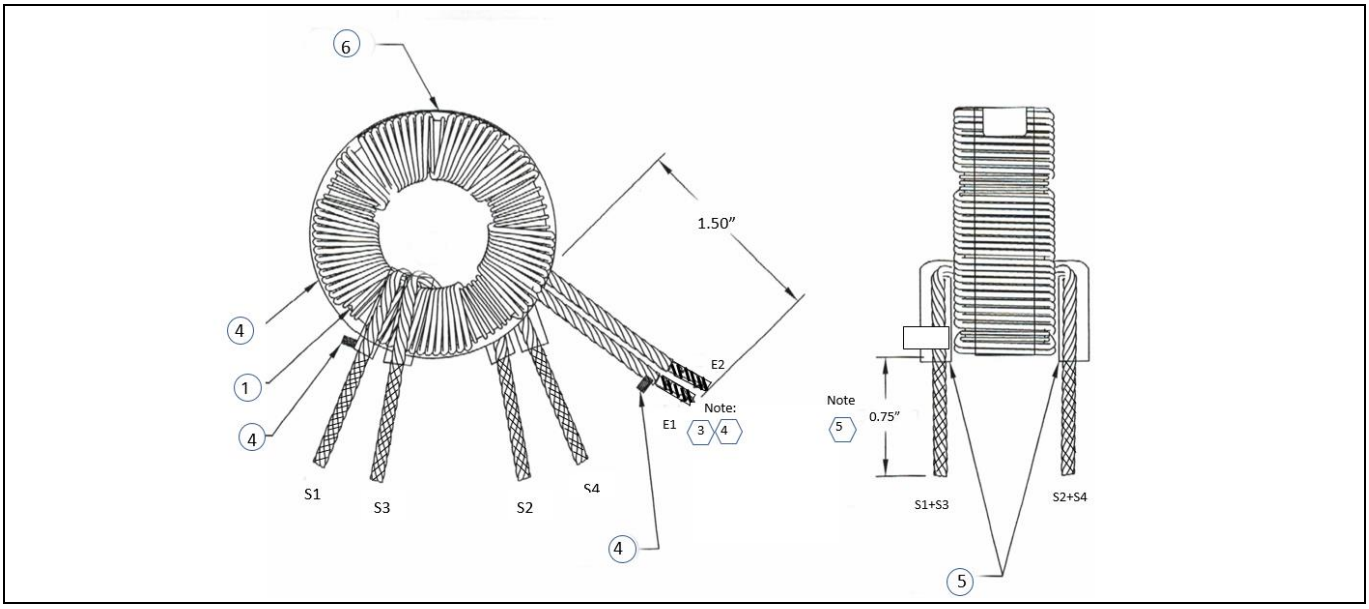

Figure 47 Main transformer mechanical drawing

Table 10 Main transformer winding structure

Winding#	S 1 F	S 2 F	S 3 F
Wire type,size Ref des	(230*44 tri layer litz) Item 2	7 filar x (75*41 litz) Item 3	7 filar x (75*41 litz) Item 3
Turns	33	3	3
Tapped	-	-	-
Lead out Position	-	-	-
Lead out type and length	flying	flying	flying
Turns per layer	33	21	21
Total layers	1 , 7	1	1
Layer Insulation	-	-	-
wrapper	-	-	-
Terminals #'s	E1, E2	S1,S2	S3,S4
Instructions	1,2,3	1,2,5	1,2,5

Table 11 Main transformer spec

Parameter	Terminals	Method- Instrument and settings	Limits
Inductance	E1 – E2	Set test frequency to 10Khz during test	620 uh – 700 uh 574 uH
Leakage inductance	E1 – E2	Short secondary leads S1 S2, S3, S4 together and measure primary inductance at 10Khz.	0.5 uh – 1.2 uh 26 uH
Hipot testing		From E1 to S1 + S3	3600 V AC / 1 sec

Board assembly:

- Sit transformer on PCB with S1, S3 connected to the dot name side, connect S2, S4 to the non-dot side
- Connect primary winding E1 to T1-2 (dot name), connect E2 to T1-F

7.1.2 Output inductor

Table 12 Output inductor material

Item	Description	Manufacturer	Part Number
	Magnetics core# C055848-A2		
	15 Ga Hynz wire red		
	Kapton polyimide Film Electrical Tape 0.25” wide		
	Label		

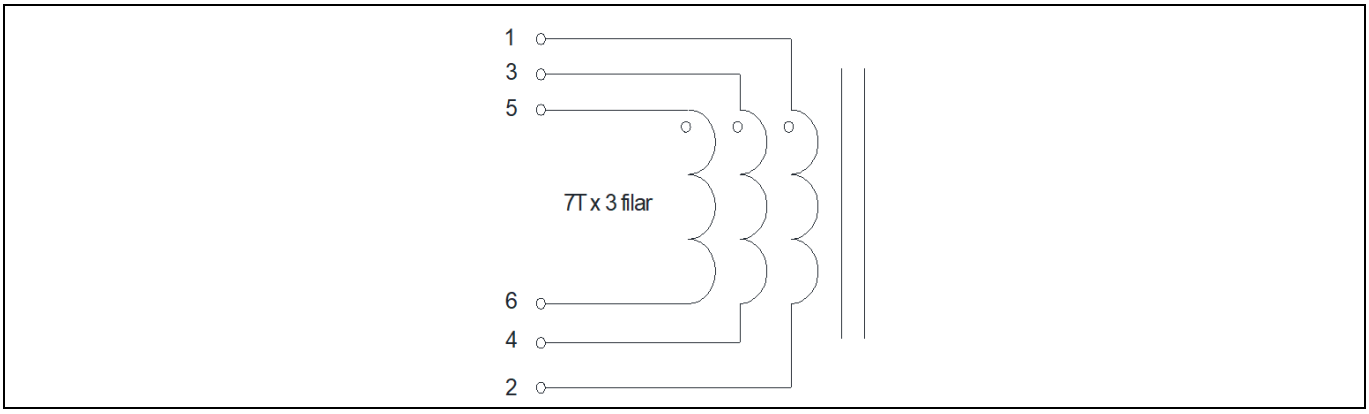

Figure 48 Output inductor schematic

Figure 49 Output inductor winding instruction

Winding#	**S 1 F**	
Wire type,size	Trifilar x 15 AWG HYNZ	
Turns	7	
Tapped	-	
Lead out position	-	
Lead out type and length	Self lead	
Turns per layer	21	
Total layers	1	
Layer insulation	-	
wrapper	-	
Terminals #’s	1,3,5 – 2,4,6	
Instructions	1,2	

Winding instruction:

1. Wind evenly across the entire bobbin.
2. Tin leads 0.5 inch to bottom of core as shown.

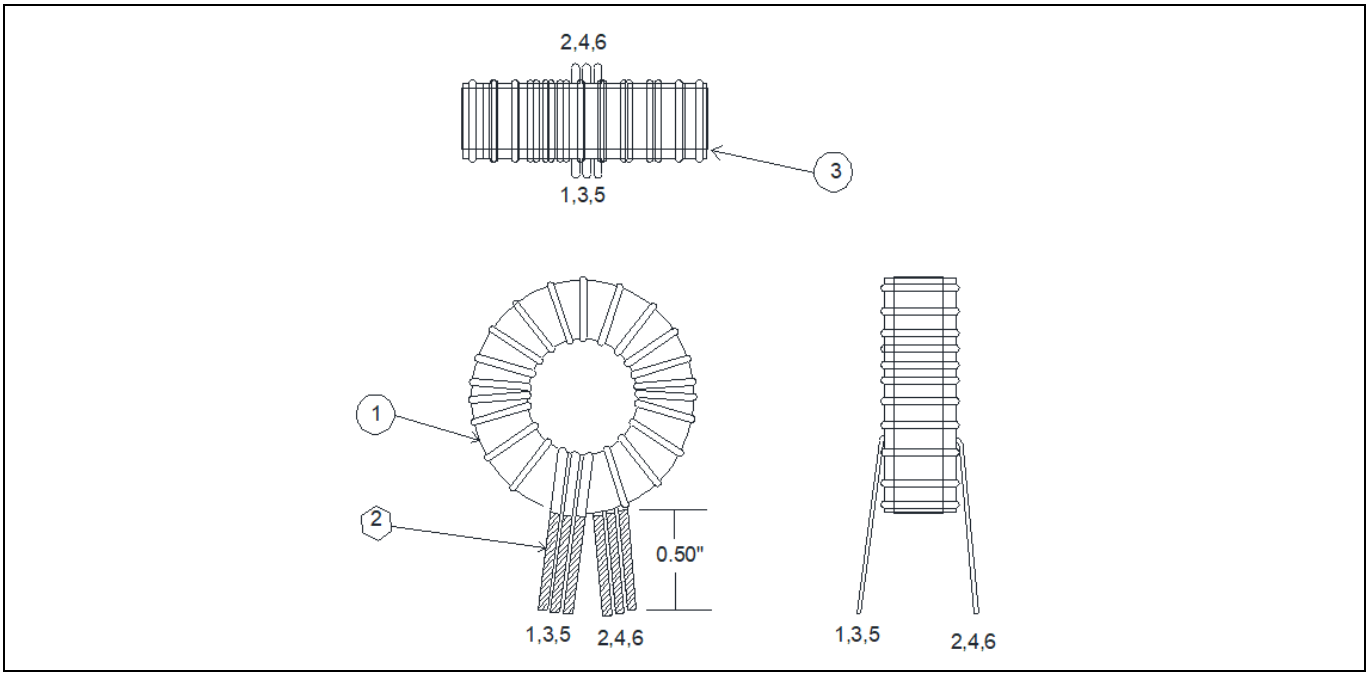

Figure 50 Output inductor drawing

Figure 51 Output inductor spec

Parameter	Terminals	Method- Instrument and settings	Limits
Inductance	1,3,5 – 2,4,6	Set test frequency to 10Khz during test	1.4uh – 2.1uh

7.2 Full bridge board

7.2.1 Resonant inductor

Table 13 Resonant inductor material

Item	Description	Manufacturer	Part Number
	Magnetics core# T50-2.		
	Rubadue# TXXL40/40T2XX-2 (MW80) triple insulated litz wire. (40 strands of 40 gauge wire).		
	Kapton polyimide Film Electrical Tape 0.125” wide.		
	Label		

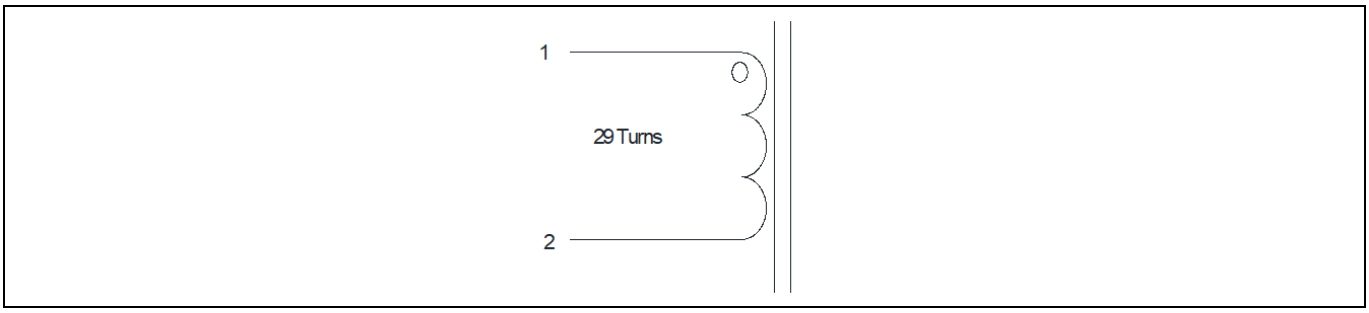

Figure 52 Resonant inductor schematic

Table 14 Resonant inductor winding instruction

Winding#	**S 1 F**	
Wire type,size Ref des	40*40 tri layer litz 2	
Turns	29	
Tapped	-	
Lead out position	-	
Lead out type and length	Self lead	
Turns per layer	29	
Total layers	1	
Layer insulation	-	
wrapper	-	
Terminals #’s	1 – 2	
Instructions	1,2,3	

Winding instruction

1. Wind evenly across the entire bobbin.
2. Strip and Tin leads 0.5 inch to 0.1” from bottom of core as shown.
3. Wrap core with 0.125” wide tape, item 3.

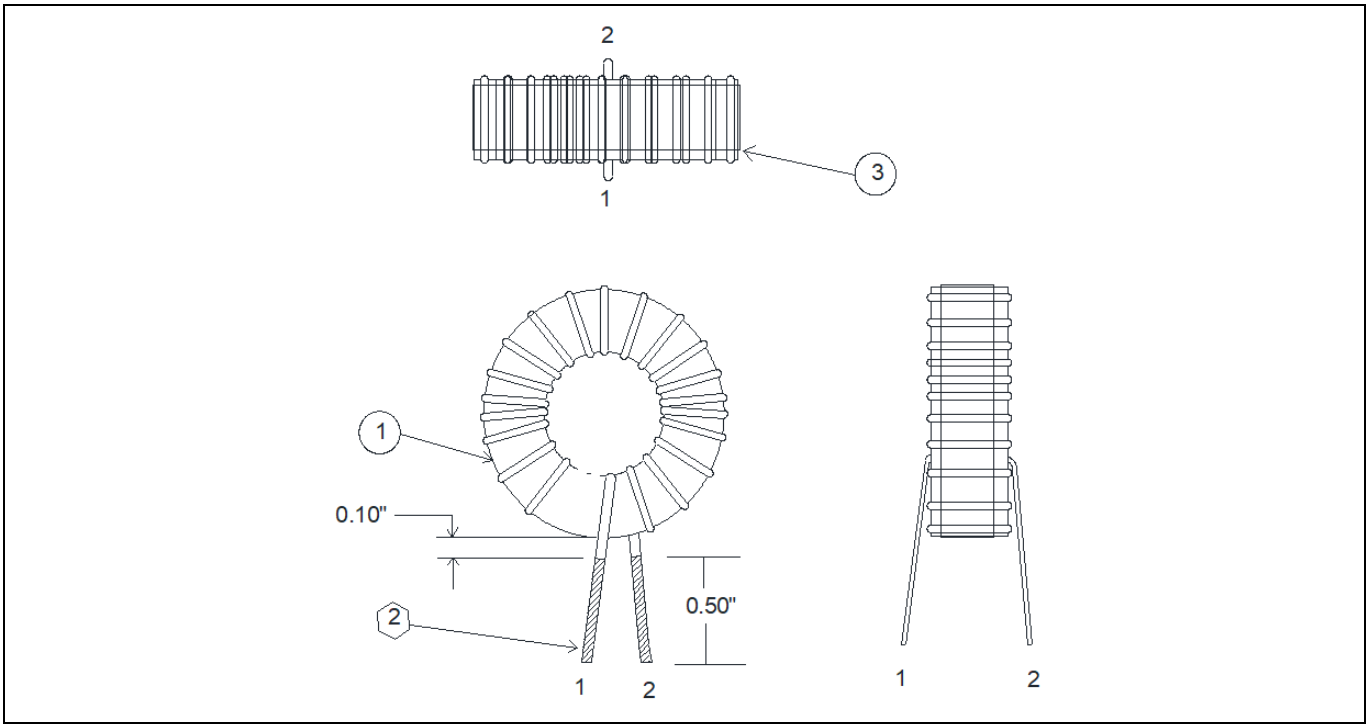

Figure 53 Resonant inductor drawing

Table 15 Resonant inductor spec

Parameter	Terminals	Method- Instrument and settings	Limits
Inductance	1 – 2	Set test frequency to 10Khz during test	4uh – 4.7uh

7.2.2 Current sense transformer

Table 16 Current transformer material

Item	Description	Manufacturer	Part Number
1	Magnetics core # 41005-TC with P type material		
2	30 Ga HYNZ wire		
3	18 Ga UL1569 wire		
4	Label		
5	Kapton polyimide Film Electrical Tape 0.25” wide, 3 mil thick		

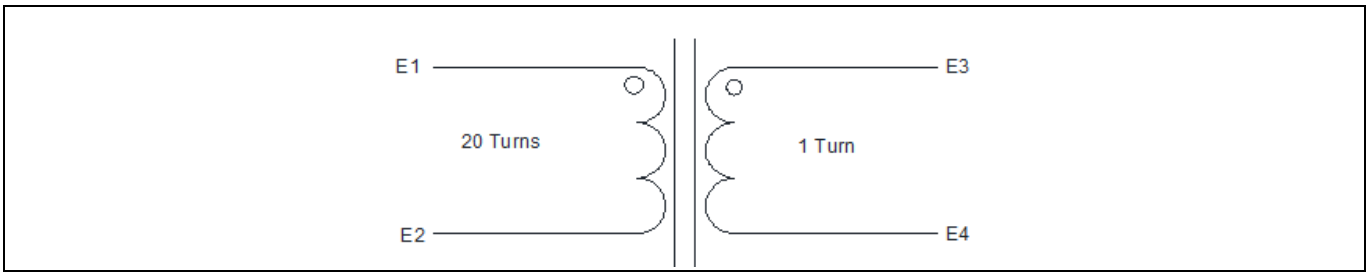

Figure 54 Current transformer schematic

Table 17 Current transformer winding structure

Winding#	S 1 F	S 2 F
Wire type,size Ref des	28 AWG Hynz Item 2	18 Ga Tri layer Item 3
Turns	20	1
Tapped	-	-
Lead out position	-	-
Lead out type and length	Flying	Flying
Turns per layer	20	1
Total layers	1	1
Layer insulation	-	-
wrapper	-	-
Terminals #’s	E1 - E2	E3 – E4
Instructions	1, 2	1, 3, 4

Winding instruction:

1. Wind evenly across the entire bobbin.
2. Tin leads E1 and E2 on winding number one, 1.25 inch long at one inch away from side of core as shown on following page.
3. Strip and tin leads on winding number two, 1 inch long to bottom of core as shown on following page.
4. Apply a piece of tape to identify the start lead E3 of winding 2 as shown on following page.

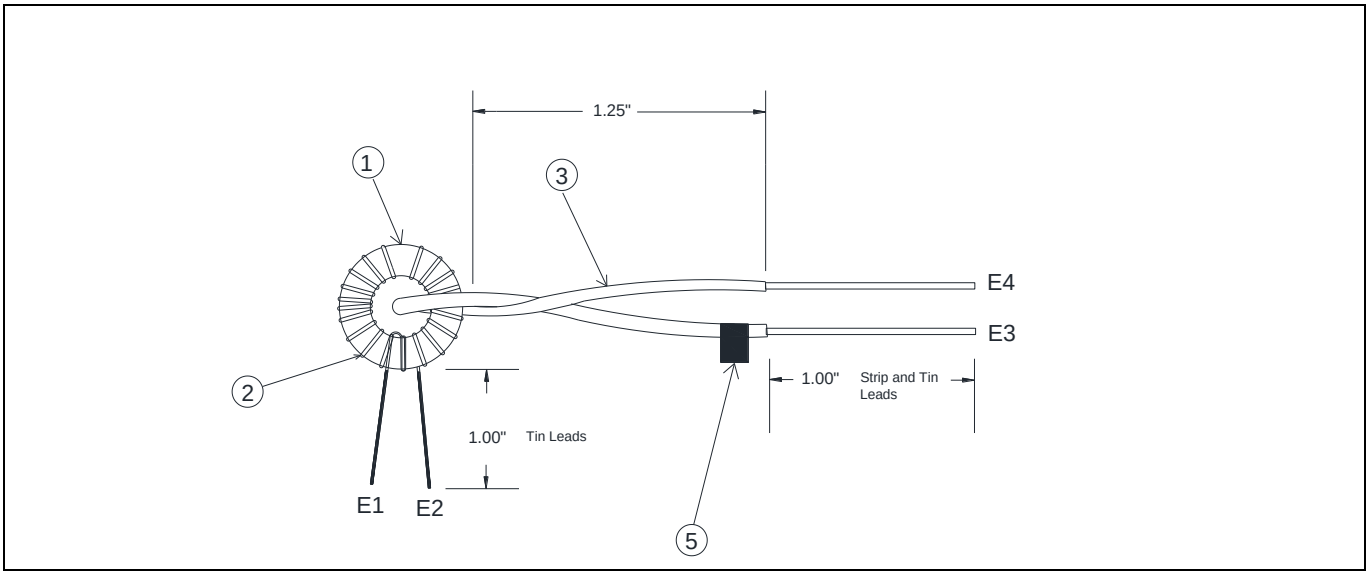

Figure 55 Current transformer drawing

Table 18 Current transformer spec

Parameter	Terminals	Method- Instrument and settings	Limits
Inductance	E1 - E2 E3 – E4	Set test frequency to 10 Khz during test	600 uh – 800 uh 1.3 uh – 2 uh
Leakage inductance			
DC resistance			
Ratio and phasing	E1 – E2	Apply 2.0 V AC at 10khz	2.0 V AC (REF)
	E3 – E4		0.05 V AC – 0.15 V AC
Leakage current			
Hipot testing	FROM E1 TO E3		3600 V AC / 1 sec
	FROM TO		
	FROM TO		

7.3 Auxiliary bias board

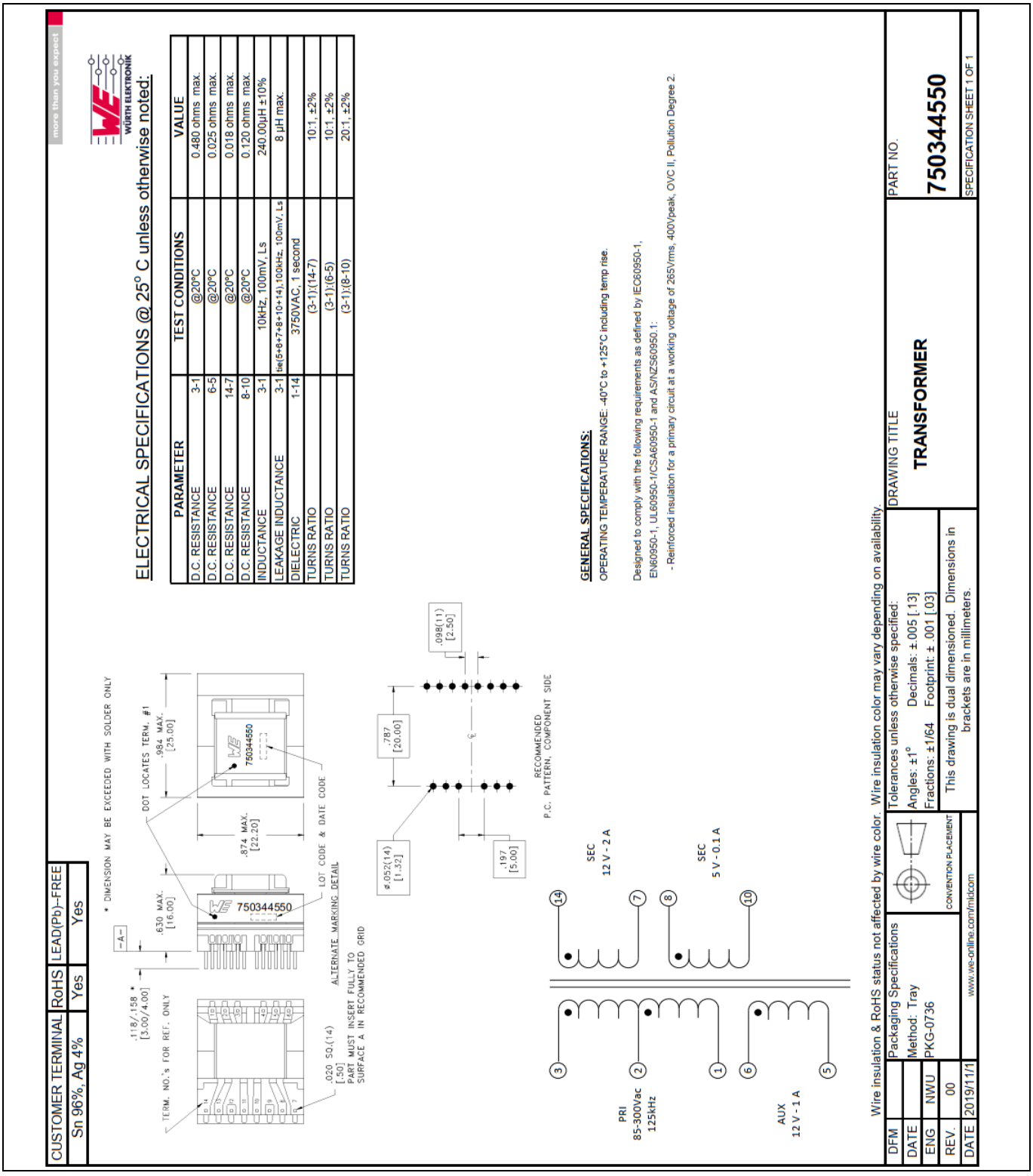

Figure 56 Auxiliary Flyback Transformer

8 Further improvements

There are several things that can be done to further improve overall system performance:

- Increase the rated power from 1000 W to 1600 W. Most server and telecom power supplies are operating at 1600 W. Digital controller and premium products such as GaN make more sense when implemented at higher power-rating power supplies. Low power-rating power supplies are more competitive and price-sensitive markets. At 1600 W, the power supplies are considered high-end and therefore GaN and a digital controller make more sense.
- Replace toroidal magnetics with mass-produced magnetics. The existing board was meant for prototyping and to act as proof-of-concept and therefore toroidal, hand-wound magnetics are used. In order to release this design for customer evaluation, it is important to use scalable and mass-production grade magnetics.
- Consider proper wire gauges (AWG) when designing the magnetics. Existing magnetics use under-spec AWG wires for all the magnetics, and this affects overall system efficiency.

9 Summary

This document introduces a complete Infineon system solution for a 1000 W PSFB-CDR isolated DC-DC converter achieving 95.36 percent peak efficiency.

XDPP1100 is a highly integrated and programmable digital power supply controller. It has a unique architecture that includes many optimized power-processing digital blocks to enhance the performance of isolated DC-DC converters, reduce external components and minimize firmware development effort. For advanced power conversion and monitoring, the XDPP1100 also provides accurate telemetry and power management bus (PMBus) interface for system communication. These advanced features make it an ideal power controller for modern high-end power systems employed in telecom and server infrastructure.

Specific power management peripherals have been added to enable high efficiency across the entire operating range, high integration for increased power density, reliability and lowest overall system cost and high flexibility with support for the widest number of control schemes and topologies. Such peripherals include: SR, input voltage FF, copper trace CS with temperature compensation, secondary-side input voltage sensing, soft-start with pre-bias, feedback loop open- or short-circuit protection, and fast load-transient response.

The XDPP1100 supports many commonly used DC-DC topologies such as hard-switched full-bridge and half-bridge, phase-shifted full-bridge, active clamp forward, full-bridge and half-bridge current-doubler rectifier, interleaved active clamp forward, interleaved half-bridge, and interleaved full-bridge. A dual-rail version of XDPP1100 also supports pre-buck or post-buck configuration.

When combined with other Infineon best-in-class devices such as CoolGaN™, OptiMOS™, EiceDRIVER™ and CoolSET™, this system solution is able to demonstrate the feasibility of using XDPP1100 on a high-voltage 1000 W PSFB CDR for telecom and server applications.

10 References

[1] Infineon Technologies, 2020. “XDPP1100 Digital Power Supply Controller” datasheet.

[2] Infineon Technologies, 2020. “Application Guide – Digital Power Controller XDPP1100”, AN_2003_PL88_2006_221026, application guide.

[3] Infineon Technologies, 2020. “Application Note – XDPP1100 Number Format and Conversion”, AN_2005_PL88_2006_073720, application note.

[4] Infineon Technologies, 2013. “ZVS Phase Shift Full Bridge CFD2 Optimized Design”, AN 2013-03, application note.

[5] Infineon Technologies, 2013. “Design of Phase Shifted Full Bridge Converter with Current Doubler Rectifier”, DN 2013-01, design note.

Revision history

Document version	Date of release	Description of changes
V 1.0	11-12-2020	First release

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2020-12-11

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AN_2011_PL88_2012_094733

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.