

Recommendations for Printed Circuit Board Assembly of Infineon QFN Packages

Additional Information

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1 Package Description

Plastic (Green) Very Thin Profile Quad Flat Non-Leaded Packages (P(G)-VQFNs), and, Plastic Green Very Very Thin Profile Quad Flat Non-Leaded Packages (P(G)-WQFNs) are near chip-scale plastic encapsulated packages (Figures 1, 2 and 3). On the bottom of each package, there are perimeter pads and a large die pad that is typically soldered to the Printed Circuit Board (PCB) to optimize electrical and thermal performance and provide board-level reliability. On the bottom of P(G)-IQFN packages (I = integrated) is a segmented die pad, because these are “multi-chip” packages encapsulating two or more different silicon dies. For example, they are used for Infineon’s integrated Driver MOSFET (metal-oxide-semiconductor field-effect transistor) devices.

Features:

- Optimized electrical performance due to design using no wire leads
- Enhanced thermal performance through exposed die pad structure
- Leads and exposed die pad with solder plating
- Small footprint, very thin package
- Package outline comply with JEDEC MO-220 standard
- Lead Tip Inspection (LTI) feature available for specific package outlines; please contact your sales representative for more details (Figure 4)

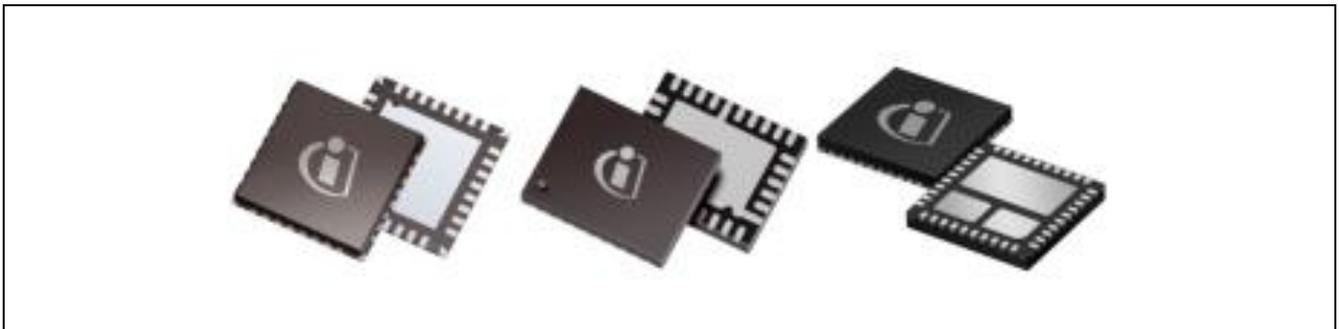


Figure 1 Examples of Infineon P(G)-VQFN and P(G)-IQFN packages

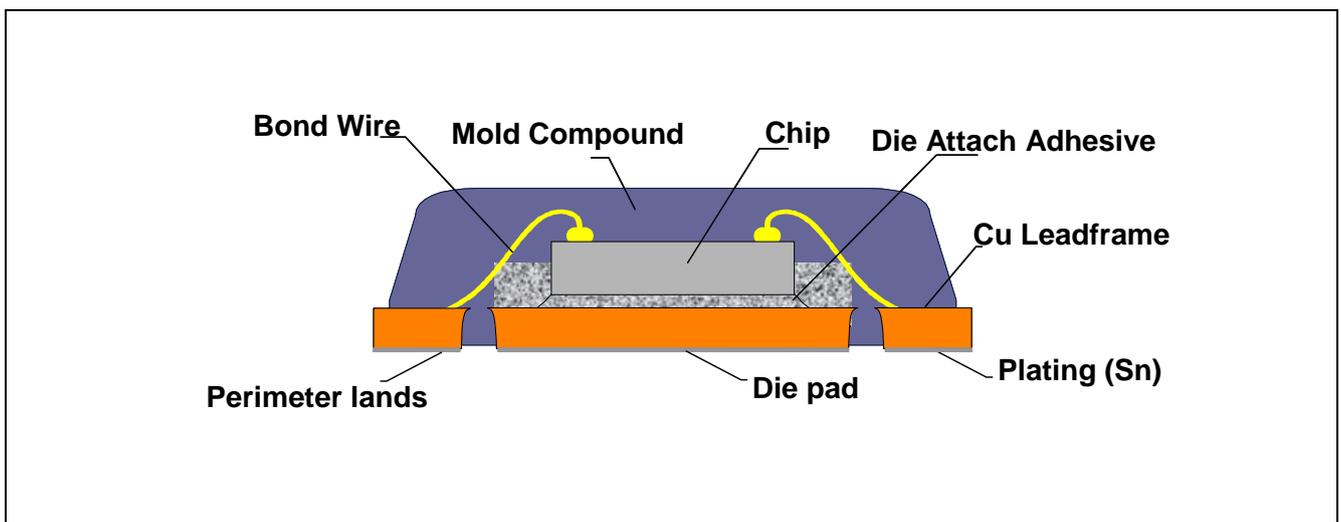


Figure 2 P(G)-VQFN punched type

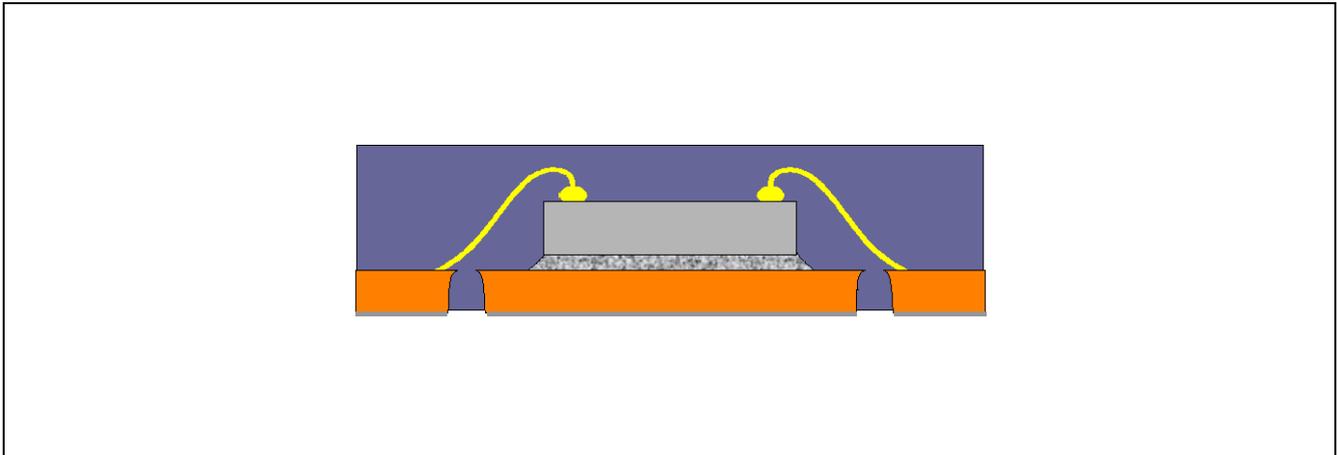


Figure 3 P(G)-VQFN sawn type

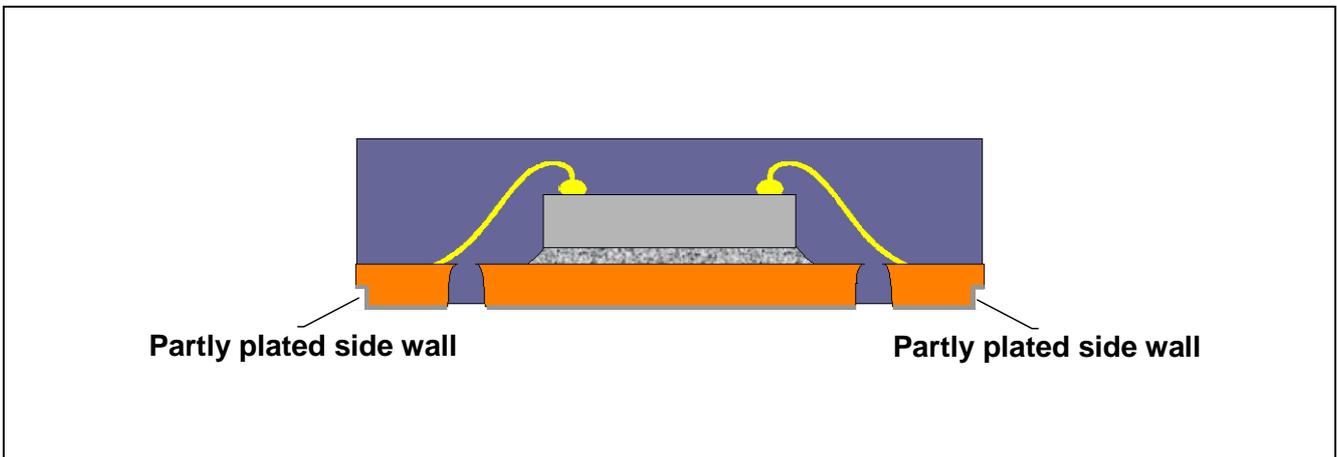


Figure 4 P(G)-VQFN sawn type with LTI feature

Semiconductor devices are sensitive to excessive electrostatic discharge, moisture, mechanical handling, and contamination. Therefore they require specific precautionary measures to ensure that they are not damaged during transport, storage, handling, and processing. For details, please refer to the General Recommendations for Assembly of Infineon Packages in “Package Handling” (available at www.infineon.com/packages).

2 Printed Circuit Board (PCB)

2.1 Routing

PCB design and construction are key factors for achieving solder joints with high reliability. Packages with exposed pads should not be placed opposite one another on either side of a PCB if double-sided mounting is used, because that will stiffen the assembled PCB and cause solder joints to fatigue earlier than in a design in which the components are offset. Furthermore, it is known that the board stiffness itself has a significant influence on the reliability (temperature cycling) of the solder joint interconnect if the system is used in critical temperature-cycling conditions.

2.2 PCB Pad Design

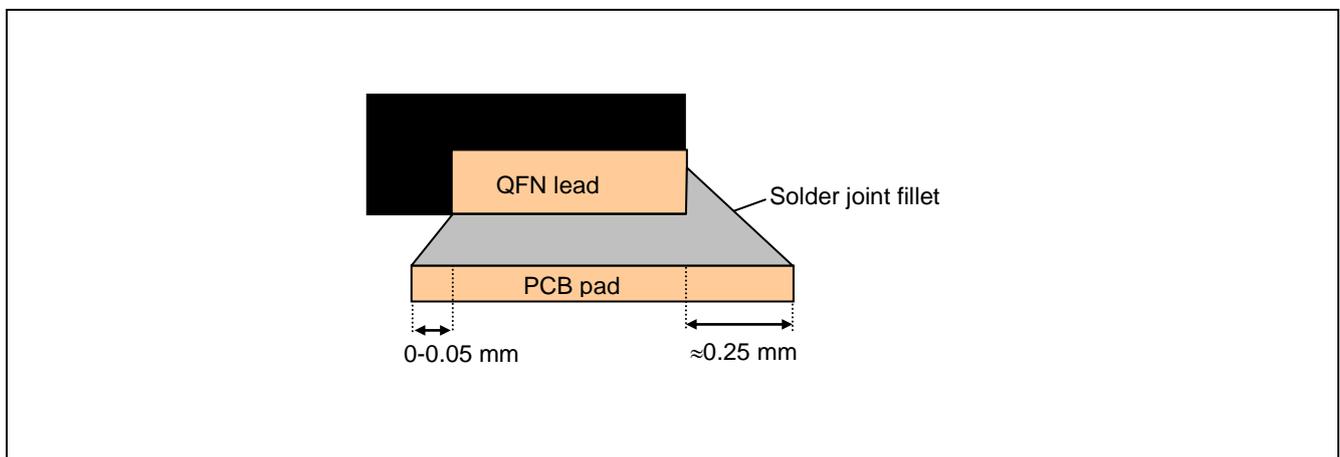


Figure 5 Schematic cross-section of a perimeter solder joint

Looking at a schematic cross-section of a solder joint through a perimeter land (Figure 5) we recommend extending the PCB pad by ≈ 0.25 mm compared to the package land in the direction of the package edge. We have also used this value to calculate the pad recommendations on www.infineon.com/packages. This extension of the PCB pad helps to develop a solder joint fillet at the side wall of the QFN land. However this cannot be guaranteed, as this area is not plated. Other influencing factors for fillet formation are package exposure to environment, solder paste material, and reflow process.

If a QFN package with an LTI feature is used, a solder joint fillet at the side wall of the QFN land is enabled, because an LTI feature provides a partly plated and therefore wettable side wall at the lead. If fillets are formed, this will be a benefit for solder joint reliability. When recommending detailed PCB pad values for the individual QFN packages, we have slightly extended the PCB pad by 0.05 mm towards the package center. For packages with low distance between QFN lands and thermal die pad, we have chosen the value 0 to avoid the risk of solder bridging.

We recommend 0.25 mm pad width for pitch 0.5 mm, and 0.35 mm pad width for pitch 0.65 mm.

The QFN packages have one or more central die pads. The surface plating is the same as for the outer package pads. In most applications, the die pads can transfer a large amount of heat into the PCB to improve thermal performance. Therefore the die pad should be soldered to the board onto the "thermal" pads. This also increases solder joint reliability, and improves electrical performance for

some applications/ products. We recommend using die pad sizes on the QFN packages as maximum “thermal” pad sizes on the PCB. Slightly smaller sizes of the “thermal” pads are also possible.

Below you can see schematic drawings of the PCB metal design for perimeter pads and the thermal pads (Figure 6 and Figure 7). Each package’s specific dimensions is available by following the links to P/PG-VQFN, P/PG-WQFN or P/PG-IQFN at www.infineon.com/packages.

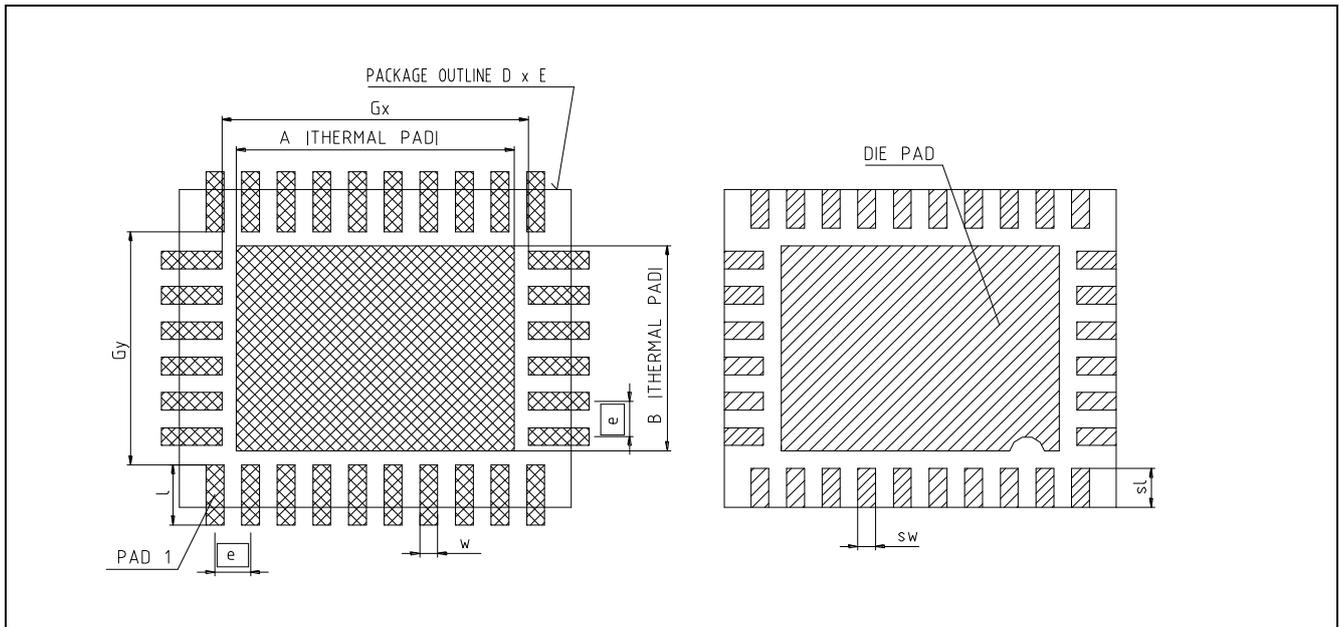


Figure 6 Schematic drawing of a VQFN PCB pad design recommendation (left side) and package bottom view (right side)

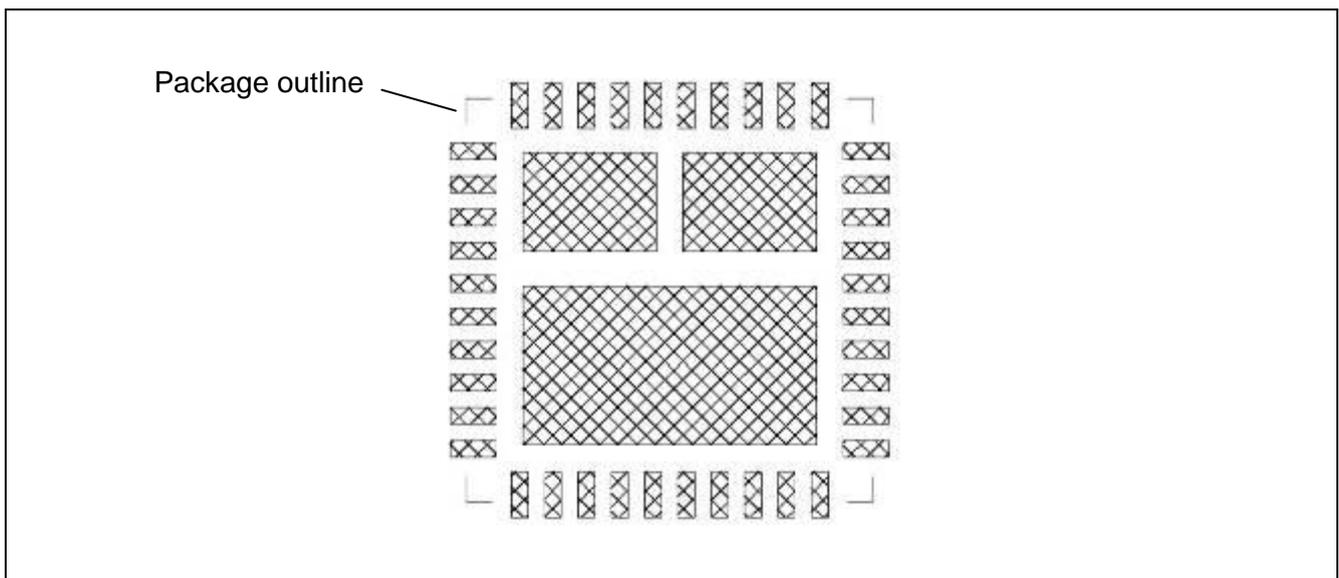


Figure 7 Schematic drawing of an IQFN PCB pad design recommendation

To connect the exposed die pad thermally and electrically directly to inner and/or bottom copper planes of the board, plated through-hole vias are used. They help to distribute the heat into the board

area. The heat spreads from the chip over the package die pad and the solder joint to the thermal pad on the board.

A typical hole diameter for such thermal vias is 0.2 - 0.4 mm. The diameter and the number of vias in the thermal pad depend on the thermal requirements of the end product, the power consumption of the product, the application, and the construction of the PCB. However, an array of thermal vias with pitch 1.0-1.2 mm can be a reasonable starting point for further optimization of most products/applications. Thermal and electrical analysis and/or testing are recommended to determine the minimum number of vias needed.

A good solder joint at the central die pad can be formed using vias that remain open on both sides of the board. However, there are two things to be considered. Open vias in the thermal pad will lead to a lower stand off between package and board. This is mostly controlled by the solder volume between the package die pad and thermal pad on the PCB. In addition, solder can protrude to the other side of the board, which may interfere with a second solder paste printing process on this opposite board side. To prevent solder beading, a wettable surface surrounding these vias on the opposite board side should be provided to act as a buffer for the surplus solder. It is also recommended to arrange the vias symmetrically in the thermal pad.

If necessary, vias can be closed by "tenting", which means the vias are covered with solder mask (e.g. dry-film solder mask). If the via tenting is done only on the opposite side of the board, the voiding rate will increase significantly. Combined with an intelligent solder mask layout for the thermal pad (segmentation of the thermal pad using solder mask bars), this method leads to good processability and balanced solder joints.

Another method to close vias is called "plugging" (filling with epoxy), followed by overplating. Very small vias (100 μm in diameter or smaller) should be filled with copper and overplated. In both cases the specification of a planar filling is necessary to avoid cavities, which will work as traps for gases, forming voids during reflow soldering.

If it is not necessary to have a direct connection from the solder pad under the exposed die pad to the inner layers of the PCB, the vias should be placed next to the footprint near the package and covered with solder mask.

3 Board Assembly

3.1 General Remarks

Many factors within the board assembly process influence assembly yield and board-level reliability. Examples include design and material of the stencil, the solder paste material, solder paste printing process, component placement, and reflow process. We want to emphasize that this document is just a guideline to support our customers in selection of the appropriate processes and materials. Additionally, optimization studies at the customer's own facilities that take into account the actual PCB, the customer's SMT equipment, and product-specific requirements may be necessary. Lead-free PG-VQFN, PG-WQFN or PG-IQFN packages with Sn plating can generally be assembled with either SnPb-based or lead-free SnAgCu-based solder paste and reflow processes, but it is important to determine whether the temperature profile used can form an adequate solder joint (formation of intermetallic compound between component plating and solder material).

3.2 Solder Stencil

The solder paste is applied onto the PCB metal pads by screen printing. The volume of the printed solder paste is determined by the stencil aperture and the stencil thickness. In most cases the thickness of a stencil has to be matched to the needs of all components on the PCB. For QFN packages of pitch up to 0.5 mm, it is recommended to use stencils 100-125 μm thick. For pitch 0.65 mm, a 150- μm stencil thickness is possible. If this does not meet the requirements of other packages on the same PCB, then a step-down stencil should be considered. To ensure a uniform and sufficiently high solder paste transfer to the PCB, laser-cut (mostly made from stainless steel) or electroformed stencils (nickel) are preferred. Rounding the corners of the apertures (radius $\sim 50\mu\text{m}$) can support good paste release.

The apertures for the perimeter solder joints should be of the same size as the metal pads on the PCB. The stencil in the thermal pad areas should be segmented into smaller, multiple openings (Figures 8 and 9). One large opening would result in excessive solder volume under the QFN die pad compared to the perimeter pads as well as significantly higher voiding rate and higher risk of solder balling.

In our tests we printed a total area of about 40-50% of the thermal pad with solder paste. With this procedure we achieved good results in board assembly yield and reliability. The resulting solder joint stand-off was typically in the range of 50-60 μm . The most appropriate way of segmenting depends on the number and location of vias (if present) and the solder resist layout on the thermal pad. In a regular thermal via matrix, the stencil openings should be arranged in areas between the vias. In our evaluations we typically have used opening sizes ranging from 0.4 mm^2 - 1.0 mm^2 , depending on via density and thermal pad size.

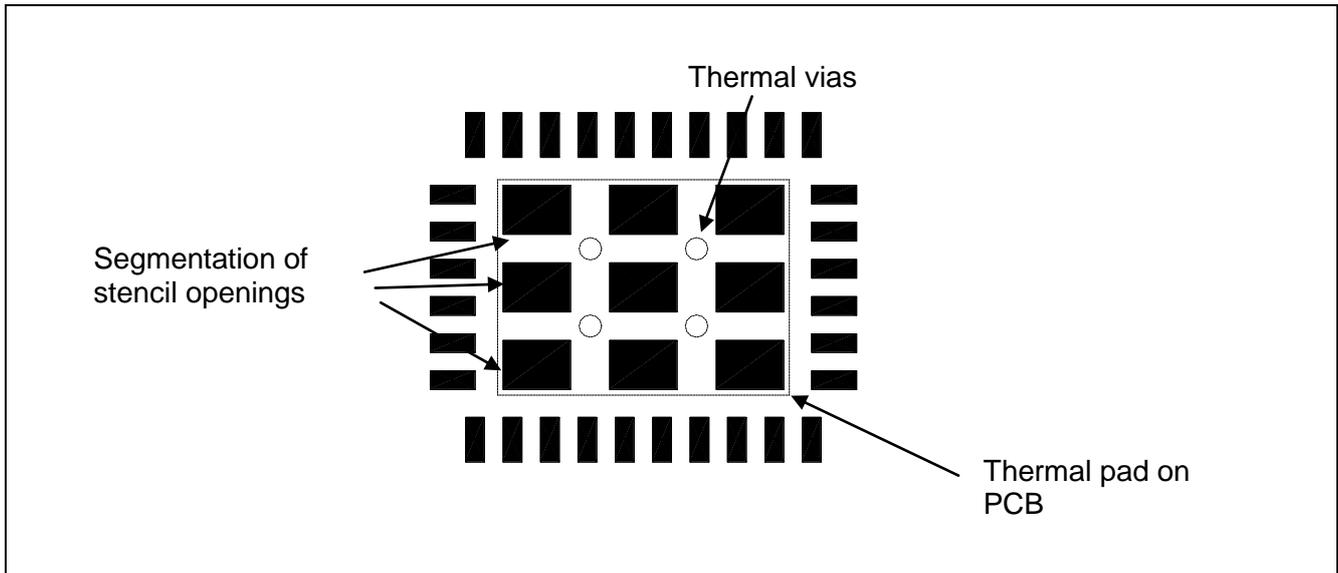


Figure 8 Example of segmentation of stencil openings on the thermal die pad area of a VQFN

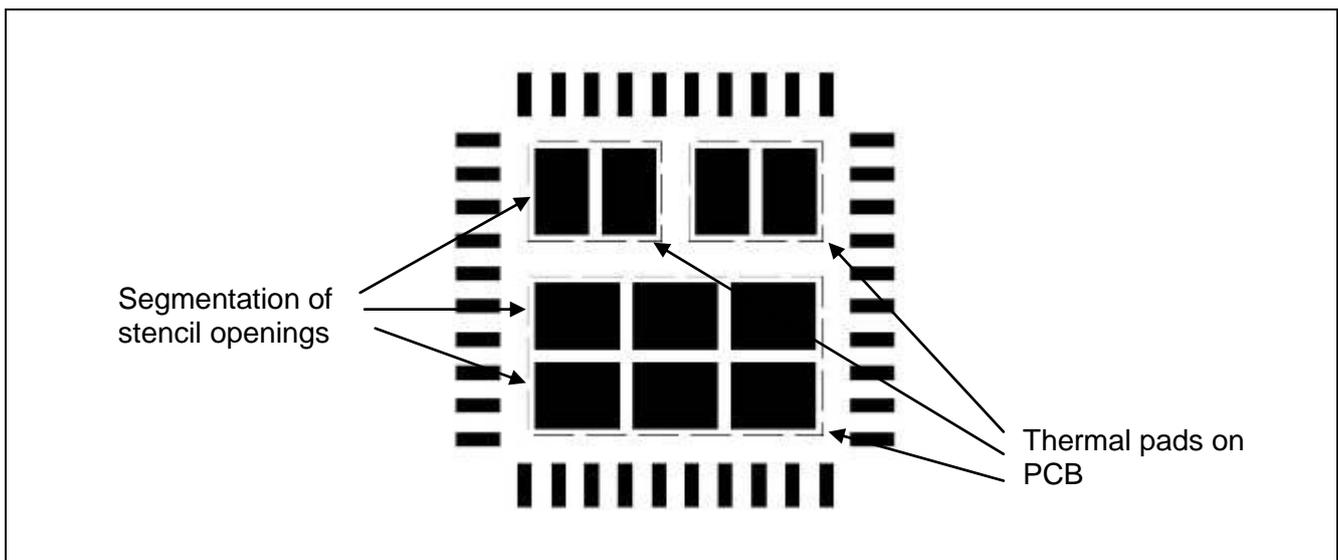


Figure 9 Example of segmentation of stencil openings on the thermal die pad areas of an IQFN

3.3 Solder Paste

Solder paste consists of solder alloy and a flux system. Normally the volume is about 50% alloy and 50% flux. In term of mass this means approximately 90 wt% alloy and 10 wt% flux. One of the functions of the flux system is to remove the contamination from the solder joints during the soldering process. The capability of removing contamination is given by the relative activation level. A lead-based solder paste metal alloy has to be of leaded eutectic or near-eutectic composition (SnPb or SnPbAg). A lead-free solder paste metal alloy composition (typically SnAgCu with Ag 3-4%, Cu 0.5-1%) can also be applied. A “no-clean” solder paste is preferred, because cleaning under the soldered QFN may be difficult. The paste must be suitable for printing the solder stencil aperture dimensions. The usage of paste type 3 or a higher type is recommended. Solder paste is sensitive to storage time, temperature, and humidity. Please follow the handling recommendations of the paste manufacturer.

3.4 Component Placement

VQFN, WQFN and IQFN packages have to be placed accurately depending on their geometry. Positioning the packages manually is not recommended.

Component placement accuracies of $\pm 50 \mu\text{m}$ are obtained with modern automatic component-placement machines using vision systems. With these systems both the PCB and the components are optically measured and the components are placed on the PCB at their programmed positions. The fiducials on the PCB are located either on the edge of the PCB for the entire PCB, or at additional individual mounting positions (local fiducials). They are detected by a vision system immediately before the mounting process. The packages are recognized by a special vision system, enabling the complete package to be centered correctly.

The maximum tolerable displacement of the components is 20% of the metal pad width on the PCB (for non-solder-mask defined pads). Consequently, for QFN packages the alignment of the device pad to the PCB pad has to be within $50 \mu\text{m}$ to assure a robust mounting process. Generally this is achievable with a wide range of placement systems.

The following remarks are important:

- Local fiducials close to the device can compensate for large PCB tolerances, especially on large boards.
- The lead-recognition capabilities should be used rather than the outline centering of the placement system.
- To ensure the identification of the packages by the vision system, adequate lighting as well as the correct choice of the measuring modes are necessary. The right settings should be available in the equipment manuals.
- Too much placement force can squeeze out solder paste and cause solder joint shorts. On the other hand, not enough placement force can lead to insufficient contact between package and solder paste, and this can lead to open solder joints or badly centered packages.

3.5 Soldering

Soldering determines the yield and quality of assembly fabrication to a very large extent. Generally all typical temperature profiles and standard reflow soldering processes are suitable for board assembly of a QFN, including:

- Forced convection
- Vapor phase
- Infrared (with restrictions)

Wave soldering is not possible. During the reflow process, each solder joint has to be exposed to temperatures above the melting point of the solder alloy for a sufficient time to get the optimum solder joint quality, whereas overheating the PCB with its components has to be avoided. Please refer to the bar code label on the packing for the peak package body temperature. It is important that the maximum temperature of the QFN package during the reflow does not exceed the specified peak temperature on the moisture level caution label on the packing of the devices (please also refer to the General Recommendations for Board Assembly, available at www.infineon.com/packages). When using infrared ovens without convection, special care may be necessary to assure a sufficiently homogeneous temperature profile for all solder joints on the PCB, especially on large, complex boards with different thermal masses of the components, including those under the QFN. The most

highly recommended type is forced-convection reflow. Nitrogen atmosphere can generally improve solder joint quality, but is normally not necessary for soldering tin-lead metal alloys. For the lead-free process with higher reflow temperatures, nitrogen atmosphere may reduce oxidation and improve the solder joint quality.

The temperature profile of a reflow process is one of the most important factors of the soldering process. It is divided into several phases, each with a special function. Figure 10 shows a general forced-convection reflow profile for soldering QFN packages. Table 1 is an example of the key data of such a solder profile that can be used for lead-free alloys. The single parameters are influenced by various factors, not only by the package. First and foremost, it is essential to follow the solder paste manufacturer's application notes. Additionally, most PCBs contain more than one package type and therefore the reflow profile has to be matched to all components' and materials' demands. We recommend measuring the solder joints' temperatures by thermocouples beneath the various packages. Take into account the fact that components with large thermal masses do not heat up at the same speed as lightweight components. The position and the surrounding of the package on the PCB, as well as the PCB thickness, can influence the solder joint temperature significantly. Maximum temperatures for the QFN package must not exceed MSL specifications.

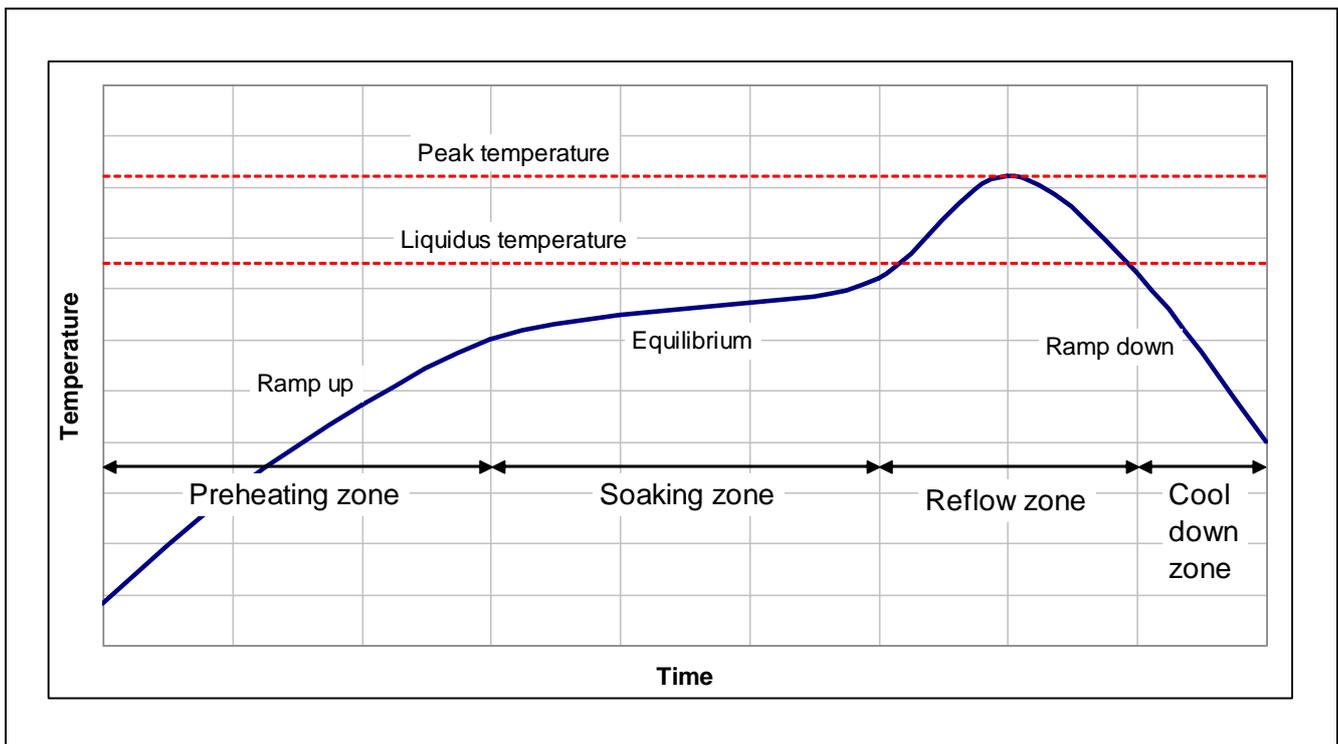


Figure 10 General forced-convection reflow solder profile

The following table is an example, not a recommendation.

Table 1 EXAMPLE of the key data for a forced-convection reflow solder profile

parameter	minimum value	typical value	max. value (acc. IPC/ JEDEC J-STD-020)	main influence
preheating rate	1.0 K/s	2.5 K/s	3.0 K/s	flux system (solder paste)
soaking temperature	140 – 170°C	140 – 170°C	150 – 200°C	flux system (solder paste)
soaking time	50 s	80 s	120 s	flux system (solder paste)
peak temperature	230°C	245°C	260°C	alloy (solder paste)
reflow time above melting point (liquidus)	40 s	60 s	150 s	alloy (solder paste)
cool-down rate	1.0 K/s	2.5 K/s	8.0 K/s	

3.6 Double-sided Assembly

VQFN, WQFN and IQFN packages are generally suitable for mounting on double-sided PCBs. That means board assembly including soldering is first done on one side of the PCB. Afterwards the second side of the PCB is assembled.

3.7 Cleaning

After the reflow soldering process, some flux residues can be found around the solder joints. If a “no-clean” solder paste has been used for solder paste printing, the flux residues usually do not have to be removed after the soldering process. Cleaning beneath a QFN package is difficult because of the small gap between package and PCB, and is therefore not recommended. However, if the solder joints have to be cleaned, the cleaning method (e.g. ultrasonic, spray or vapor cleaning) and solution have to be selected while taking into account the kinds of packages to be cleaned, the flux used in the solder paste (rosin-based, water-soluble, etc.), and environmental and safety aspects. Removing/drying of even small residues of the cleaning solution should also be done very thoroughly. Contact the solder paste manufacturer for recommended cleaning solutions.

3.8 Inspection

A visual inspection of the solder joints with conventional Automatic Optical Inspection (AOI) systems is limited to the outer surface of the solder joints. Since the non-wetting of the package lead side walls is not a rejection criterion, the usefulness of an optical inspection is questionable.

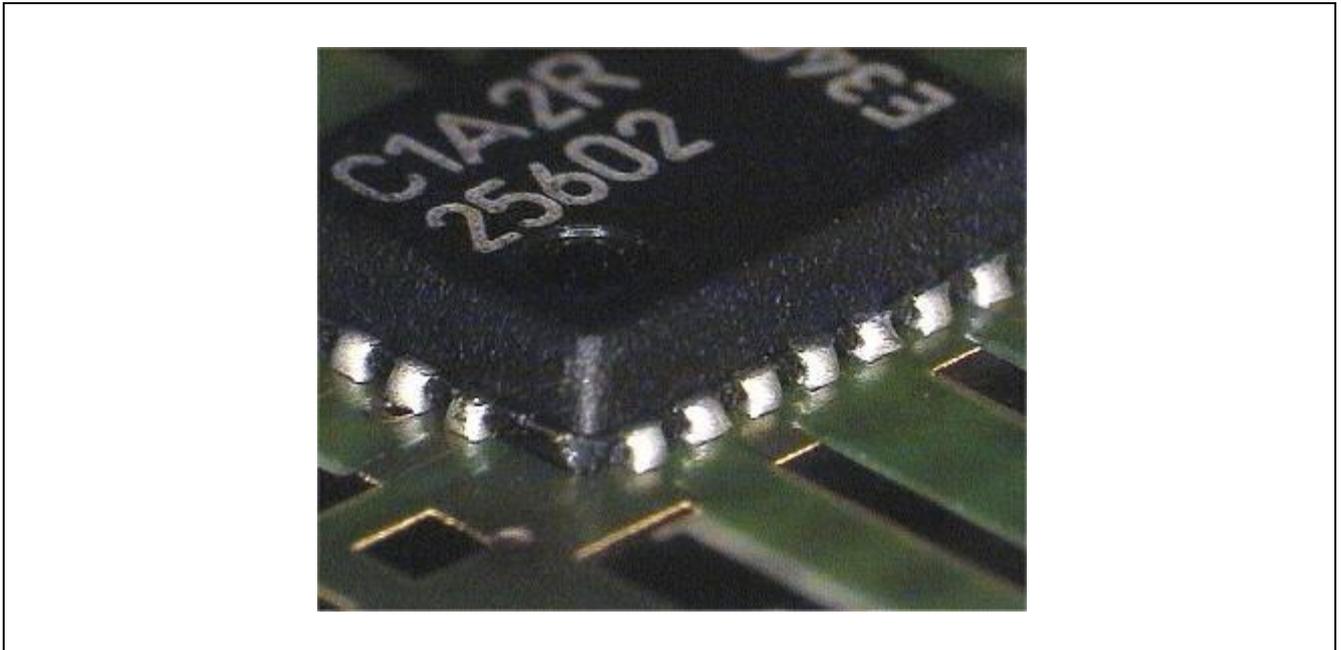


Figure 11 Overview of a soldered VQFN package

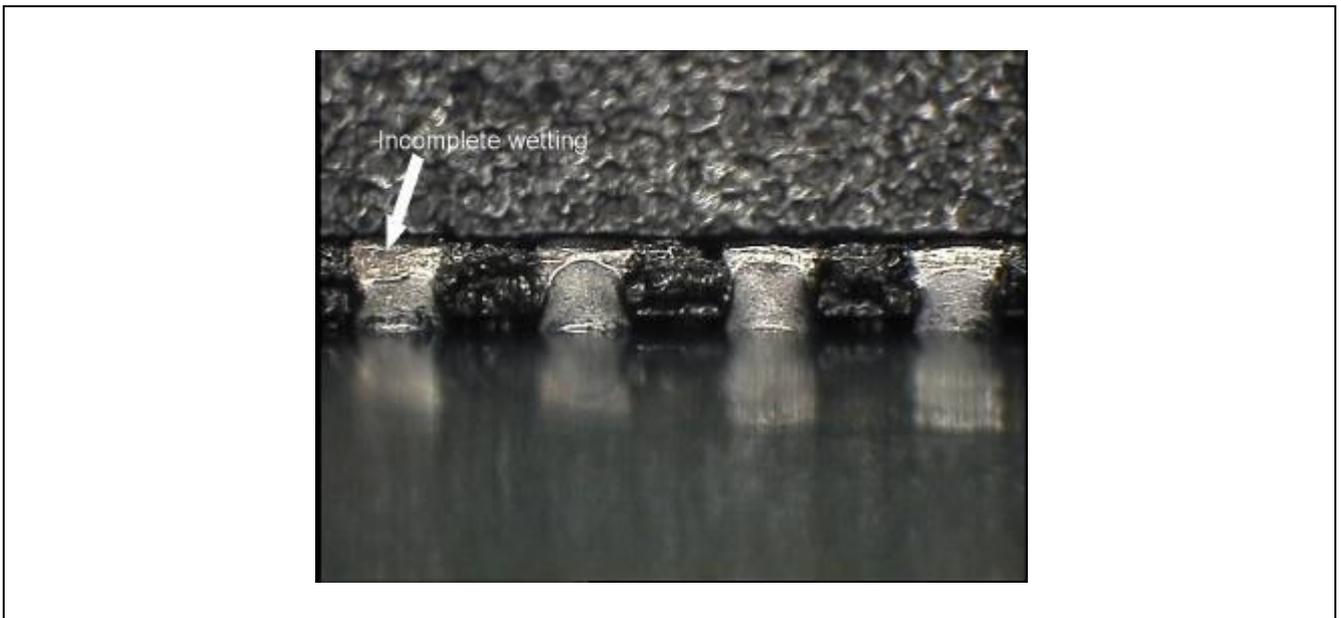


Figure 12 Non-wetting of the lead side wall is not a criterion for rejection

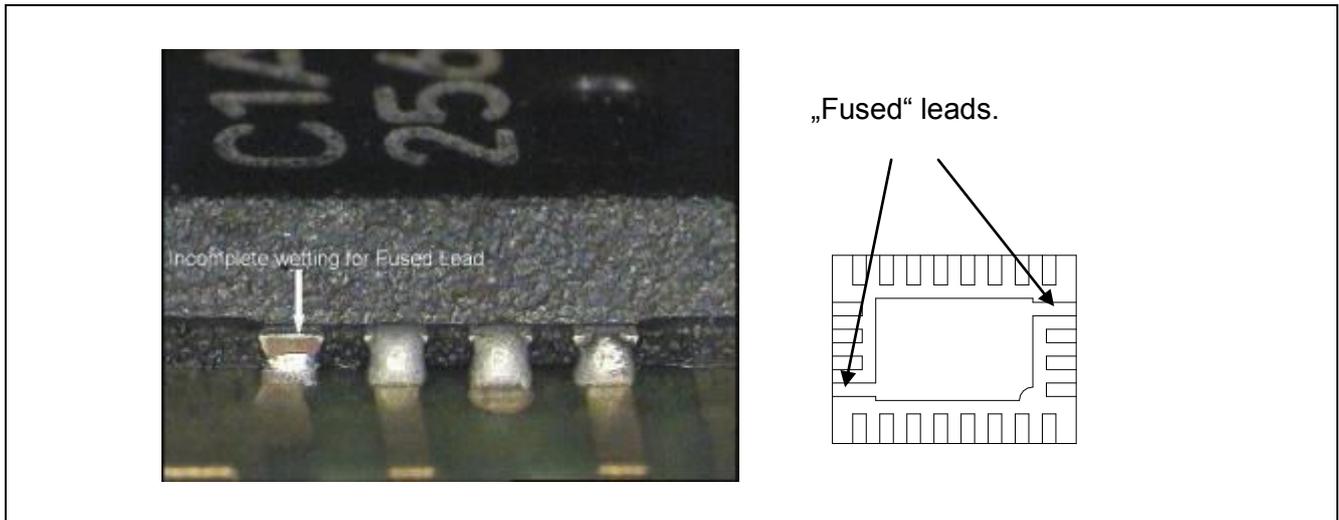


Figure 13 “Fused” leads can also show incomplete wetting of the lead side walls. This is also not a rejection criterion. Fused leads denote QFN lands, which are directly connected to the die pad via the leadframe.

The only reasonably efficient method for inline control of this process is the implementation of Automatic X-ray Inspection (AXI) systems. AXI systems are available as 2D and 3D solutions. They usually consist of an X-ray camera and the hardware and software needed for inspection, controlling, analyzing, and data transfer routines. These systems reliably detect soldering defects such as poor soldering, bridging, voiding, and missing parts. For the acceptability of electronic assemblies, please refer to the IPC-A-610C standard.

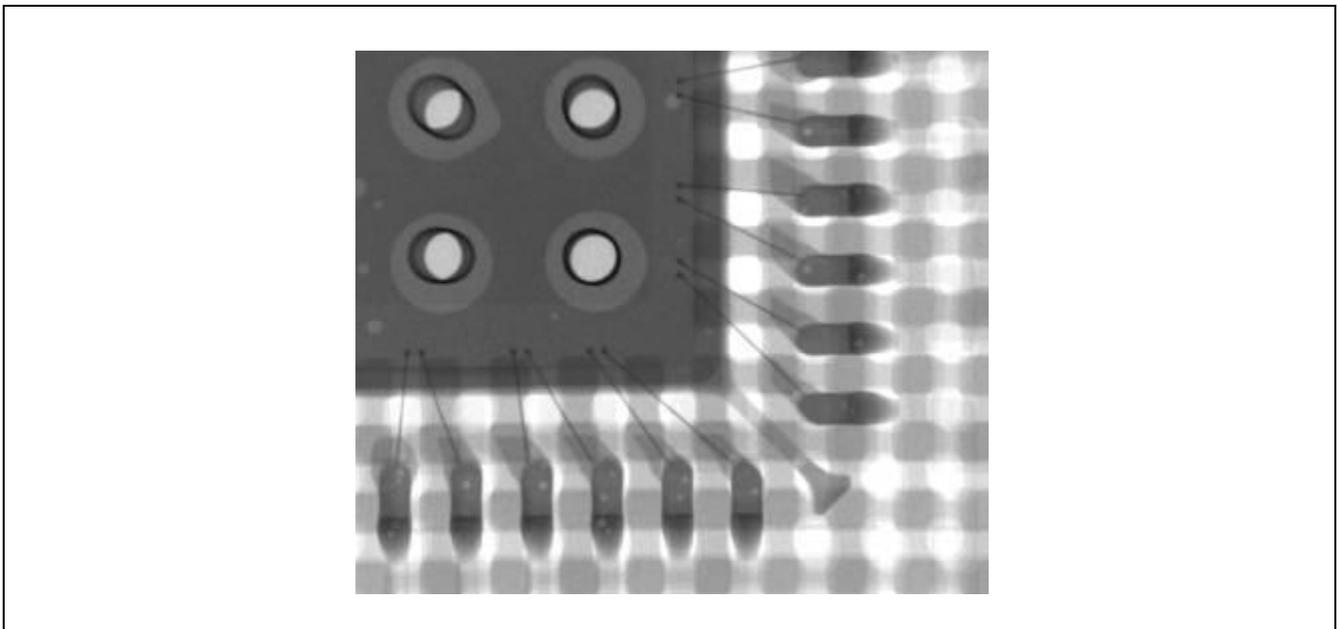


Figure 14 Typical X-ray image of soldered VQFN package. Investigations have shown that voids in size and amount as shown in this image do not reduce reliability.

Cross-sectioning of a soldered package as well as dye-penetrant analysis can serve as tools for sample monitoring only, because of their destructive character.

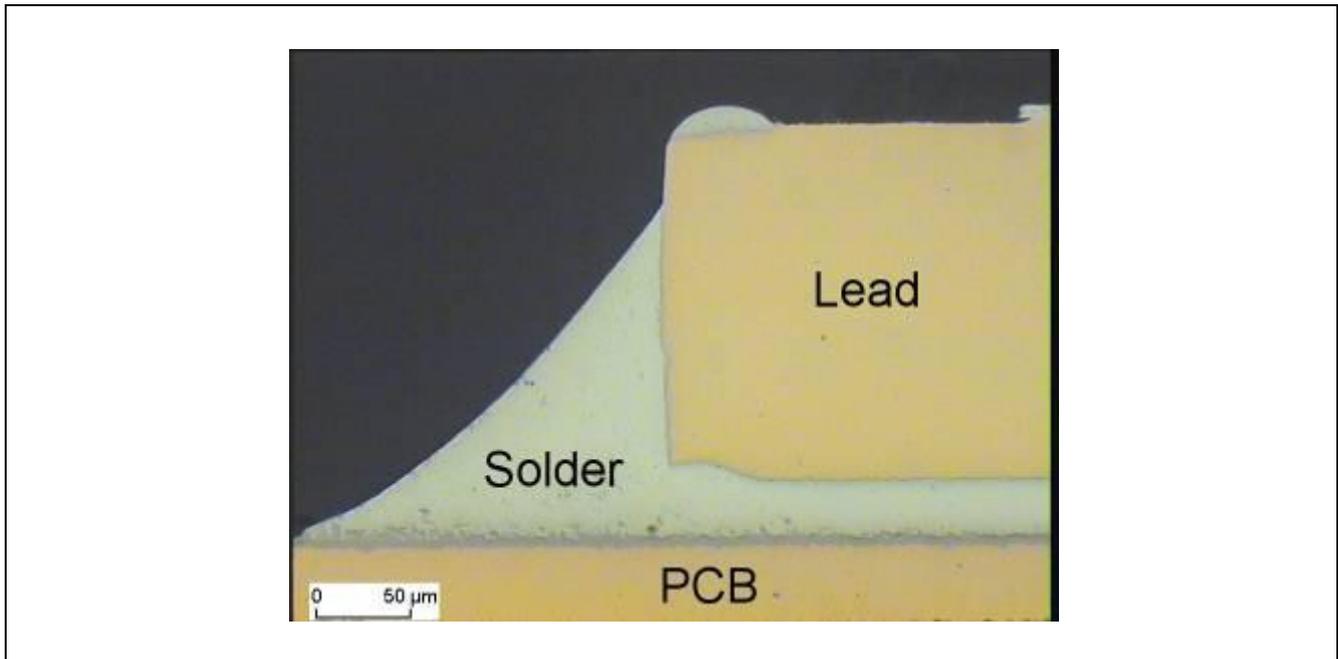


Figure 15 Cross-section of a QFN solder joint

If a package is equipped with an LTI feature, a wetting of the lead side wall is possible because an LTI feature provides a partly plated lead side wall.

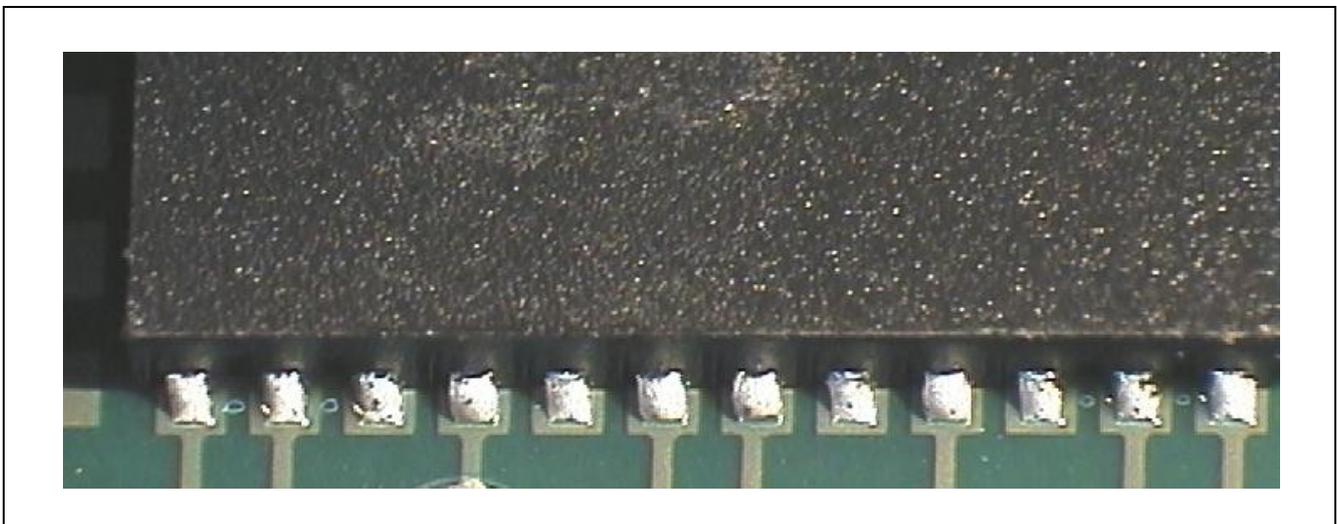


Figure 16 VQFN with LTI feature – wetted lead side wall

Special notes for lead-free solder joints:

Lead-free solder joints look different from tin-lead (SnPb) solder joints. Tin-lead joints typically have a bright and shiny surface. Lead-free (SnAgCu) solder joints typically do not have this bright surface. Lead-free solder joints are often dull and grainy. These surface properties are caused by the irregular solidification of the solder, as these solder alloys are not exactly eutectic (like the 63Sn37Pb solder alloy). This means that SnAgCu solders do not have a melting point but a melting range of several degrees. Although lead-free solder joints have this dull surface, they are not of lower reliability than SnPb joints. It is therefore necessary to teach the inspection staff what these new lead-free joints look like, and/or to adjust optical inspection systems to handle lead-free solder joints.

4 Rework

If a defective component is detected after board assembly, the device can be removed and replaced by a new one. Due to possible damage while removing the component, a desoldered component should not be reused. Nevertheless, desoldering the old component (if analysis afterwards is planned) and resoldering of the new component has to be done very carefully. Repair of single solder joints is not possible.

4.1 Tooling

The rework process is commonly done on special rework equipment. There are a lot of systems available on the market, and for processing these packages the equipment should fulfill the following requirements:

Heating: Hot air heat transfer to the package and PCB is strongly recommended. Temperature and air flow for heating the device should be controlled. With freely programmable temperature profiles (e.g. by PC controller), it is possible to adapt the profiles to different package sizes and thermal masses. PCB preheating from the underside is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but infrared heating should be used only for augmenting the hot air flow from the upper side. Nitrogen can be used instead of air.

Vision system: The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of package to PCB, a split optic should be used. Microscope magnification and resolution should be appropriate for the pitch of the device.

Moving and additional tools: The device should be relocatable on the whole PCB area. Placement accuracy better than $\pm 50 \mu\text{m}$ is recommended. The system should have the capability of removing solder residues from PCB pads (special vacuum tools).

4.2 Device Removal

If a defective component is going to be sent back to the supplier, no further defects must be introduced to the device during its removal from the PCB, because this may hinder the supplier's failure analysis. The following recommendations should be followed:

Moisture: Depending on its MSL, the package may have to be dried before removal. If the maximum storage time out of the dry pack (see label on packing material) is exceeded after board assembly, the PCB has to be dried according to the recommendations; otherwise too much moisture may have been accumulated and damage may occur (popcorn effect). Please also refer to the standard J-STD-033.

Temperature profile: During the soldering process, it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (Section 3.5).

Mechanics: Be careful not to apply high mechanical forces during package removal. Otherwise, failure analysis of the package can be impossible, and/or the PCB can be damaged. For large packages, pipettes (vacuum nozzles) can be used. Pipettes are implemented on most rework systems.

4.3 Site Redressing

After removing the component, the pads on the PCB have to be cleaned of solder residues. Don't use steel brushes because steel residues can lead to bad solder joints.

Before placing a new component on the PCB, solder paste should be applied to each PCB pad by printing (special micro stencil) or dispensing. No-clean solder paste is recommended.

Using only flux without applying additional solder is not recommended because the resulting solder joints will be thinner and their reliability will differ from that of a standard PCB assembly.

If a desoldered component has to be resoldered, the component has to be cleaned and old solder and flux have to be removed first. This has to be done with special care so that the package is not harmed by mechanical or thermal stress, or by material such as flux, solder, and cleaning solvents that may penetrate into the package through the optical window and/or vent holes.

4.4 Reassembly and Reflow

After preparing the site, the package can be placed onto the PCB. The maximum applied pick&place force should not exceed the force applied during standard board assembly.

It is also possible to position the package exactly above the PCB pads, at a height just above the pads so that there is no contact between the package and the PCB. The package is then dropped into the printed or dispensed solder paste depot (zero-force placement).

During the soldering process, it should be assured that the package peak temperature is not higher and temperature ramps are not steeper than for the standard assembly reflow process (Section 3.5). Investigation has shown that if distance, time, and airflow are properly controlled, a hot air temperature of 300°C can be used, for example, without violating the maximum allowed reflow profile.

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