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TID RLAT Variables Report for Cypress 72Mb QDR SRAMs (CYRS1543AV18)

Date: 20 Dec 2011 Revision: A

Prepared By: _____ 20 Dec 2011
JD Instruments Date

Executive Summary

Radiation Lot Acceptance Testing (RLAT) is performed on a continuing basis to insure parts meet required radiation hardness levels. RLAT is performed using Total Ionizing Dose (TID) as the sole type of radiation in accordance with Cypress Semiconductor's Rad Hard Quality Management specification.

MilStd 883, Method 1019 (TM1019) states that RLAT must be performed on parts that have been fully screened and burned-in unless it has been shown that there is no difference in radiation response between burned-in and non-burned-in parts. It further states that all spec sheet parameters must be measured unless certain parameters have been shown to be unaffected by radiation.

This report will address these issues to demonstrate that it is not necessary to use fully burned-in parts for RLAT TID testing. It will also show that it is not necessary to measure most AC parameters as part of the RLAT test suite. Technology characterization data (TCV) will also be presented to show that the process is inherently radiation tolerant to at least 2X the guaranteed TID level.

AC Testing - Because of their high frequency of operation CYRS1543AV18 QDR SRAMs present unique measurement problems for RLAT. Many AC parameters (e.g. data set-up and hold) have limits of only +/- 0.5nS at 250MHz clock frequency and these are difficult to measure "on-site" at a radiation facility. These parameters can be only be measured at facilities remote from the radiation source where it would not be possible to return the parts to radiation within the 2 hour time limit imposed by TM1019.

We irradiated units from 3 Fab lots and followed TM1019 dry ice procedure to evaluate the pre/post radiation performance of all AC parameters listed in the SMD. AC testing was carried out for pre/post radiation samples at Cypress Semiconductor's production test floor utilizing an Advantest T5592 production grade tester.

Most AC parameters showed no detectable change with radiation. Parameters such as Tsd (Data Setup to Clock Rise) involve only a small portion of circuitry that is peripheral to most of the chip. I/O circuitry generally uses larger geometry devices that are much faster than internal circuitry and logic paths are short.

The only AC parameter that showed any change with radiation was the maximum operating frequency with no errors ("Fmax" or inversely "Tcyc"). Write/Read operations involve long logic chains and analog type functions (e.g. sense amps). These parts operate with a latency of 2 clock cycles so the actual Write/Read operations are isolated from I/O timing.

Fmax/Tcyc can be determined on-site at the radiation source by varying the clock frequency of the DUT. Future production RLAT testing will include functional tests at 300MHz (spec limit is 250MHz). If the parts pass at this frequency then they will be considered acceptable. If they fail at 300MHz but pass at 250MHz then their Fmax/Tcyc will be determined by varying the test frequency. Tcyc will be tracked vs. radiation and one-sided tolerance limit statistics will be used for lot acceptance.

AC testing of other parameters will not be part of the ongoing production RLAT testing procedure.

Burn-In vs. Non-Burn-In Parts - Test results and analysis presented in this report will show that there is no difference in radiation response between burned-in and non-burned-in parts so non-burned-in parts will be used for future RLAT testing.

Technology Characterization Vehicle (TCV) - A complete set of DC and functional AC tests were performed up to 2X the specified TID limit. All parameters for these parts were well within limits hence meeting the RHACL specified in Appendix C of MIL-STD 38535.

1.0 PART DESCRIPTION

CYRS1543AV18 devices have the architecture shown in Figure 1. Internally read and write operations are 72 bits wide. Control logic and latches convert the internal memory architecture to the "X18" architecture seen externally.

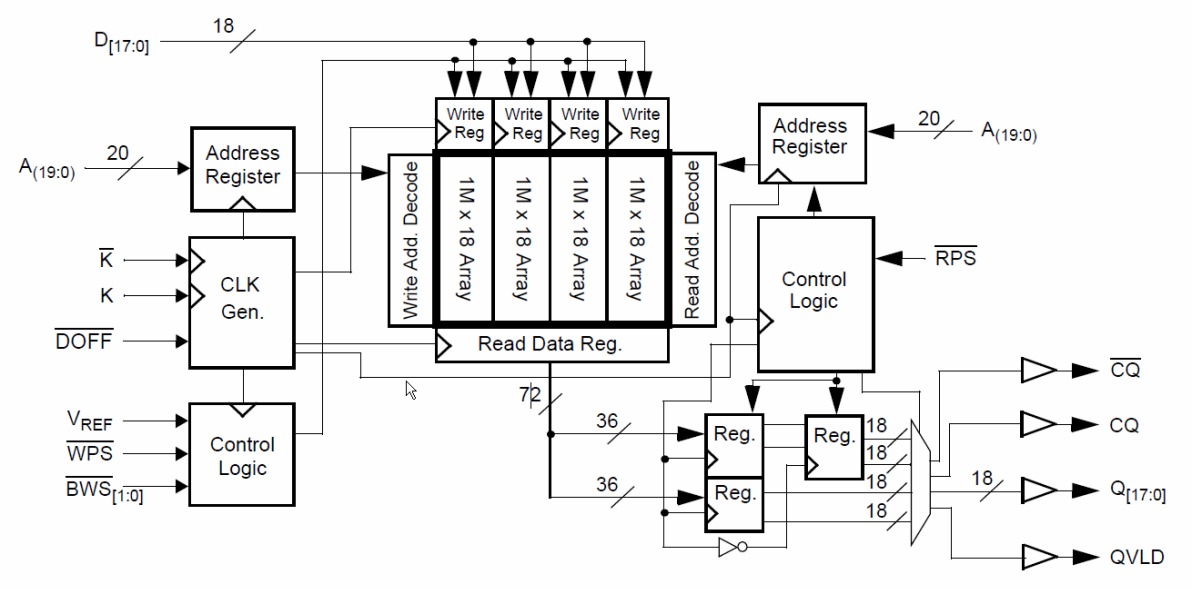


Figure 1. Functional Diagram for CYRS1543AV18

Devices were provided in 165 position CGA packages ball FBGA packages. These were inserted into sockets for bias and test. A picture of an open socket is shown in Figure 2 alongside a test device that is flipped over to show the column grid pattern on its bottom surface.

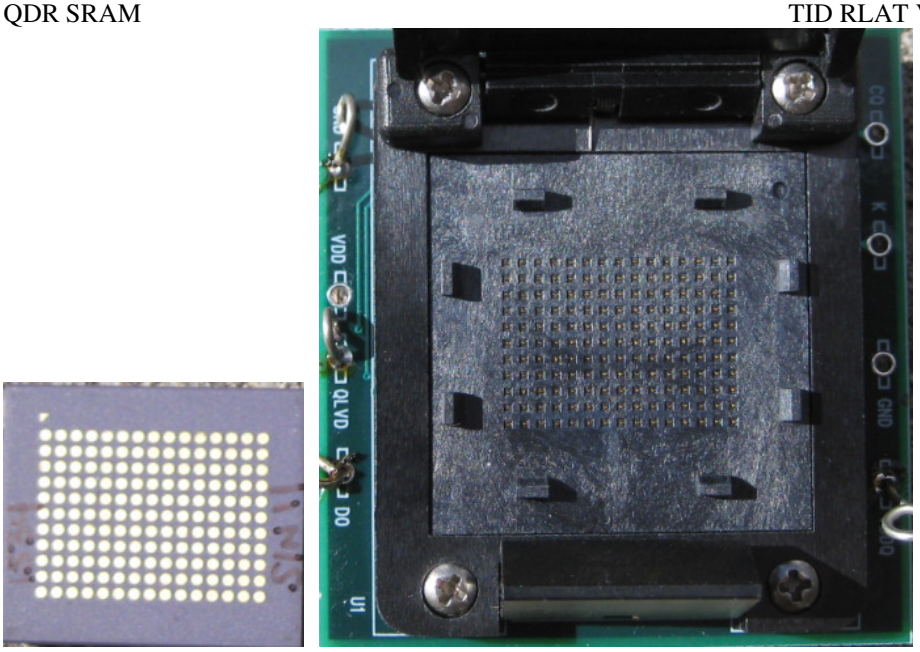


Figure 2. Bottom Surface of DUT and Open Socket

Four devices were mounted to each bias board prior to being exposed to radiation. These devices were arranged in a 2 X 2 matrix to minimize dose rate variation across the pattern. Figure 3 shows this pattern along with measured dose rates. Dose rates were measured using a calibrated meter as detailed in Attachment A. Measurements indicated less than +/-1% variation in dose rate across the exposure pattern.

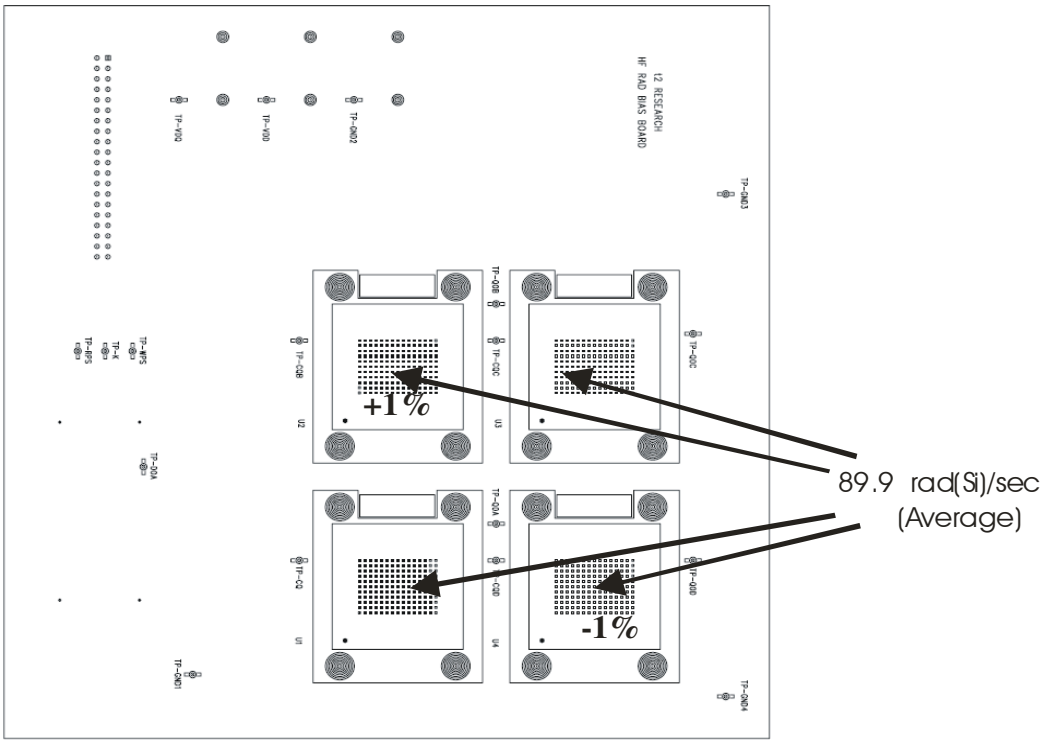


Figure 3. DUT Pattern and Dose Rate

Each DUT board was connected to a “stimulus board” as shown in figure 4. This board provided the high frequency clock for the 4 devices on the DUT board and wrote a checkerboard pattern into the parts during radiation. Each 2 board set was placed in a lead-aluminum box during radiation as shown in figure 5.

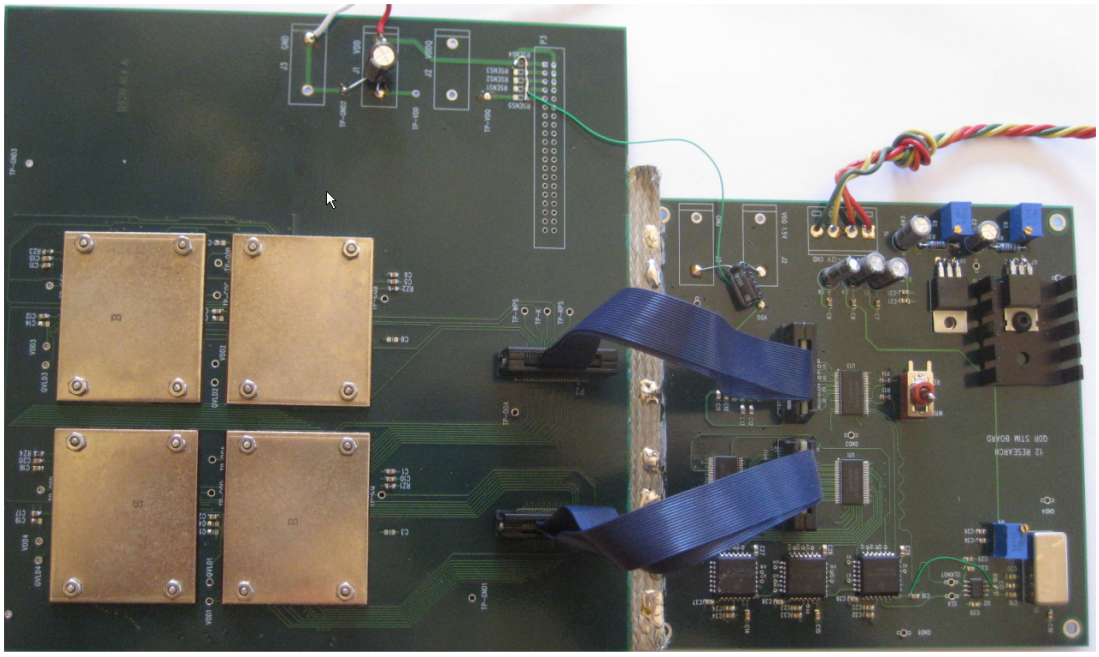


Figure 4. DUT Board/Stimulus Board Combination

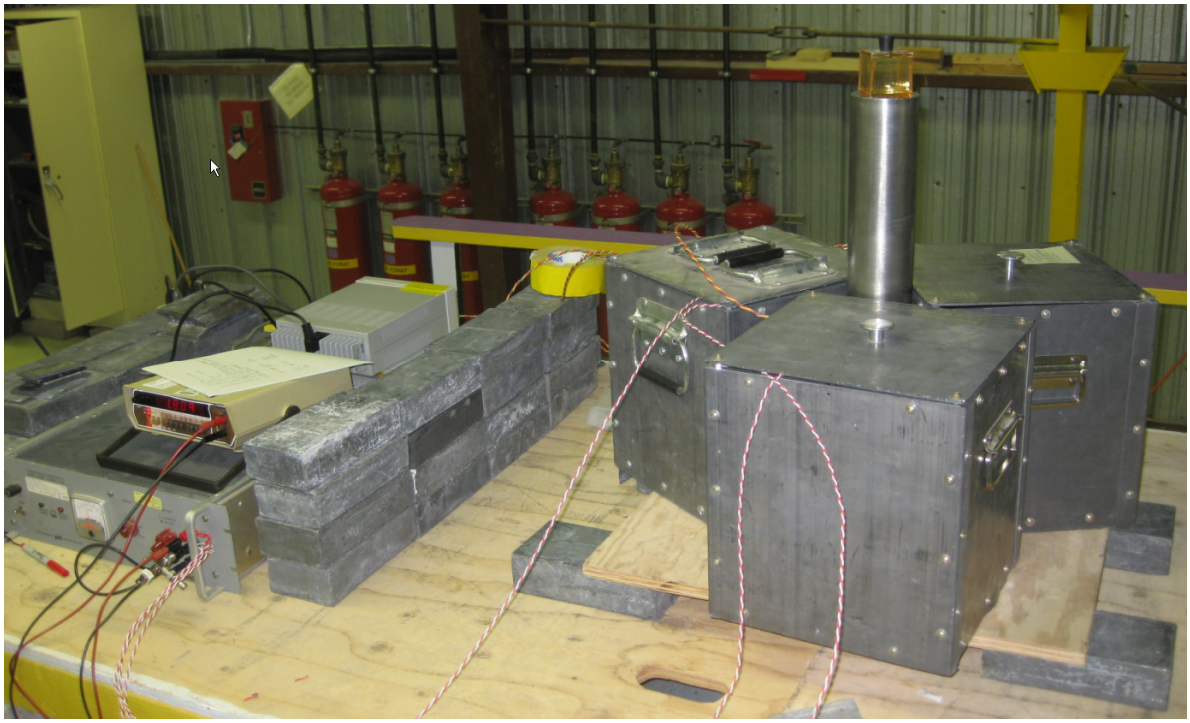


Figure 4. DUTs Being Irradiated

Tests were performed using an Algorithmic Test Vector (ATV) system from JD Instruments as shown in figure 6. This is a portable system containing many of the features found in larger main-frame test systems. For this application it is particularly useful in that it collects data in both primitive error logs and also records summary results in spreadsheet form, simplifying on-site understanding of results as the test proceeds.

Figure 6. ATV Test System used for SEE Testing

All irradiations and tests were performed on these parts while they are operating at their maximum clock frequency of 250MHz with a constant checkerboard pattern. Thus, the SRAM portion of the device was in a static condition even through the rest of the device was operating at it's maximum frequency.

Irradiations were performed with the devices biased to their maximum supply voltages (Vdd = Vddq = 1.9V). Later testing was performed with devices biased to their nominal voltages (Vdd =1.8V, Vddq = 1.5V). This was considered the worst case combination of bias conditions since more radiation damage will be induced at a higher bias and AC performance (e.g. race conditions) are worse at lower biases.

In order to achieve a 250MHz operating frequency a special test board was designed that contains an FPGA to provide the high speed interface to the DUT. The ATV system provided the patterns to be written to the DUT and the FPGA performed the actual write operation. Similarly, ATV initiated a read operation by issuing a command to the FPGA. The FPGA then read a burst of 4 memory locations from the DUT and passed the information to the ATV at a slower speed.

All tests were performed at room temperature which was ~21^0C (70^0F). Testing was begun within ~5 minutes following the end of each radiation step. All testing was completed and parts were again under irradiation within ~½ hour. This irradiate/test sequence insured that any parameters exhibiting "rapid" room temperature annealing would be measured at their worst (most extreme) levels.

RLAT electrical test conditions are presented in Appendix A. Bias conditions used during irradiation are presented in Appendix B. Pictures of the test board are shown in Appendix C.

2.0 Functional Tests and Measured Parameters

Three types of tests were performed for this report: DC Parametric, Functional and AC parametric. Testing was divided between on-site tests at the radiation source (RLAT tests) and testing at the manufacturing facility (AC Characterization tests). Specific sets of tests are given below.

2.1 RLAT Tests

DC Parametric tests included all DC parameters listed in subgroup 1 of SMD 5962-11201. Specifically these included: Voh, Vol, Voh(low), Vol(low), Vih, Vil, Ix, Ioz, Idd and Isb. Vref was verified by varying the Vref input and performing functional tests. Idd and Isb were measured using 5 memory patterns which included CB, CB*, All 1's, All 0's and D=A.

Functional tests included writing/reading CB and CB* patterns to the part (CB/CB*) as well as writing/reading a pattern where the memory contents at each address equaled the lower 18 address bits (D=A).

AC Parametric tests included running the DUT at full speed (250MHz) and verifying its operation. This verified that the part met it's Tcyc (Fmax) parameter.

2.2 AC Characterization Tests

AC characterization tests were performed using the 4 functional algorithms specified in SMD 5962-11201, Appendix A. Specifically these were: CB/CB*, March, XY March and CEDES. Each algorithm was performed while measuring AC parameters so a set of measurements was collected for each parameter at every DUT/radiation condition.

AC tests included all standard manufacturing parameters. These are listed in table 1. Some parameters are measured relative to several inputs or conditions. Thus, for instance, Tsc is measured relative to the RPS, WPS and BWS pins. In the table these pins/conditions are shown in parentheses.

Parameter	Description
Tcyc	K Clock Cycle Time
Tkhkh	K Clock Rise to K* Clock Rise
Tas	Address Setup to K Clock Rise
Tsc (_Rps#, _Wps#, _Bws#)	Control Setup to K Clock Rise
Tds (_ /1 /2)	Data Setup to Clock Rise
Tah (_/1)	Address Hold after K Clock Rise
Thc(_Rps#, _Wps#, _Bws#)	Control Hold after K Clock Rise
Tdh (_ /1 /2)	Data Hold after Clock Rise
Tco (1 /2)	Clock Rise to Data Valid
Tdoh (1 /2)	Data Output Hold after Clock Rise
Tccqo (1 /2)	K/K* Clock Rise to Echo Clock Valid

Table 1. Standard Manufacturing AC Measurements

3.0 AC Parametric Measurements vs. Radiation

Parts from 3 Fab lots were irradiated and transported back to Cypress Semiconductor using the TM1019 dry ice procedure. Pre/post radiation measurements were made of all AC parameters listed in the SMD. AC testing was carried out pre-radiation and again after the devices were irradiated to 300K rad(Si). DC parameters and AC functionality were measured on-site during irradiation using the same test programs, fixtures and procedures that are used for RLAT testing.

Table 2 shows the parts that were used for this test.

Fab Lot	S.N.
L4046805	1
"	2
"	3
L4034627A	10
"	11
"	12
L4034627	19
"	20
"	21

Table 2. Parts Used for AC Testing

Typical results of the AC characterization are shown in figure 7, a plot of Tsd (Data Setup to Clock Rise) before and after radiation.

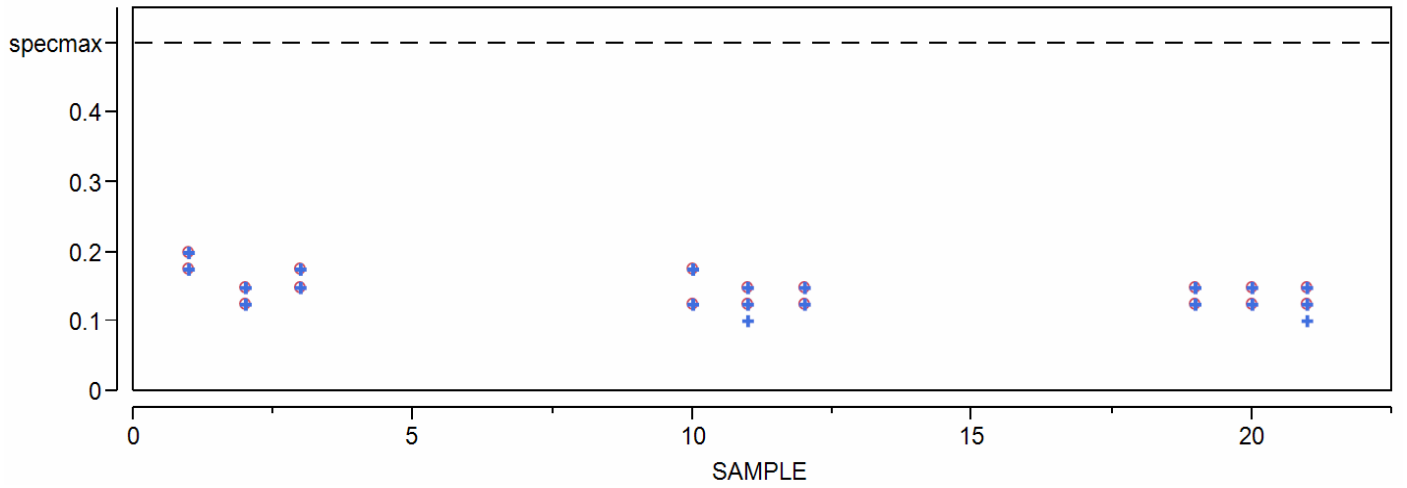


Figure 7. Tsd Before Radiation (Pink Circles) and After 300K rad(Si) (Blue Crosses)

Note in this figure that the horizontal axis is the serial number of the DUT and the vertical axis is the measured setup time. Pre-radiation measurements are shown as pink circles and post-radiation are shown as blue crosses. Several test patterns were used for each part at each radiation level resulting in several symbols for each part/level. The spec limit for this parameter is 0.5nS so obviously all parts passed. Also obviously there was no change in this parameter after radiation to 300K rad(Si).

A complete set of pre/post radiation plots are included in Appendix D. These plots show that there was no change in any I/O AC parameter (e.g. setup/hold parameters, prop delays).

There was a slight change in the maximum operating frequency of the devices (Fmax or inversely Tcyc) as can be seen in figure 8.

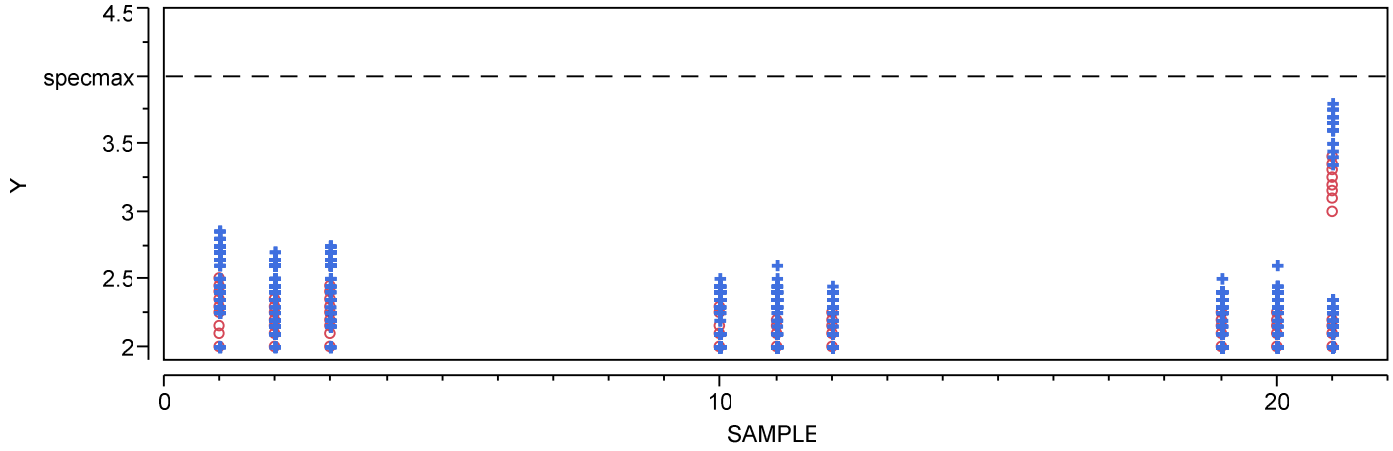


Figure 8. Tcyc Before Radiation (Pink Circles) and After 300K rad(Si) (Blue Crosses)

These parts operate with a latency of 2 clock cycles so actual Write/Read operations are isolated from I/O timing. Write/Read operations involve long logic chains and analog type functions (e.g. sense amps). The slight decrease in Fmax (increase in Tcyc) represents a change to some portion of this internal circuitry and can be attributed to the radiation exposure.

Also note that one DUT (SN21) showed sensitivity to certain patterns before total-dose exposure. This could be due to a pre-existing defect on the Die.

4.0 Burned-In vs. Non-Burned-In Radiation Response

Eight DUTs were tested to evaluate the effect of burn-in on radiation sensitivity. Parts used are shown in table 3. DC parameters and AC functionality were measured on-site during irradiation using the same test programs, fixtures and procedures that are used for RLAT testing. The first 5 parts in the table were irradiated to 300K rad(Si) and transported back to Cypress Semiconductor using the TM1019 dry ice procedure for AC characterization. The last 3 parts were further irradiated to 450K rad(Si).

Burned In?	S.N.
Yes	19AC
“	30AC
“	51AC
No	18NBI
“	38NBI
“	39NBI
“	42NBI
“	55NBI

Table 3. Parts Used for Burn-In/No-Burn-In Testing

Typical results of the AC characterization are shown in figure 9, a plot of Tco (Clock Rise to Data Valid) before and after radiation. Several test patterns were used for each part at each radiation level resulting in a spread of measurements for each part/level.

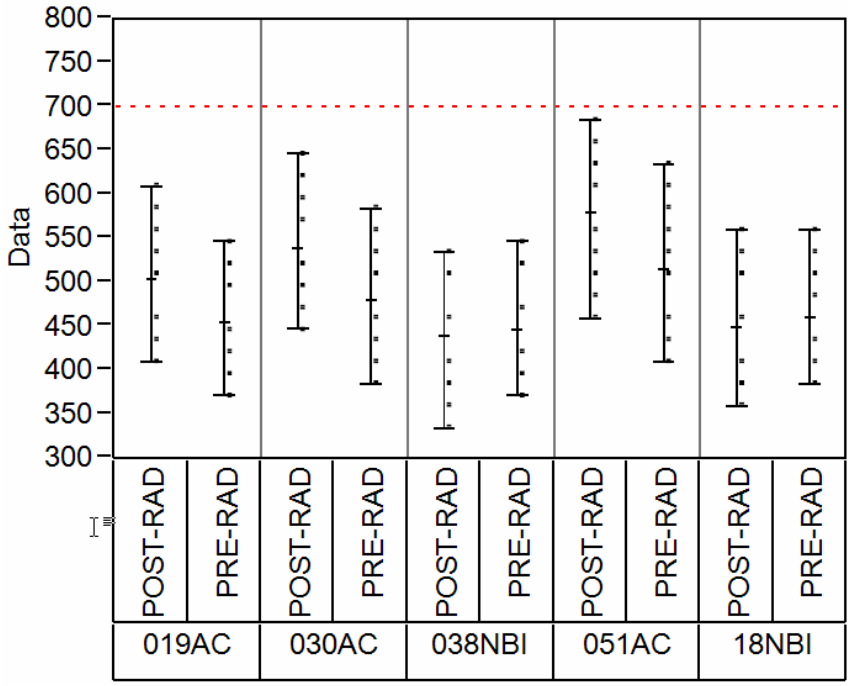


Figure 9. Tco Pre- and Post-Radiation, Various Devices

In this plot the pre- and post-radiation spread for each DUT is plotted separately and both plots are directly above the corresponding DUT name.

Please note that the burned-in units were AC characterized before burn-in and after irradiation, but not just before irradiation. Thus, any changes between the two measurements could be the result of either burn-in or radiation. This figure shows that the 2 non-burned-in parts (SN18 and SN38) changed very little with radiation. The other 3 parts (SN19, SN30, SN51) all showed a slight shift after both burn-in and irradiation. For these 3 parts the entire data spread has shifted slightly upwards. Based on previous lifetime testing of this product this shift is interpreted as being caused by the burn-in and not the radiation.

This difference in AC shift between burned-in and non-burned-in parts was seen on several parameters. The only parameter where a significant shift was seen on both burned-in and non-burned-in parts was Fmax (or inversely Tcyc). Results of this parameter are shown in figure 10.

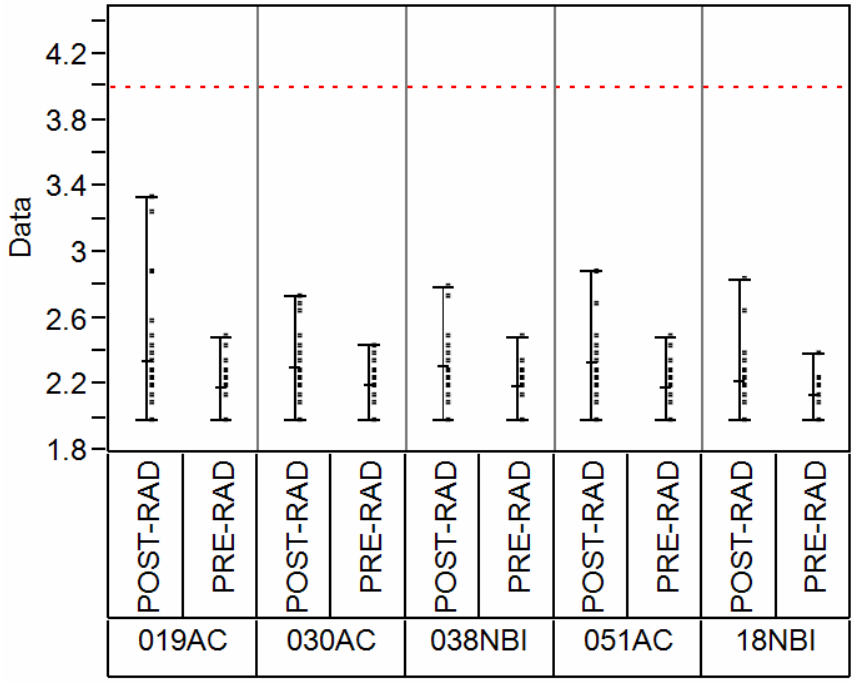


Figure 10. Tcyc Pre- and Post-Radiation, Various Devices

Note in this figure that all parts show an increase in Tcyc after radiation. This is the same parameter that showed radiation sensitivity in the AC parameter TID sensitivity testing reported in section 2.0 above. Also note that shifts in this parameter are of similar magnitude as seen in section 3.0.

A complete set of plots for the AC measurements is included in Appendix E.

All 8 parts were also measured on-site for AC functionality and DC parametrics. Five of the parts were irradiated to 300K rad(Si) and then removed for AC characterization. The other 3 parts were then irradiated to 450K rad(Si). All parts remained fully functional at 250MHz at all radiation levels and none of the measured parametrics showed any significant change.

5.0 Technology Characterization Vehicle Data

Six DUTs were tested to evaluate the inherent radiation hardness and the capability level of the technology. Parts used for this test are shown in table 3. All parts were irradiated to 600K rad(Si) which is 2X the guaranteed TID level for these parts. DC parameters and AC functionality were measured on-site during irradiation using the same test programs, fixtures and procedures that are used for RLAT testing.

Fab Lot	S.N.
L4046805	4
“	5
L4034627A	13
“	14
L4034627	22
“	23

Table 3. Parts Used for Inherent Radiation Sensitivity Testing

There was a slight increase in operating current with increasing radiation and also a slight increase in Iozh. Figures 11 and 12 show these changes. No other parameters showed any noticeable change.

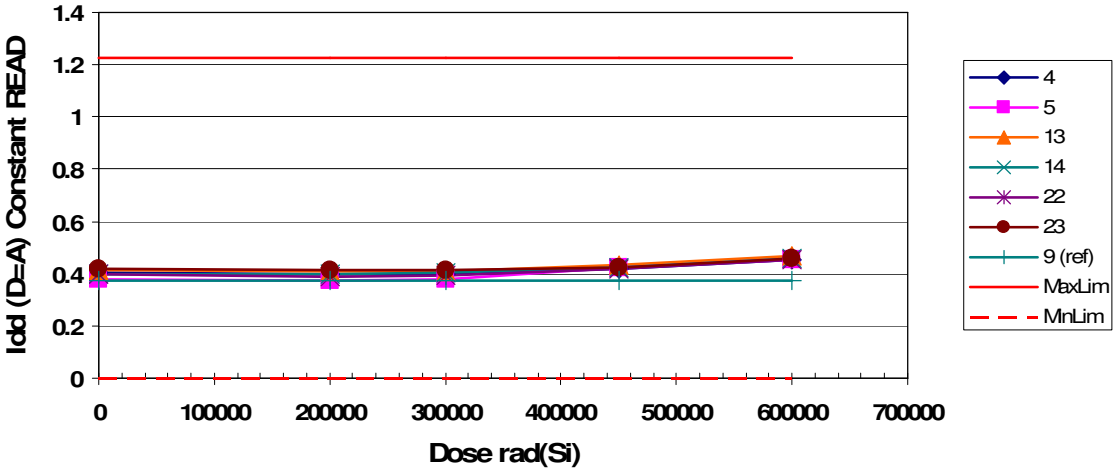


Figure 11. Idd Constant READ, D=A Pattern vs. Radiation

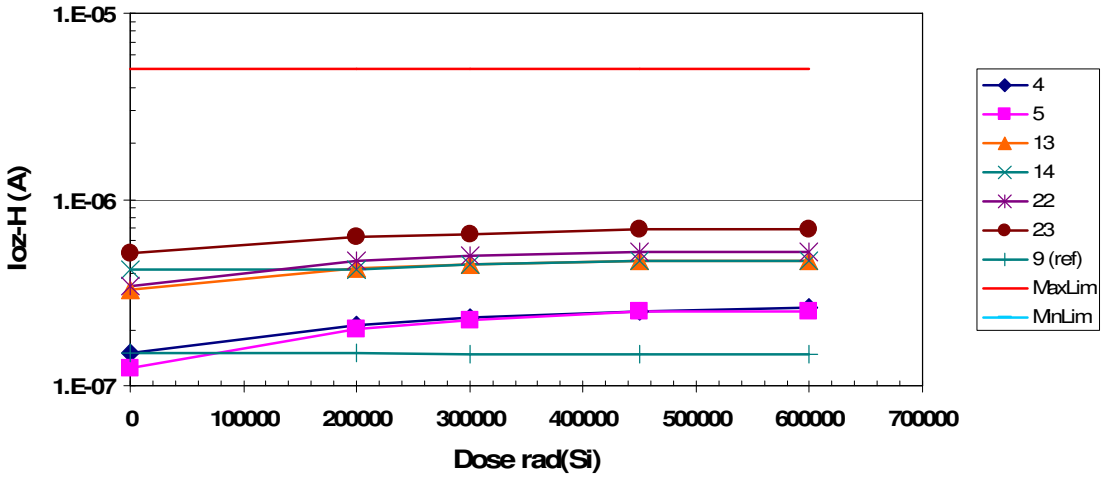


Figure 12. Iozh vs. Radiation

A complete set of plots for the DC measurements is included in Appendix F.

6.0 Conclusions

TID testing has been carried out on samples from multiple fabrication lots and multiple flow options. It has been established whether RLAT units are tested prior or post burnin does not impact the AC parameters of the device. Therefore RLAT units can be selected for RLAT testing prior or post burnin. Furthermore a detailed AC characterization has revealed that only Tcyc is sensitive to total ionizing dose during RLAT testing. Therefore Tcyc will be added to SMD subgroup9 and validated during RLAT testing. We have furthermore established that there is no lot to lot variability and the process is stable with respect to radiation hardness assurance.

In addition the technology capability level has been established at 600krad total ionizing dose which fulfills MIL-PRF-38535 Apendix. C requirements for radiation assurance with respect to TCV.

Appendix A. RLAT Test Conditions and Specifications

Common Test Conditions:

VDDq During Measurements = 1.8V
VDD During Measurements = 1.5V
Clock Frequency = 250MHz

1. Idd – Various Patterns (1.225A) – CB, CB*, All 1's, All 0's, D=A
2. Isb – Various Patterns (600mA) –CB, CB*, All 1's, All 0's, D=A
3. IiL/Iih – Input Leakage Current (+/-5uA)
    a. 0V & Vddq applied to all Address Pins
    b. Measure Input Currents
    c. Record Highest Value
4. Iozl/Iozh – Output Leakage Current (+/-5uA)
    a. 0V & Vddq applied to all I/O Pins
    b. Measure Output Currents
    c. Record Highest Value
5. Voh(Low Current)/ Voh (2mA) – Output High Voltage (min) (>1.2V / >0.82V)
    a. Load 4 successive memory location with all 1's
    b. Continuously Read Pattern,
    c. Measure outputs with -0.1mA/-2mA load current
    d. Record lowest reading
6. Vol(Low Current)/Vol(2mA) – Output Low Voltage (max) (<0.2V / <0.58V)
    a. Load 4 successive memory location with all 0's
    b. Continuously Read Pattern,
    c. Measure outputs with +0.1mA/+2mA load current
    d. Record highest reading
7. Vih - Input Logic Voltage for Proper Operation (<0.85V)
    a. Vary Vih in binary search sequence
    b. For every voltage level perform write/read of entire memory
    c. Record highest input voltage for which all memory locations pass

8. Vil - Input Logic Voltage for Proper Operation (>0.65V)
    a. Vary Vil in binary search sequence
    b. For every voltage level perform write/read of entire memory
    c. Record lowest input voltage for which all memory locations pass

Appendix B. Bias Conditions During Irradiation
VDD During Irradiation = 1.9V

VDD and VDDQ Pins = 1.9V
VSS Pins = 0V
Load Checkerboard pattern into all DUTs
Clock Frequency = 250MHz

Appendix C. Photographs of Boards and Fixturing

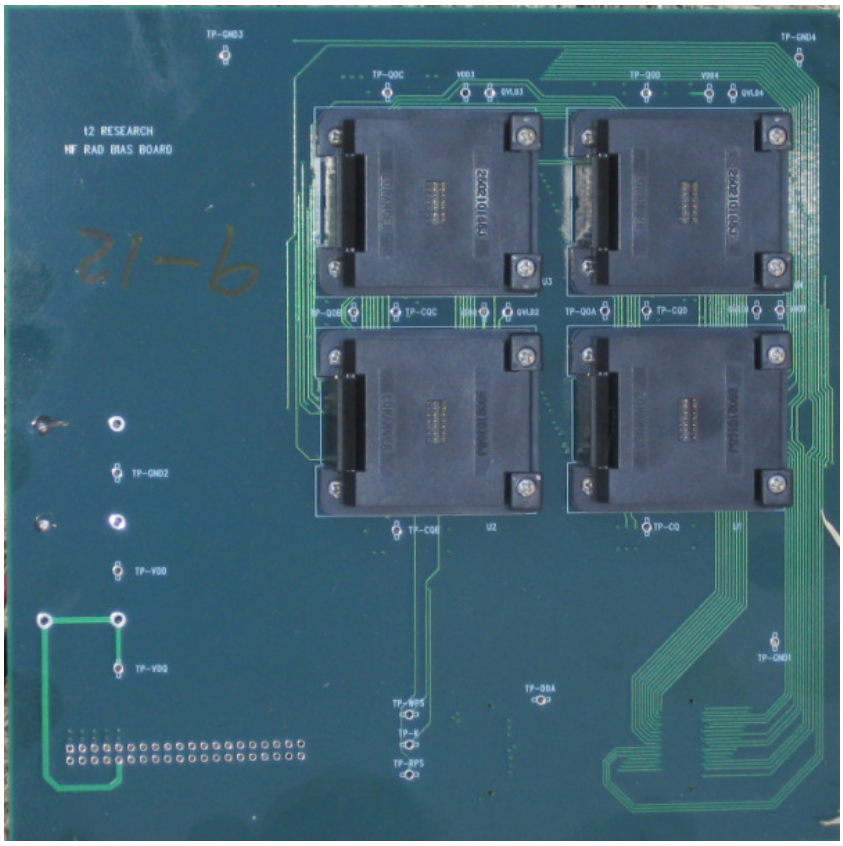


Figure C1. Front of Bias Board

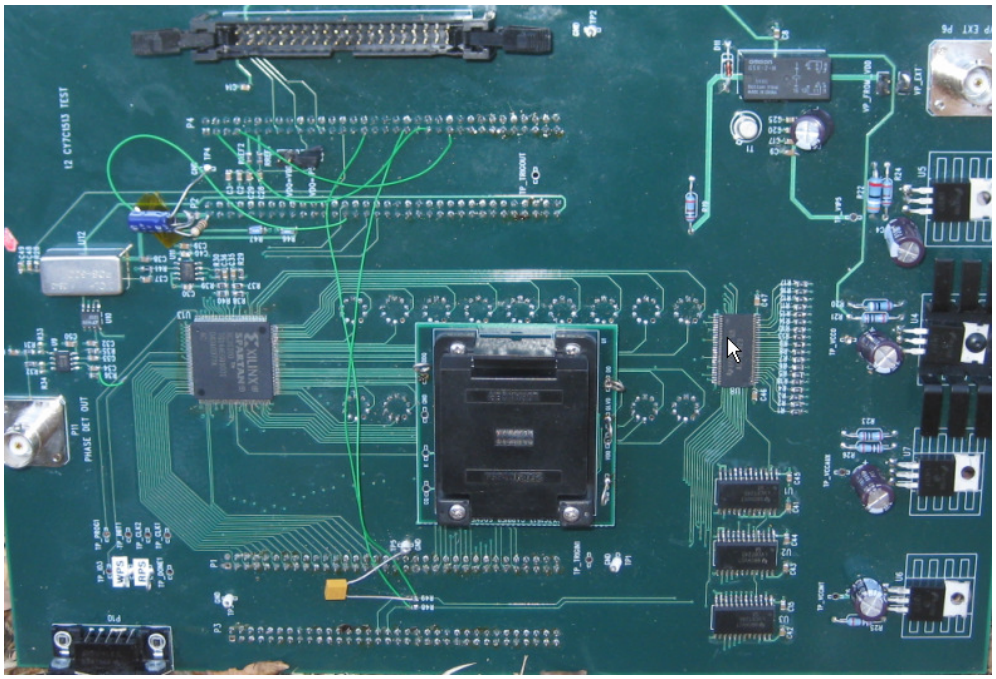
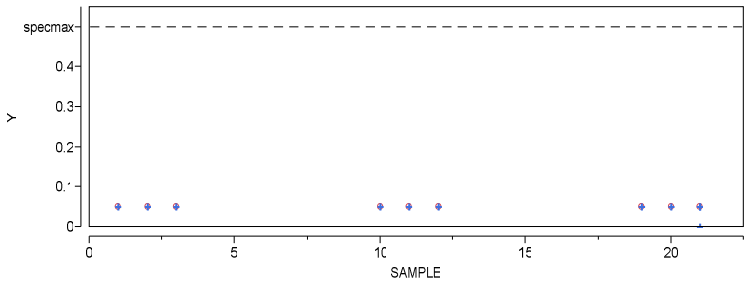
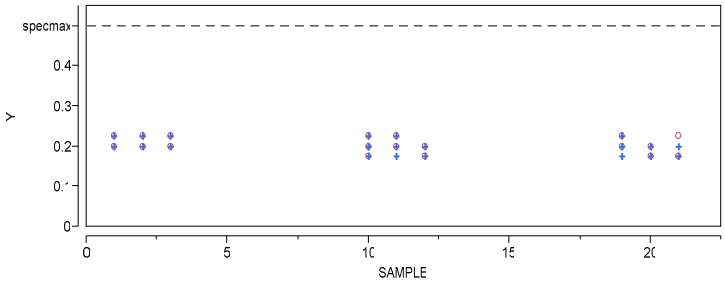


Figure C2. Test Card

Appendix D. AC Parameters vs. TID Radiation, 3 DUTs ea. From 3 Lots



Tah



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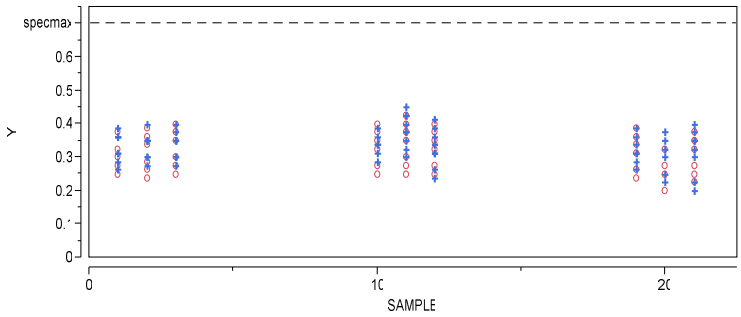
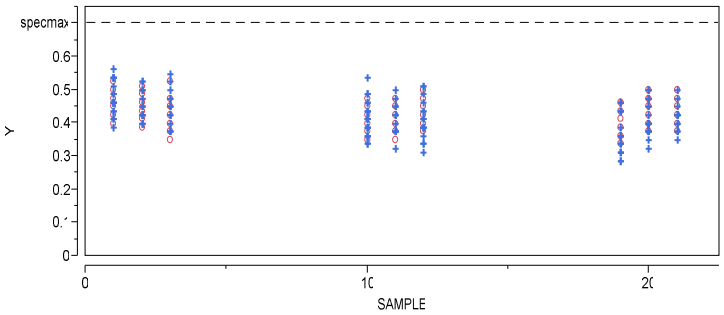
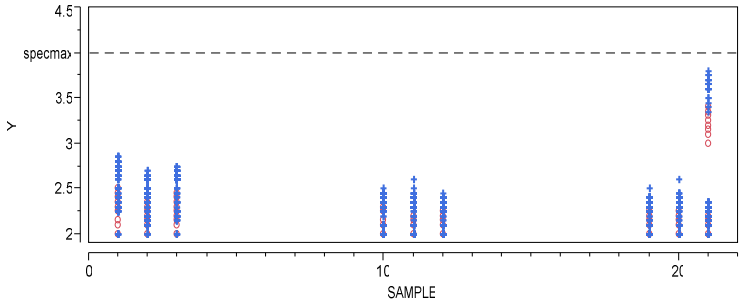


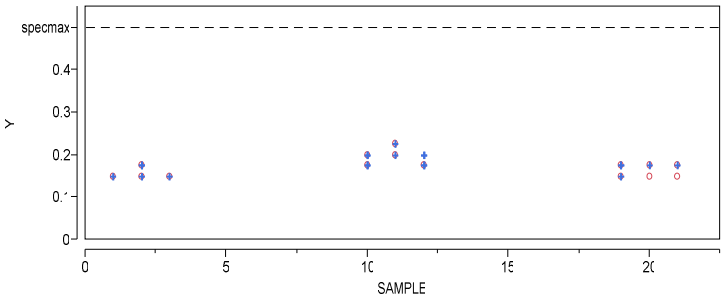
Tccqo



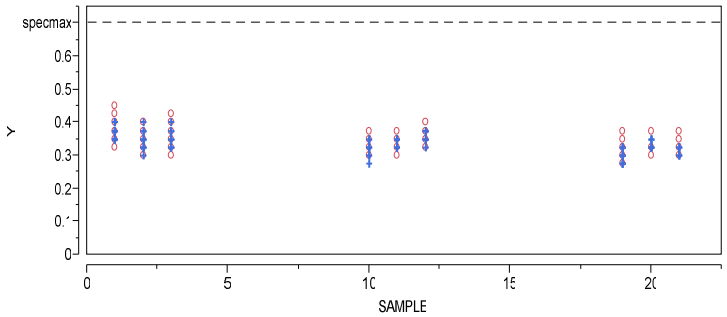
Tco



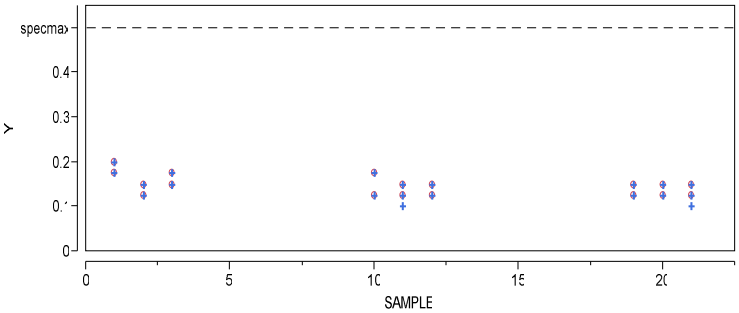
Tcyc



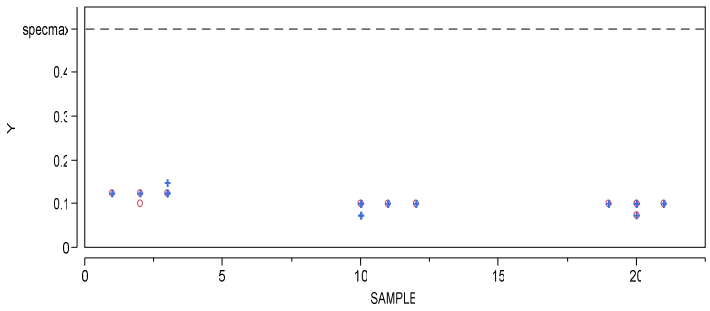
Tdh



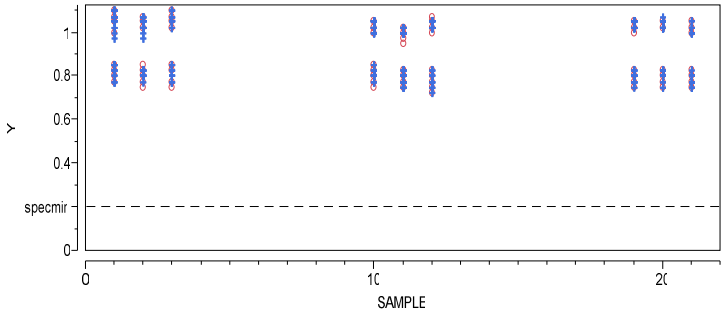
Tdoh



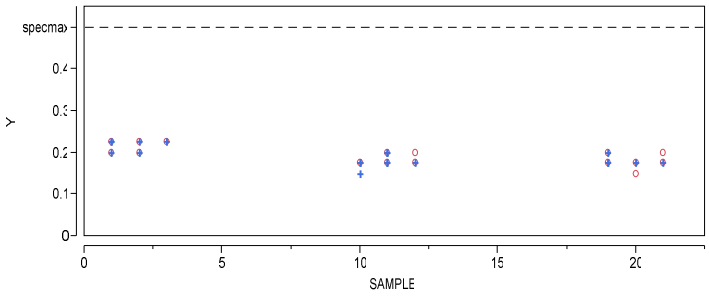
Tds



Thc

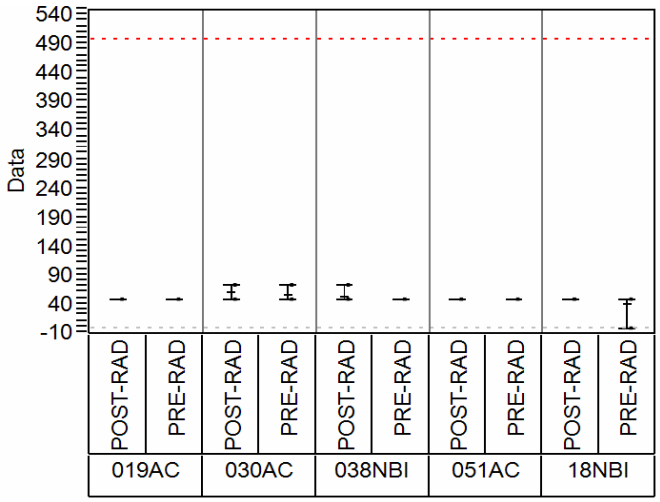


Tkhk*h

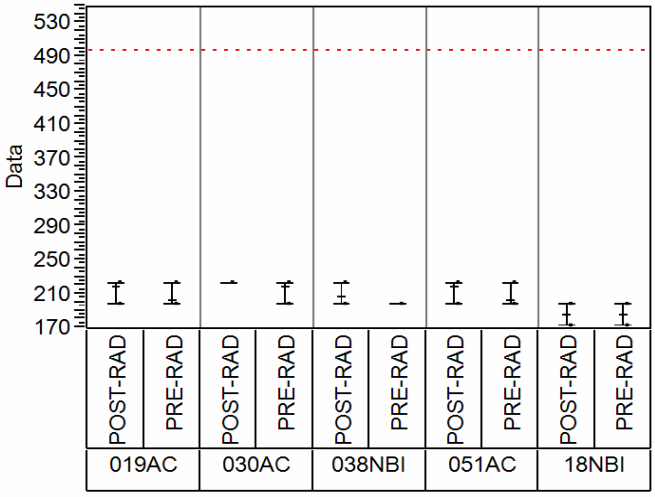


Tsc

Appendix E. TID Radiation Sensitivity of Burned-In vs. Non-Burned-In Parts



Tah



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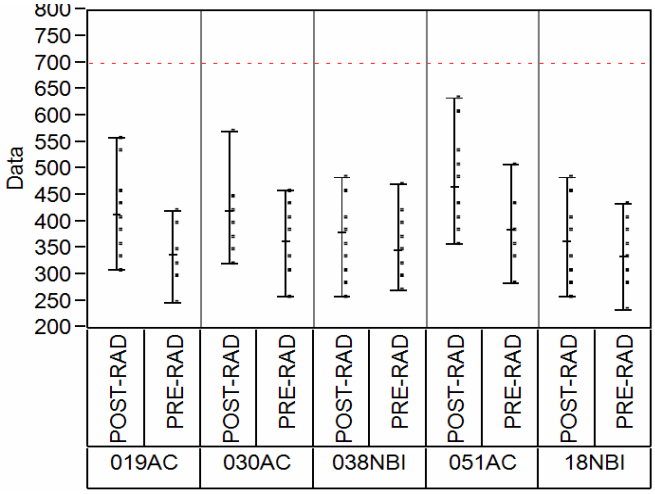

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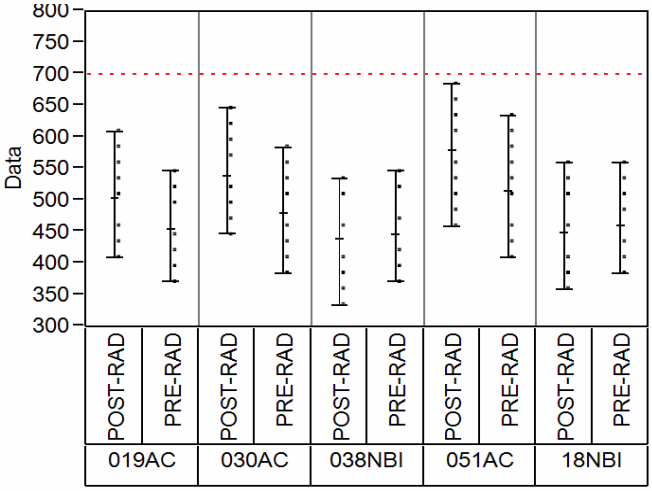

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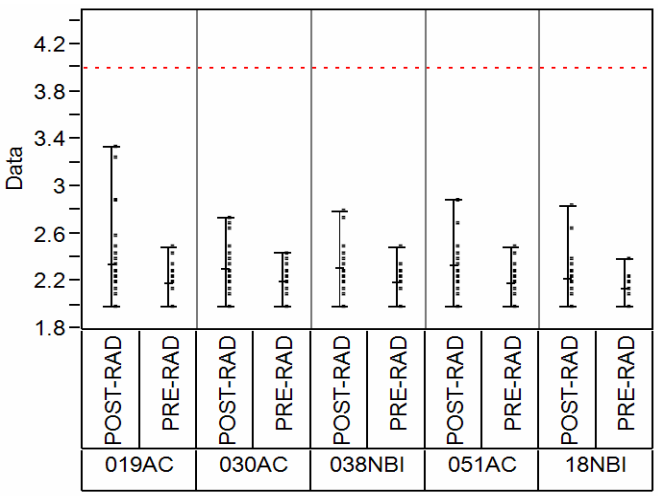

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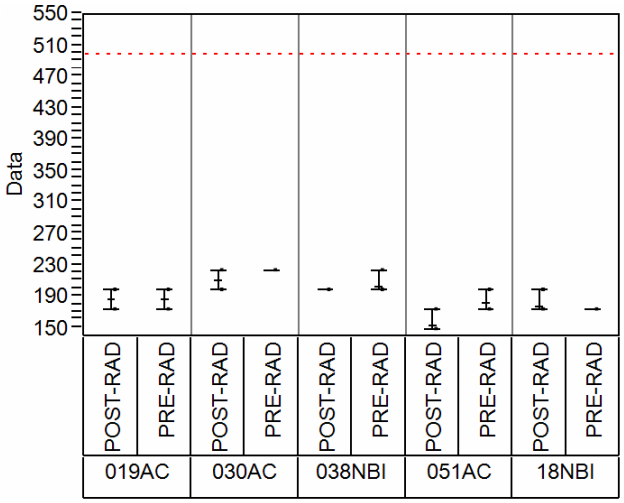

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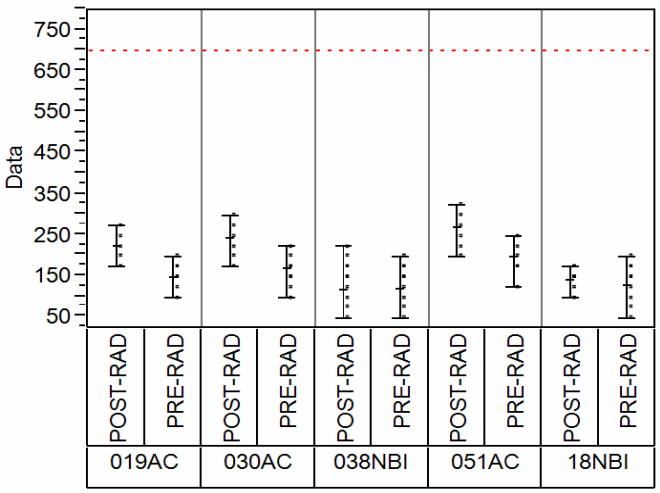

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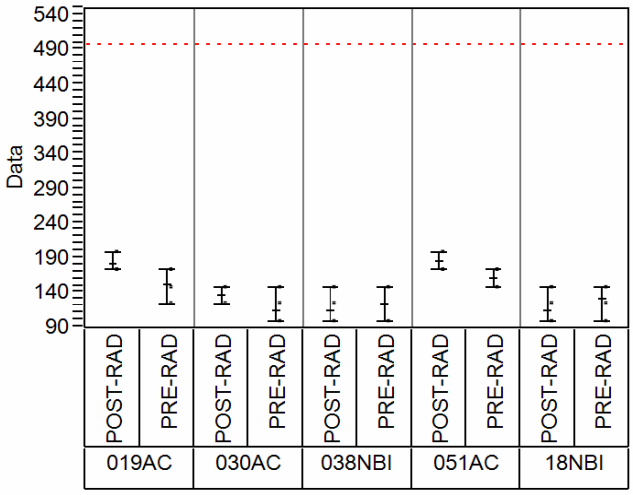

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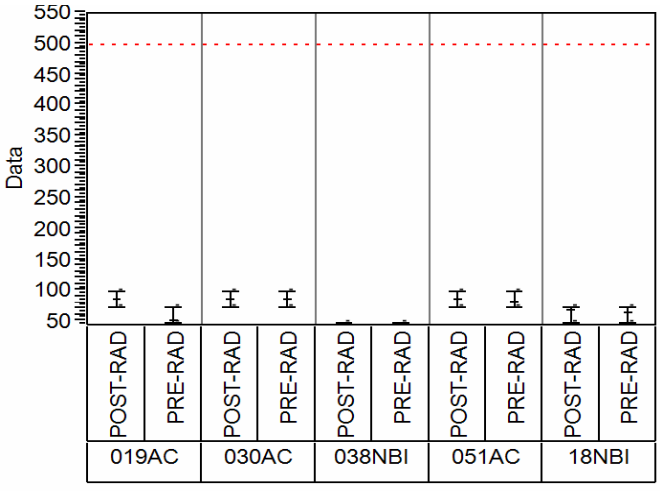

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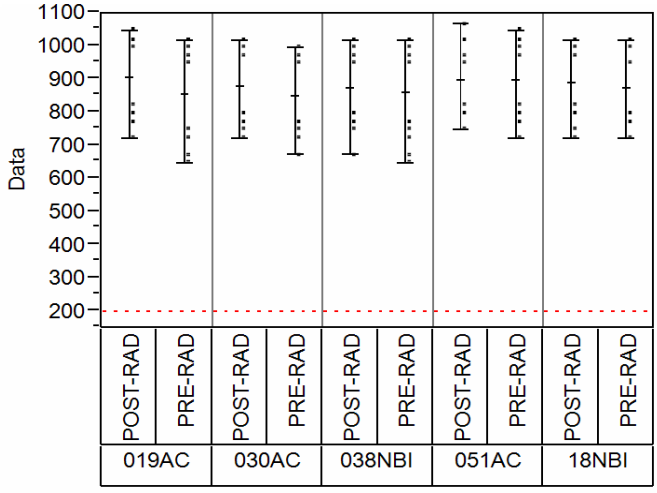

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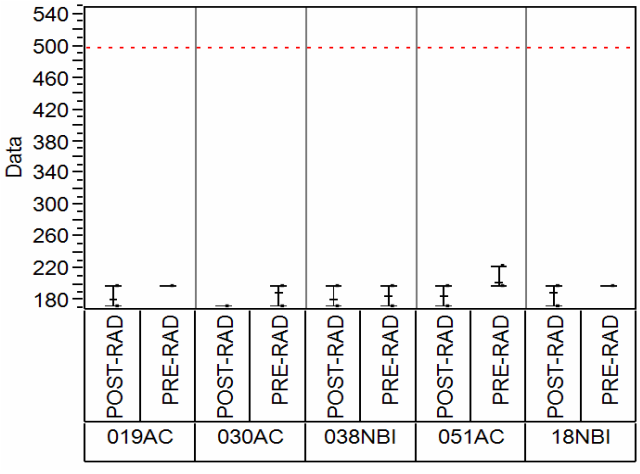
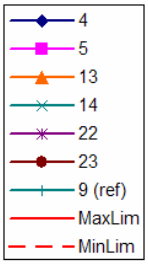


Tsc

Appendix F. Inherent Radiation Sensitivity Measurements



Legend for Plots