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SEE Final Report for Cypress Semiconductor CYRS1543AV18, 72-Mbit QDR SRAMs

Date: 20 Dec 2011 Revision: B

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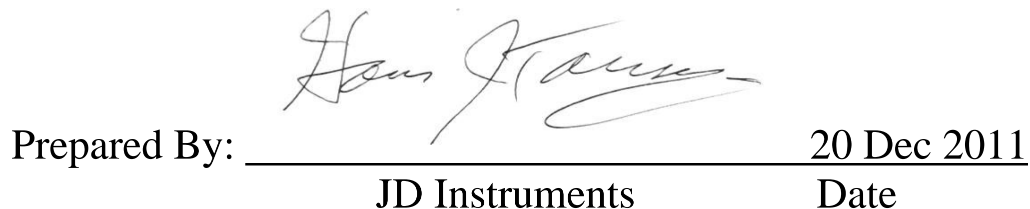

Prepared By: ______________________ 20 Dec 2011
JD Instruments Date

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1.0 Test Overview

Single Event Effects (SEE) testing was performed on Cypress Semiconductor CYRS1543AV18 72-Mbit QDR SRAMs on 9/10 Dec, 2010 at the Texas A&M University Cyclotron facility. Memory on this device is accessed via an 18 bit wide data buss. Because of the QDR architecture there are 18 inputs (D0 – D17) and 18 separate outputs (Q0 – Q17). Write and READ operations are both done in bursts of 4 to successive internal memory locations.

Internally read and write operations are 72 bits wide as shown in figure 1. Control logic and latches convert the internal memory architecture to the "X18" architecture seen externally.

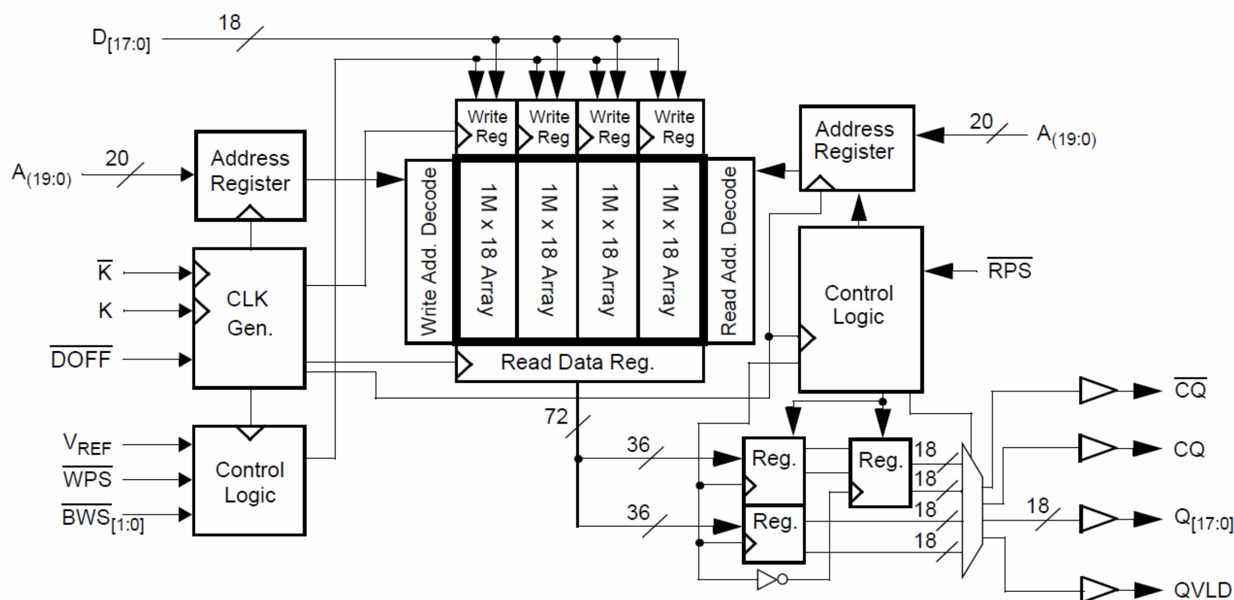

Figure 1. Functional Diagram for CYRS1543AV18

Testing was performed using a JD Instruments Algorithmic Test Vector (ATV) system. The main chassis of the tester was located in the SEE irradiation room and connected to the test head mounted on the actuating arm of the chamber. A USB cable connected the tester to a controlling computer located in the experimenter area.

These devices were packaged in column grid array (CGA) packages which had their lids attached with tape. They were permanently mounted to small carrier cards to make handling them easier at the facility and to prevent damaging them when their tops were removed. An overview of the carrier card is shown in figure 2.

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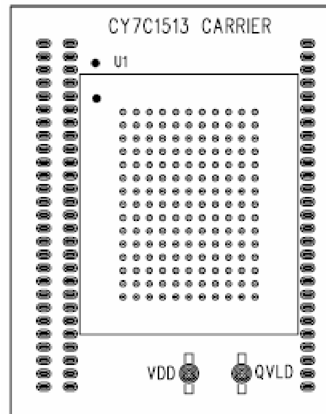

Figure 2. Carrier Card for CYRS1543AV18

All testing was done with one device at a time inserted into a test card mounted on the ATV test head. Circuit schematics for the test card are shown in attachment 1.

Testing was performed by Jake Tausch of JD Instruments and Helmut Puchner of Cypress Semiconductor.

Testing was done in compliance with ASTM F1192, “Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices” and also in compliance with EIA/JESD57, “Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation”.

Results from previous testing on commercial versions of the part were used to select LET values for testing in order to test portions of the LET vs. Cross-section curve required by EIA/JESD57. Previous test results from commercial parts are included in this report for comparison purposes and are clearly differentiated from results for the part version being qualified herein.

Four types of tests were performed:

1. Static Bit Upset
    a. Checkerboard Pattern
    b. Data at each address = Lower 18 bits of address (D=A)
2. Dynamic Test of Control Logic
3. Latchup
4. Single Event Functional Interrupt (SEFI)

Five parts were measured at every condition. For all tests, including static upset tests, the parts were continuously clocked at 250MHz.

Three ion species were used for this test. Copper (^{63}CU) was used for LETs between 20 and 30 (MeV*cm^2)/mg, Nitrogen (^{14}N) for LET = 1.3 (MeV*cm^2)/mg, and Xenon (^{129}Xe) for LETs between 53 and 120 (MeV*cm^2)/mg.

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Testing was performed using the 15 MeV SEE beam. Parts were irradiated in air at a distance of 30mm from the aramica window of the source. Figures 3 and 4 show the range vs. LET for various ions available with this set-up. Note that all ions used had a range >120u in silicon

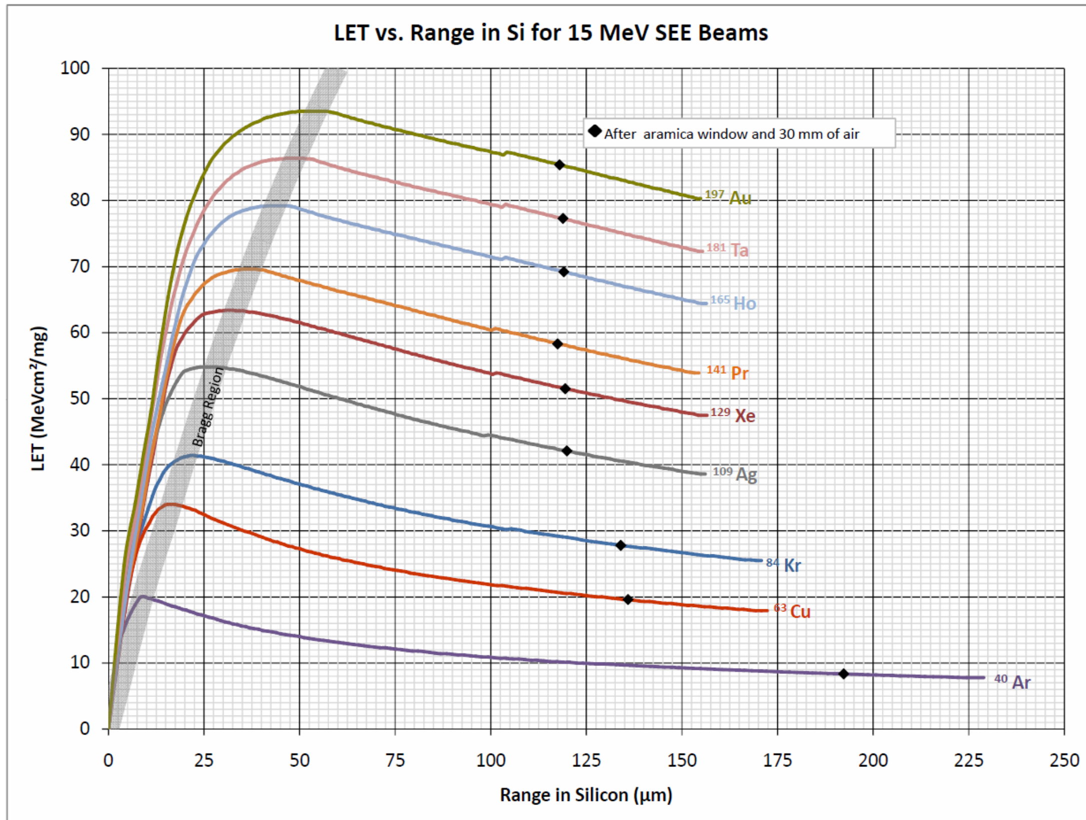

Figure 3. Ion Range vs. LET, Various Ions, 15 MeV beam, Texas A&M Cyclotron

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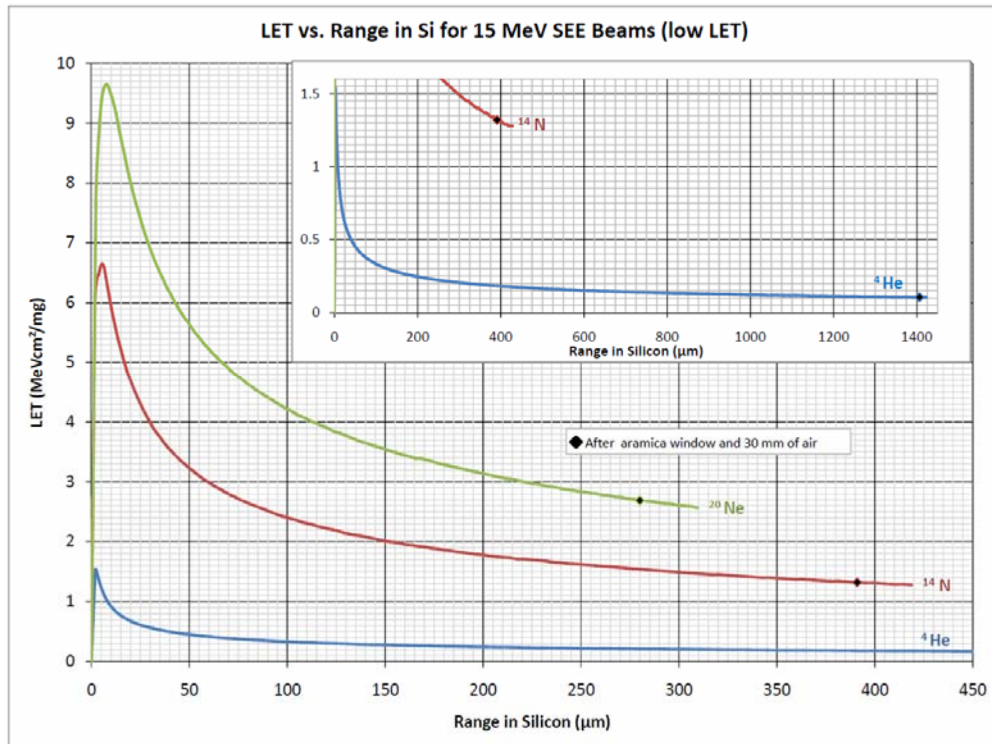

Figure 4. Ion Range vs. LET, low LET Ions, 15 MeV beam, Texas A&M Cyclotron

Figure 5 shows a cross-section for devices manufactured at this technology node. Note that all parts were manufactured using 3u epi wafers and that the total thickness of all overlayers was 5.5u. Any sensitive nodes must be within the 3u silicon layer and underneath the overlayers. Thus, ions must have a penetration depth of at least 8.5u to insure they reach all sensitive nodes. Since the actual range for the all ions is ~120u then they are sufficient for this test.

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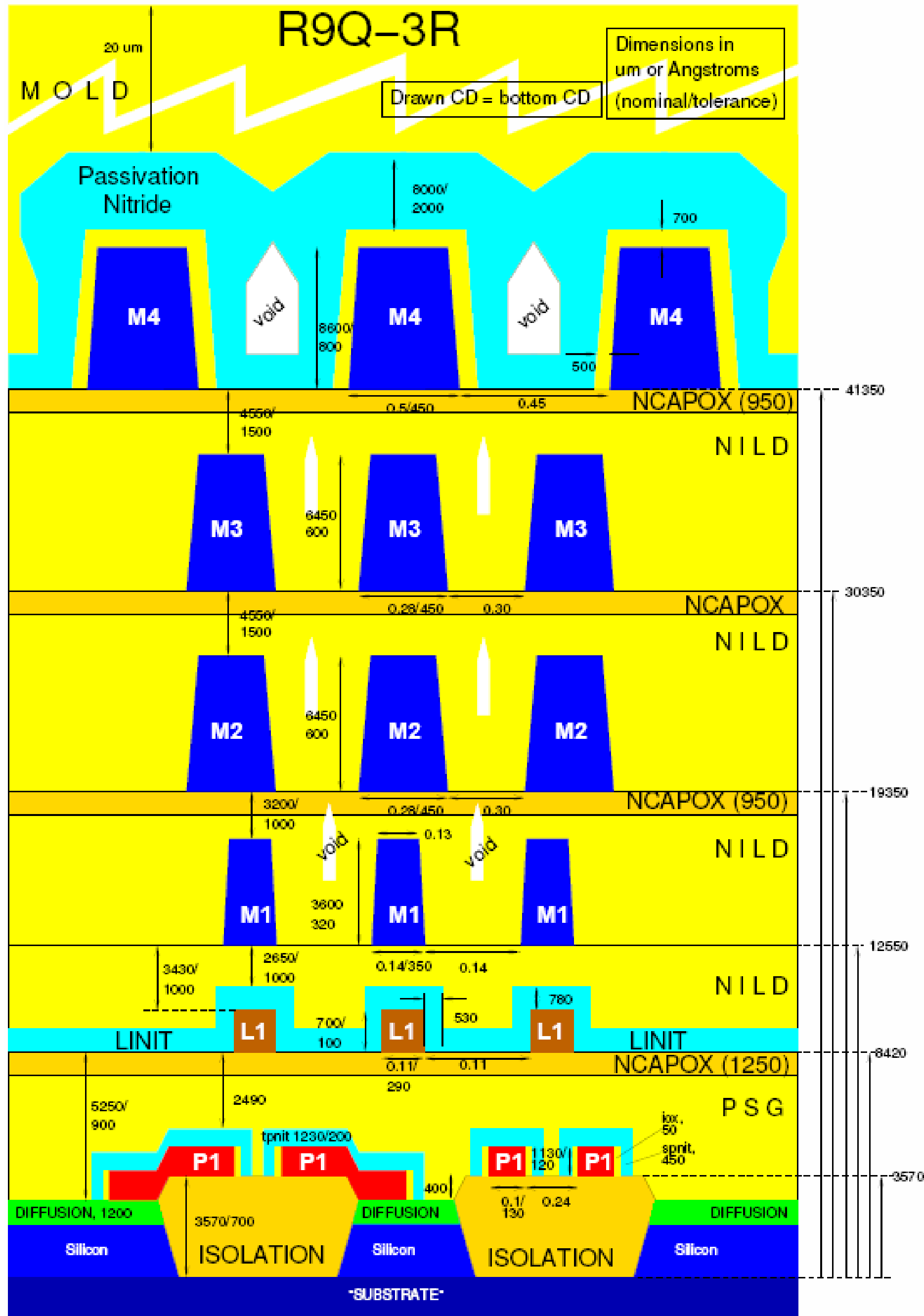

Figure 5. Device Cross-section in Angstroms

Accumulated total dose was tracked for each DUT over the course of testing (see Attachment 2. Run Log). Dose was calculated in the Run Log as LET * Fluence * 1.602E-5 and this agreed exactly with the dose as reported by the TAMU facility in run sheets.

Since all 5 DUTs were subjected to the same test sequence their resultant accumulated dose was very similar, ranging from 20.2K rad(Si) to 28.1K rad(Si). The variation in dose was due to some test exposures being performed more than once on some parts.

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These parts have previously been tested for total ionizing dose (TID) effects using ^{60}CO and have shown no sensitivity below doses of several hundred thousand rad(Si). The dose accumulated during these tests is not considered significant.

2.0 Latch-Up

These parts were tested for single event latch-up (SEL) at a single “worst case” condition of LET=120 (MeV*cm^2)/mg, Temp=125^{0}C and Vdd = Vddq = 1.9V. Latchup would be indicated by a sudden increase in Idd although a pattern was repeatedly written/read to the entire memory during the exposure runs so any occurrences of SEFI (Single Event Functional Interrupt) would have also been detected (see section 6.0 for further discussion of SEFI test sequence).

The LET value of 120 (MeV*cm^2)/mg was achieved by degrading the Xe ion to a normal incident LET of 60 (MeV*cm^2)/mg and irradiating the DUT at an angle of 60 degrees.

A DUT temprature of 125^{0}C was achieved by placing strip heaters underneath the carrier card of each DUT and heating the carrier card/DUT from the back side. An infrared thermometer was used to measure the actual die temperature. The infrared thermometer had a calibrated accuracy of +/- 1^{0}C (see figure 6).

Figure 6. Infrared Thermometer

Five temperature measurements were made on each die prior to SEL irradiation to insure the temperature of the carrier card/DUT combination had reached stable (no large temperature gradient). The die temperature was considered to be the average of all 5 readings.

Figure 7 shows typical temperature measurement results for one DUT prior to SEL irradiation.

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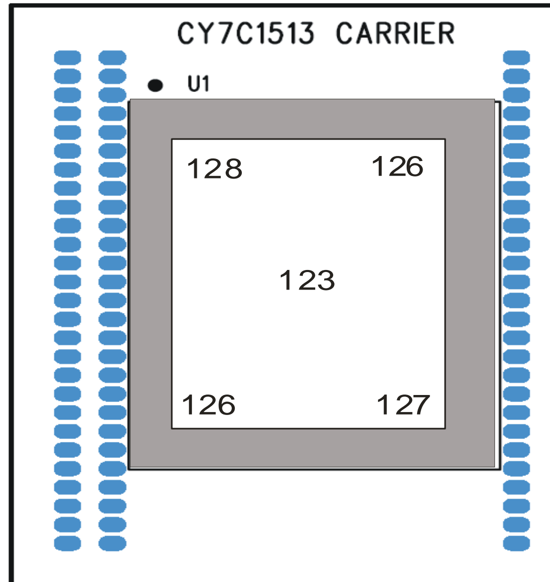

Figure 7. Distribution of Measured Temperatures Across DIE

Table 1. shows the 5 temperature measurements for each of the 5 DUTs prior to SEL irradiation as well as the average DIE temperature.

	POSITION					
	TOP			BOTTOM		Average
DUT	Left	Right	CENTER	Left	Right	Temp
1	136	130	124	122	124	127.2
2	133	133	125	124	127	128.4
3	133	130	124	118	121	125.2
4	128	133	124	124	127	127.2
5	128	126	123	126	127	126

Table 1. SEL DIE Temperature Measurements

Each of the 5 DUTs were irradiated to at least 1E7 ions/cm^2 and none of them exhibited any increase in power supply currents. DUT SN5 was actually irradiated to 1.39E7 ions/cm^2, again with no increase in power supply currents.

Combining results from all SEL runs, 5 devices were exposed a total of 5.43E7 ions/cm^2 at an LET of 120 (MeV*cm^2)/mg and temperature of 125^{0}C with no evidence of latchup. The conclusion is that these parts are not susceptible to latchup from heavy ion irradiation. Further, no SEFI failures were ever detected during this elevated temperature, high LET testing.

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3.0 Memory Upsets

Memory upset testing on these parts tests was performed with Vdd = 1.7V and Vddq = 1.4V. Upset behaviour was determined by loading them with a fixed pattern, irradiating to some fluence and then reading the pattern back. Two patterns were used: checkerboard and “D=A”. The D=A pattern is one in which the data at any given address is the same as the lower 18 bits of the address. Even though this was a static test the parts were operated at a constant clock frequency of 250 MHz. Writing and reading was performed in bursts of 4.

In accordance with EIA/JESD57, LET values should be chosen to yield cross sections relative to saturation of 75-80%, 50%, 25%, 10% and Onset. Results from previous testing of commercial parts were used to select LET values that would give these results. Table 2 shows that the results from this test closely match the recommended values.

	DUT Cross-Section (cm^2)						
LET	SN1	SN2	SN3	SN4	SN5	Average	% of SAT
94	1.2E-07	1.215E-07	1.673E-07	2.06029E-07	1.57491E-07	1.54E-07	100.0%
53.1	9.5E-08	7.37E-08	1.386E-07	1.23892E-07	1.29985E-07	1.12E-07	72.7%
30	4.86E-08	4.476E-08	9.295E-08	9.03387E-08	9.11263E-08	7.35E-08	47.6%
20.3	4.59E-08	2.918E-08	5.767E-08	5.02434E-08	4.7072E-08	4.60E-08	29.8%
1.3	5.88E-10	4.663E-10	7.461E-10	6.74884E-10	7.37243E-10	6.42E-10	0.4%

Table 2. Static Upset Cross-Sections for CB Data

Static upset results for the checkerboard pattern are plotted in figure 8.

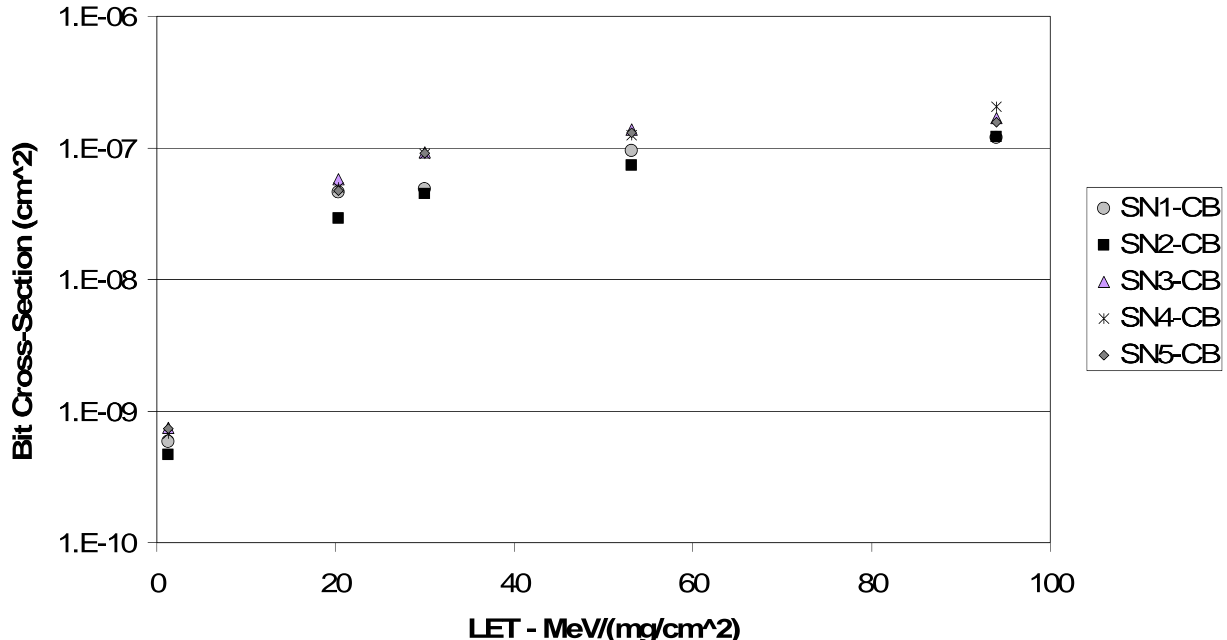

Figure 8. Static Upset Cross-Sections, Checkerboard Pattern

Figure 9. shows the cross-section measurements for both the checkerboard and D=A patterns. This plot shows that there was no pattern sensitivity to the upsets.

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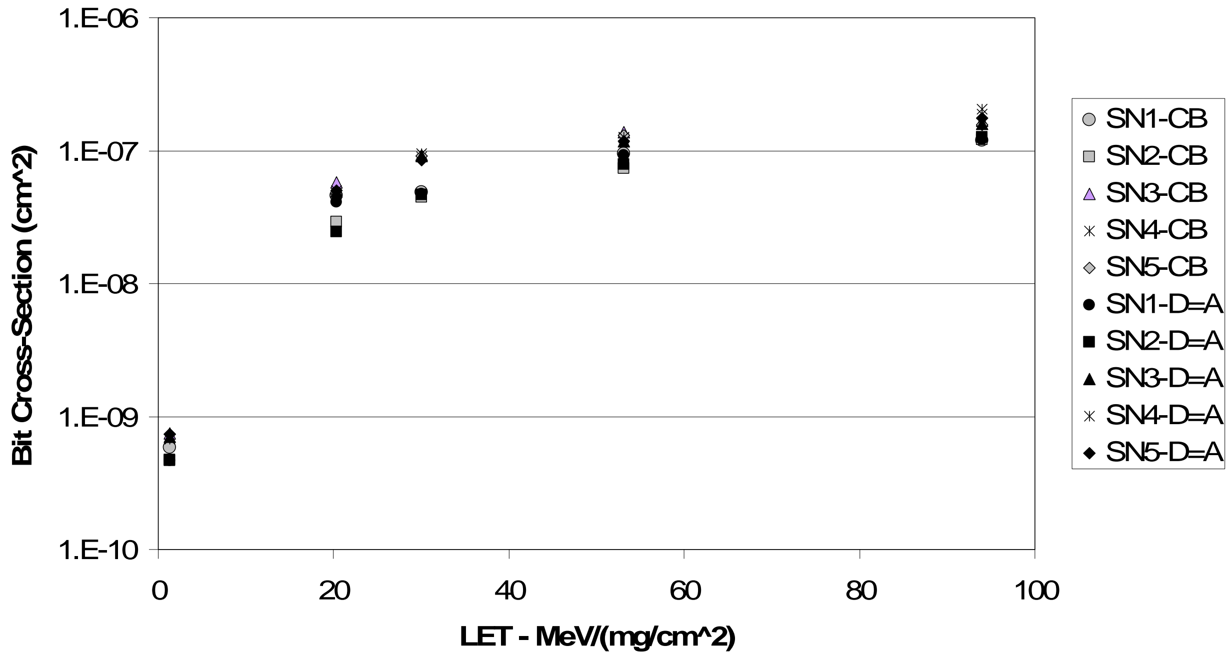

Figure 9. Static Upset Cross-Sections, Checkerboard and D=A Patterns

Commercial versions of this part have been tested extensively for SEE. For comparison purposes, Figure 10 shows data from the present test plotted along with data measured on commercial versions of this part type in previous tests

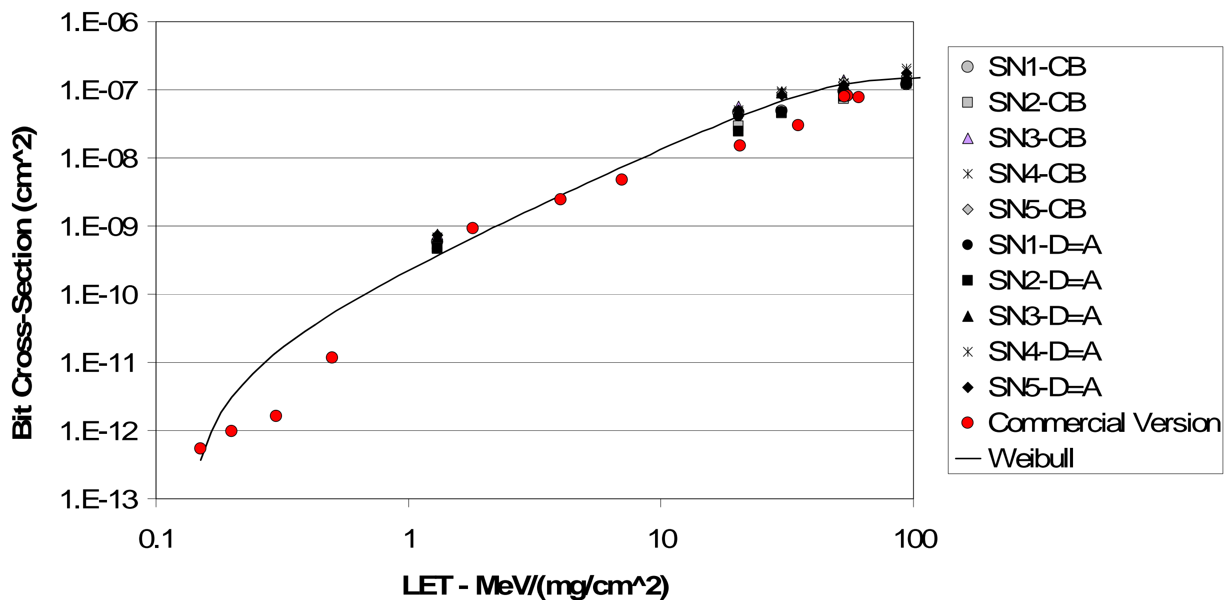

Figure 10. Static Upset Cross-Sections, Including Data From Previous Tests

Figure 10 is plotted on log-log scales so that data points at much lower LET values can be seen. From this plot it is obvious that parts tested here had very similar heavy ion response to commercial parts tested previously. It should be noted that data from previous tests were

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performed on parts with slight manufacturing variations (splits) which explains why they vary slightly from the present parts.

Figure 10 also includes a Weibull curve fitted to the data. Weibull parameters for this curve are as follows:

OnSet LET = 0.13 MeV/(mg/(cm^2))
Width = 40
Exponent = 1.7
Saturated X-Section = 15 u^2 = 1.5e-7 cm^2

4.0 Multi-Cell Upsets

These parts are designed so that memory cells for any given bit position are “tiled”. Thus, for example, all cells containing information that will be read out in the logical bit “0” position will be co-located in one physical array and this will be separated from other “tiles”. The result is that a multi-cell upset event from one heavy ion strike will present itself, when the part is read, as multiple upsets, all at the same bit position, but at different logical addresses. Examples of this pattern are shown in figure 11 where portions of recorded error logs are shown after a part has been exposed to several ions with increasing LET values.

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addr	data EXP	ERR	#BIT
0x26b5	011000110011000110	---------------F--	1
0x42e8	011000110011000110	--------------F---	1
0x15549	100011001100011001	----F-------------	1
0x2f67c	011000110011000110	---F--------------	1
0x356bd	011000110011000110	----F-------------	1
0x3a7cc	011000110011000110	------F-----------	1
0x3b1b3	100011001100011001	----------F-------	1
0x3d963	100011001100011001	-----F------------	1
0x5d734	100011001100011001	-----------F------	1
0x78d20	100011001100011001	---F--------------	1
0x8437c	100011001100011001	------F-----------	1
0x8dfde	011000110011000110	------------F-----	1
0xb3295	011000110011000110	----F-------------	1
0xbac1a	100011001100011001	-------------F----	1
0xc8a94	100011001100011001	F-----------------	1
0xd0830	100011001100011001	----F-------------	1
0xed2bd	100011001100011001	-------F----------	1
0x10dade	011000110011000110	F-----------------	1
0x113089	100011001100011001	F-----------------	1
0x123167	100011001100011001	---F--------------	1
0x1353b2	011000110011000110	-F----------------	1
0x138a85	100011001100011001	----------------F-	1
0x14622d	011000110011000110	-----------F------	1
0x15d7db	100011001100011001	----------------F-	1
0x1693d1	011000110011000110	----F-------------	1
0x177ba9	100011001100011001	-----------F------	1
0x1a8636	100011001100011001	-------F----------	1
0x1b0481	011000110011000110	------F-----------	1
0x1b4289	011000110011000110	------F-----------	1
0x1cb4cd	100011001100011001	F-----------------	1
0x1df226	100011001100011001	---------------F--	1
0x1e6e8a	011000110011000110	-----F------------	1
0x1e6f2d	011000110011000110	-----------F------	1
0x1e8e28	011000110011000110	-----------------F	1
0x1ebd6d	100011001100011001	---------------F--	1
0x1f80bf	100011001100011001	-----F------------	1
0x217613	100011001100011001	------F-----------	1
0x2254bd	100011001100011001	--F---------------	1
0x2595f0	011000110011000110	----F-------------	1
0x25e82b	011000110011000110	--------------F---	1
0x2857d4	011000110011000110	-----F------------	1
0x296fce	011000110011000110	-----------------F	1
0x2d1256	100011001100011001	-----------F------	1
0x2ee796	100011001100011001	---------F--------	1
0x300360	011000110011000110	----------F-------	1
0x3249ae	100011001100011001	------F-----------	1

LET = 1.8

addr	data EXP	ERR	#BIT
0xa5404	011000110011000110	-F----------------	1
0xa541c	011000110011000110	-F----------------	1
0xa63ab	100011001100011001	-------------F----	1
0xa6400	011000110011000110	-F----------------	1
0xa89e5	011000110011000110	-----------------F	1
0xa89ed	011000110011000110	-----------------F	1
0xa8dc3	100011001100011001	------F-----------	1
0xa8dcb	100011001100011001	------F-----------	1
0xa99e9	011000110011000110	-----------------F	1
0xa9c99	011000110011000110	-----------F------	1
0xa9dc7	100011001100011001	------F-----------	1
0xaac95	011000110011000110	-----------F------	1
0xacebf	011000110011000110	--------F---------	1
0xadc53	011000110011000110	------F-----------	1
0xadeb7	100011001100011001	--------F---------	1
0xadebf	100011001100011001	--------F---------	1
0xae026	100011001100011001	-F----------------	1
0xae03e	100011001100011001	-F----------------	1
0xae3a8	011000110011000110	------------F-----	1
0xae3ac	100011001100011001	------------F-----	1
0xaec4f	011000110011000110	------F-----------	1
0xaeeb3	100011001100011001	--------F---------	1
0xaeebb	100011001100011001	--------F---------	1
0xaeec3	100011001100011001	--------F---------	1
0xaf022	100011001100011001	-F----------------	1
0xaf434	011000110011000110	------F-----------	1
0xaf43c	011000110011000110	------F-----------	1
0xaf44c	011000110011000110	------F-----------	1
0xafa87	100011001100011001	------------F-----	1
0xafa8b	011000110011000110	------------F-----	1
0xb0128	100011001100011001	-----F------------	1
0xba74a	100011001100011001	F-----------------	1
0xbd11f	011000110011000110	-F----------------	1
0xbe103	011000110011000110	-F----------------	1
0xbf129	100011001100011001	-----F------------	1
0xc05fb	100011001100011001	-----F------------	1
0xc1377	100011001100011001	---------F--------	1
0xc237b	100011001100011001	---------F--------	1
0xc32b3	011000110011000110	----------------F-	1
0xc32cb	011000110011000110	----------------F-	1
0xc42c7	011000110011000110	----------------F-	1
0xc42cf	011000110011000110	----------------F-	1
0xc680f	011000110011000110	----F-------------	1
0xc780b	011000110011000110	----F-------------	1
0xc7813	011000110011000110	----F-------------	1
0xc8aeb	100011001100011001	---F--------------	1

LET = 20.6

addr	data EXP	ERR	#BIT
0x9f85	100011001100011001	-----F------------	1
0x9f8d	100011001100011001	-----F------------	1
0xaf89	100011001100011001	-----F------------	1
0xaf91	100011001100011001	-----F------------	1
0x19cd6	100011001100011001	F-----------------	1
0x1acd6	011000110011000110	F-----------------	1
0x1acde	011000110011000110	F-----------------	1
0x1bcd2	011000110011000110	F-----------------	1
0x1bcda	011000110011000110	F-----------------	1
0x1ea4e	011000110011000110	-----F------------	1
0x1ea56	011000110011000110	-----F------------	1
0x1ea5e	011000110011000110	-----F------------	1
0x1ea66	011000110011000110	-----F------------	1
0x1fa46	100011001100011001	-----F------------	1
0x1fa4a	011000110011000110	-----F------------	1
0x1fa4e	100011001100011001	-----F------------	1
0x1fa56	100011001100011001	-----F------------	1
0x1fa5e	100011001100011001	-----F------------	1
0x1fa66	100011001100011001	-----F------------	1
0x3768a	011000110011000110	--F---------------	1
0x38686	011000110011000110	--F---------------	1
0x3868a	100011001100011001	--F---------------	1
0x3968e	100011001100011001	--F---------------	1
0x50723	011000110011000110	-----F------------	1
0x5072b	011000110011000110	-----F------------	1
0x51727	011000110011000110	-----F------------	1
0x5172f	011000110011000110	-----F------------	1
0x52727	100011001100011001	-----F------------	1
0x5cfc0	100011001100011001	---F--------------	1
0x5cfc4	011000110011000110	---F--------------	1
0x8c231	100011001100011001	-------F----------	1
0x8c249	100011001100011001	-------F----------	1
0x8d231	011000110011000110	-------F----------	1
0x8d235	100011001100011001	-------F----------	1
0x8e245	011000110011000110	-------F----------	1
0x8e24d	011000110011000110	-------F----------	1
0xa0cb3	100011001100011001	-------F----------	1
0xa1490	100011001100011001	-----F------------	1
0xa14a8	100011001100011001	-----F------------	1
0xa1cb3	011000110011000110	-------F----------	1
0xa1cbb	011000110011000110	-------F----------	1
0xa2494	100011001100011001	-----F------------	1
0xa24a4	100011001100011001	-----F------------	1
0xa24ac	100011001100011001	-----F------------	1
0xa2caf	011000110011000110	-------F----------	1
0xa2cb7	011000110011000110	-------F----------	1

LET = 55

addr	data EXP	ERR	#BIT
0x2	011000110011000110	---------------F--	1
0x12	011000110011000110	---------------F--	1
0x1a	011000110011000110	---------------F--	1
0x84	100011001100011001	F-----------------	1
0x231	100011001100011001	-----------------F	1
0x235	011000110011000110	-----------------F	1
0x239	100011001100011001	-----------------F	1
0x23d	011000110011000110	-----------------F	1
0x241	100011001100011001	-----------------F	1
0x245	011000110011000110	-----------------F	1
0x251	100011001100011001	-----------------F	1
0x259	100011001100011001	-----------------F	1
0x25d	011000110011000110	-----------------F	1
0x283	100011001100011001	---------F--------	1
0x287	011000110011000110	---------F--------	1
0x28b	100011001100011001	---------F--------	1
0x293	100011001100011001	---------F--------	1
0x297	011000110011000110	---------F--------	1
0x29b	100011001100011001	---------F--------	1
0x29f	011000110011000110	---------F--------	1
0x2a3	100011001100011001	---------F--------	1
0x2ab	100011001100011001	---------F--------	1
0x2b3	100011001100011001	---------F--------	1
0x2bb	100011001100011001	---------F--------	1
0x2bf	011000110011000110	---------F--------	1
0x404	100011001100011001	--------------F---	1
0x40c	100011001100011001	--------------F---	1
0x41c	100011001100011001	--------------F---	1
0x650	011000110011000110	---F--------------	1
0x654	100011001100011001	---F--------------	1
0x660	011000110011000110	---F--------------	1
0x664	100011001100011001	---F--------------	1
0x668	011000110011000110	---F--------------	1
0x66c	100011001100011001	---F--------------	1
0x1231	011000110011000110	-----------------F	1
0x1239	011000110011000110	-----------------F	1
0x1241	011000110011000110	-----------------F	1
0x1249	011000110011000110	-----------------F	1
0x1251	011000110011000110	-----------------F	1
0x1259	011000110011000110	-----------------F	1
0x1261	011000110011000110	-----------------F	1
0x1269	011000110011000110	-----------------F	1
0x126d	100011001100011001	-----------------F	1
0x1283	011000110011000110	---------F--------	1
0x1293	011000110011000110	---------F--------	1
0x129b	011000110011000110	---------F--------	1

LET = 115.6 (110 deg-C)

Figure 11. Multi-Cell Memory Upset Patterns With Increasing LET ions

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One interesting feature of the error logs recorded by the ATV test system is that the information for each failing address includes the logical address, expected pattern, pattern of failing bits and also a count of the number of bits that failed at that address ("#Bit" column in the error log). From this it is easily seen that, even though higher LET ions caused multiple cells to upset, there were no instances of multiple bits failing at any address.

In fact, for all static testing performed on this set of parts there was never an instance where 2 or more bits were upset at any address. It should be noted that all static tests were designed to limit the total number of bit upsets from any one exposure to 20,000 or less. This limited the probability of multiple bits being upset at any address from separate, random ion strikes. Thus, the conclusion is that multi-cell upsets from any single ion strike will never cause a multi-bit failure at any address so that these memories are well suited to EDAC.

5.0 Control Circuitry Upsets

Control circuitry for these parts includes such things as address decoding logic, write strobes, sense amps, data latches, clock trees, etc. Special dynamic tests were performed to detect upsets in the control circuitry of these parts.

The dynamic test consisted of writing to a burst of 4 addresses and then immediately reading from those same addresses. This was started at address "0" and continued through the entire address space of the DUT. The pattern used for this test was "D=A". Since the data pattern was present for such a short time in the memory addresses space being exercised then any upset would most likely come from strikes on control logic circuitry.

In fact, upsets were recorded in the control logic portion of these parts and they had a distinctly different character from random memory upsets. Figure 12 shows a portion of one error log from a control logic test.

Test#	Total Errs	Logged Errs	ADDR	DATA EXP	ERR	#BIT
40	8	8	0xa10dd	0001000011011101	--------------FF	2
			0xa10e0	0001000011100000	-----------FFFF-	4
			0xa10e1	0001000011100001	----------FFFFFF	6
			0xa10e2	0001000011100010	-----------FFFF-	4
			0xa10e3	0001000011100011	-----------FFFF-	4
			0xa10e5	0001000011100101	--------------FF	2
			0xa10e7	0001000011100111	---------------F	1
			0xa10e9	0001000011101001	--------------FF	2
81	4	4	0x48a30	1000101000110000	-----------FFF--	3
			0x48a31	1000101000110001	-----------FFF--	3
			0x48a32	1000101000110010	-----------FFF--	3
			0x48a33	1000101000110011	-----------FFF--	3

Figure 12. Typical Control Logic Memory Upset Patterns

Note in this error log that one control logic upset occurred in test #40 and another didn't occur until test #81. In this case the test number corresponds to a write/read sequence through

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the entire memory space (4,194,304 addresses) using the burst address sequence described above. Thus, the entire memory was completely written and read 41 times between control logic upsets so their occurrence was extremely rare. In fact, for a total fluence of 5E5 ions/cm^2 there was typically 4-5 control logic errors.

A strike in the control logic circuitry typically resulted in a burst of multi-bit failures that could not be corrected using EDAC.

The probability of a control logic upset is very small. Figure 13 shows the cross-section of static memory upsets compared to the cross-section of control upsets when both are plotted as device level upsets. This plot shows that the difference in saturated cross-sections for the two types of events are approximately 6 orders of magnitude apart.

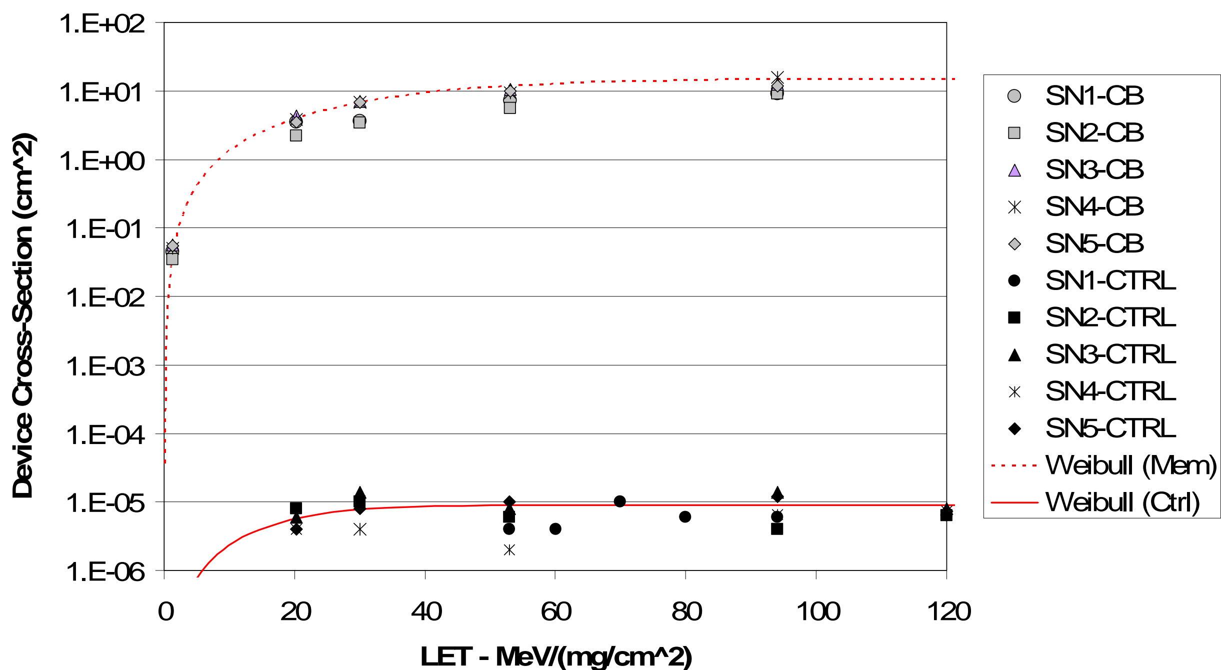

Figure 13. Checkerboard and Control Logic
Device Level Cross-Sections

Figure 13 also shows a Weibull curve fitted to the control upset data. Weibull parameters for this curve are as follows:

OnSet LET = 0.13 MeV/(mg/(cm^2))
Width = 20
Exponent = 1.7
Saturated X-Section = 900 u^2 = 9.0e-6 cm^2

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6.0 SEFI Behaviour

A Single Event Functional Interrupt (SEFI) is an upset in some portion of the device which causes continuing device failure until the device is reset or power cycled. No SEFIs were ever observed on any of these devices over the course of the entire test. Even when the devices were being tested for SEL they were being constantly exercised with the control logic upset algorithm (Write/Read, D=A, 4 address burst) to insure that they were functioning correctly.

Since no SEFIs were ever observed over the course of this test then we can combine the fluences from all devices and say that no SEFIs were observed when irradiated with various ions that had a combined fluence of 6.9E7 ions/cm^2.

7.0 Calculated Upset Rates

The Weibull fit for these devices had the following values:

Memory Upsets (bit):

OnSet LET = 0.13 MeV/(mg/(cm^2))
Width = 40
Exponent = 1.7
Saturated X-Section = 15 u^2 (1.5e-7 cm^2)

Control Upsets (device):

OnSet LET = 0.13 MeV/(mg/(cm^2))
Width = 20
Exponent = 1.7
Saturated X-Section = 900 u^2 (9.0e-6 cm^2)

Using these values the following device upset rates were calculated for various orbits using CREME96.

	SEUs/Device/Day	CTRL Upsets/Device/Day
Space Station, Solar Minimum	1.80E+00	7.90E-06
Space Station, Worst Day (Flare)	7.68E+02	4.40E-03
Geosynchronous, Solar Minimum	1.72E+01	6.60E-05
Geosynchronous, Worst Day (Flare)	6.70E+04	6.70E-01

Figure 14. Upset Rates for Various Orbits

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8.0 Conclusions

These parts all behaved very similarly when exposed to heavy ion radiation. Upset behavior was simple and repeatable. None of the parts latched up and none of the parts showed SEFI behavior. No single ion strike ever caused multiple bit upsets at one logical address so these memories should behave very well when used with a simple EDAC scheme such as Hamming.

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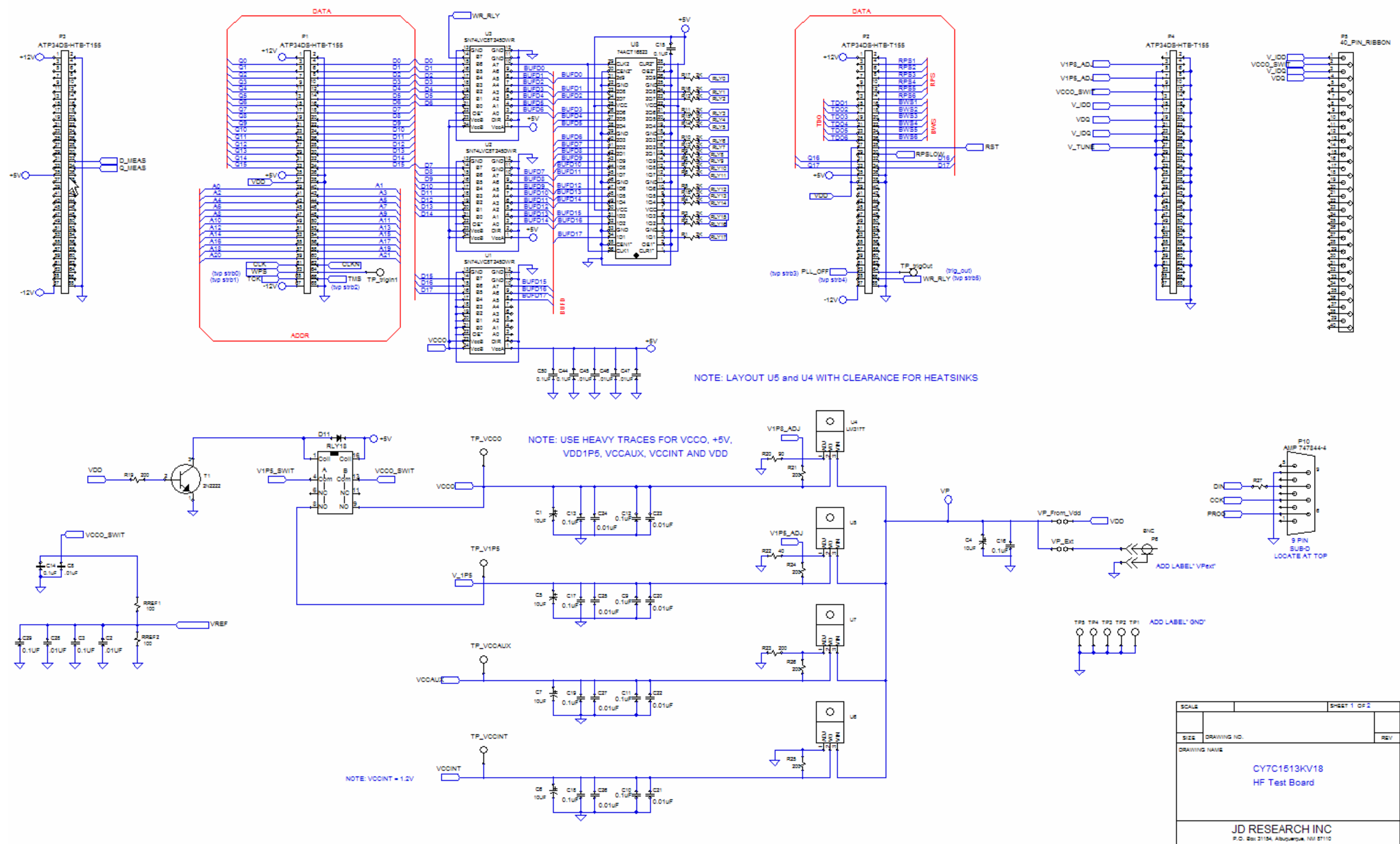
Attachment 1. Test Board Schematic



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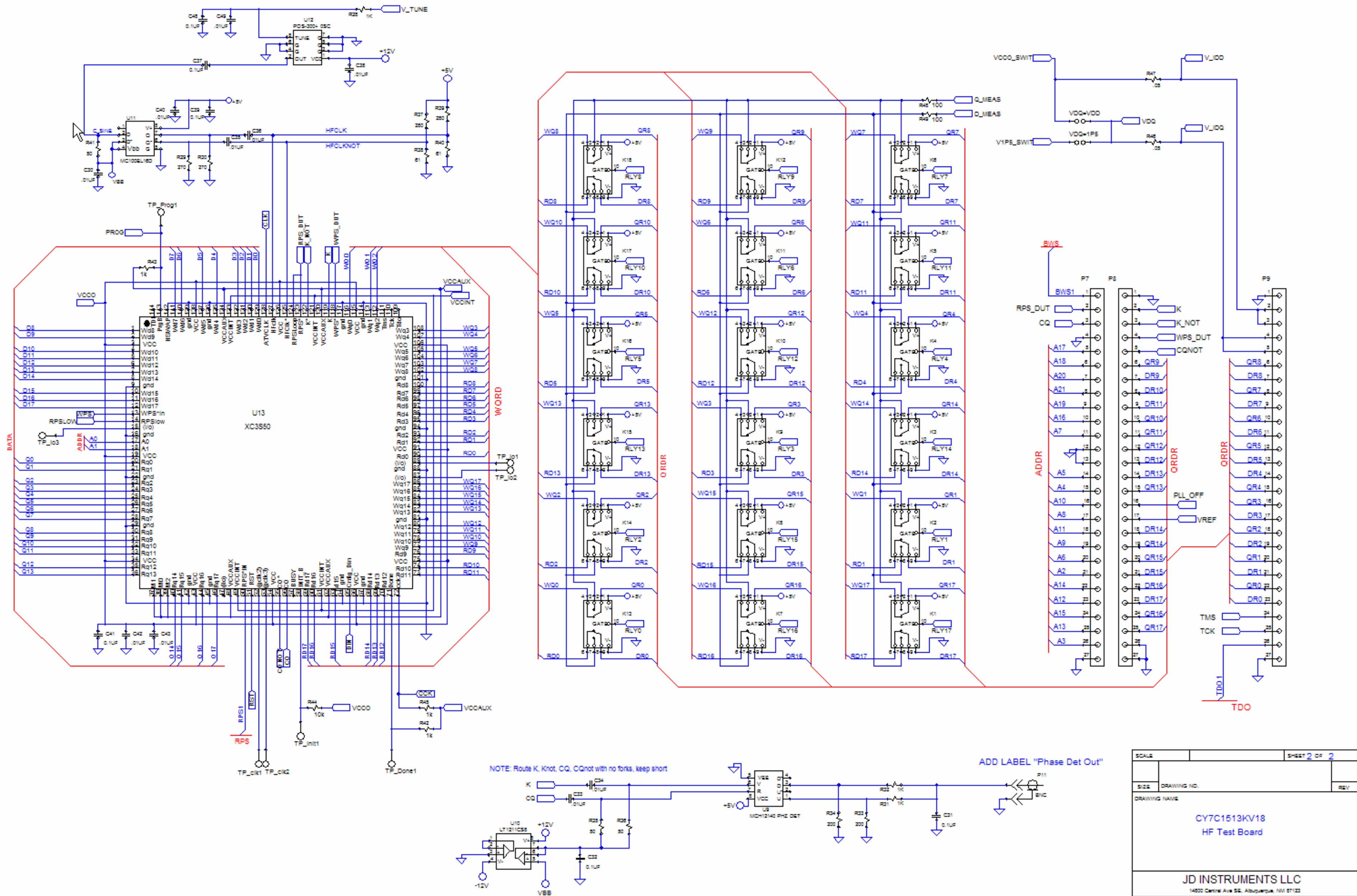

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Attachment 2. Run Log

RUN#	DUT	Start Time	Duration (Seconds)	Test	Clock Freq (MHz)	Ion	LET	Fluence	Flux	#Errs	#SEFI	#Pwr Cycles	Temp	High Current Latch?	Dose	Comment
1	SN1	9:23:34:38 12/9/20	83.81	CB,Static	240	CU	20.3	4930	112.2	17067	0	0	25	No	1.6013	
2	SN1	9:33:42:68 12/9/20	72.77	D=A	240	CU	20.3	4018	99.5	12372	0	0	25	No	1.305	
3	SN1	9:37:40:07 12/9/20	105.35	CB,Static	240	CU	30	3977	108.8	14580	0	0	25	No	1.909	
4	SN1	9:40:18:53 12/9/20	87.72	D=A	240	CU	30	4023	110.8	14345	0	0	25	No	1.931	
5	SN1	9:48:35:60 12/9/20	200.64	Ctrl Logic & SEFI	240	CU	30	1993000	12870	719	0	0	25	No	956.64	FLUX TOO High! 20Events
6	SN1	9:54:42:73 12/9/20	488.01	Ctrl Logic & SEFI	240	CU	30	500600	1094	76	0	0	25	No	240.29	
7	SN1	10:08:55:83 12/9/20	406.29	Ctrl Logic & SEFI	240	CU	20.3	500000	1318	4	0	0	25	No	162.4	No Real Events
8	SN2	10:21:17:65 12/9/20	69.48	CB,Static	240	CU	20.3	6295	186.4	13866	0	0	25	No	2.0446	
9	SN2	10:23:02:12 12/9/20	49.59	D=A	240	CU	20.3	3927	220.6	7250	0	0	25	No	1.2755	
10	SN2	10:25:25:97 12/9/20	58.27	CB,Static	240	CU	30	3986	133.5	13471	0	0	25	No	1.9133	
11	SN2	10:26:55:22 12/9/20	58.56	D=A	240	CU	30	4036	135.9	14136	0	0	25	No	1.9373	
12	SN2	10:28:52:93 12/9/20	134.08	Ctrl Logic & SEFI	240	CU	30	1000000	12990	327	0	0	25	No	480	FLUX TOO High!
13	SN2	10:31:52:32 12/9/20	545.47	Ctrl Logic & SEFI	240	CU	30	499700	964	188	0	0	25	No	239.86	5 Events
14	SN2	10:42:21:82 12/9/20	501.31	Ctrl Logic & SEFI	240	CU	20.3	499800	1049	121	0	0	25	No	162.34	4 Events
15	SN3	10:56:39:97 12/9/20	63.88	CB,Static	240	CU	20.3	4019	101.8	17499	0	0	25	No	1.3054	
16	SN3	10:58:15:82 12/9/20	65.58	D=A	240	CU	20.3	3942	102.4	14683	0	0	25	No	1.2804	
17	SN3	11:00:28:35 12/9/20	66.46	CB,Static	240	CU	30	2660	72.1	18667	0	0	25	No	1.2768	
18	SN3	11:02:19:25 12/9/20	90.3	D=A	240	CU	30	4019	67.94	27604	0	0	25	No	1.9291	
19	SN3	11:04:52:93 12/9/20	668.61	Ctrl Logic & SEFI	240	CU	30	500000	781.3	151	0	0	25	No	240	7 Events
20	SN3	11:17:11:73 12/9/20	487.13	Ctrl Logic & SEFI	240	CU	20.3	500000	1080	487256	0	0	25	No	162.4	3 Events
21	SN4	11:29:05:16 12/9/20	112.99	CB,Static	240	CU	20.3	4000	145.7	15173	0	0	25	No	1.2992	
22	SN4	11:31:25:27 12/9/20	55.97	D=A	240	CU	20.3	4012	145.3	14265	0	0	25	No	1.3031	
23	SN4	11:33:37:37 12/9/20	63	CB,Static	240	CU	30	3952	108.2	26954	0	0	25	No	1.897	
24	SN4	11:35:07:28 12/9/20	60.2	D=A	240	CU	30	4010	115.4	28967	0	0	25	No	1.9248	
25	SN4	11:36:53:13 12/9/20	595.28	Ctrl Logic & SEFI	240	CU	30	499100	957.4	44	0	0	25	No	239.57	2 Events
26	SN4	11:48:04:31 12/9/20	439.29	Ctrl Logic & SEFI	240	CU	20.3	500000	1229	145	0	0	25	No	162.4	2 Events
27	SN5	11:59:11:88 12/9/20	65.8	CB,Static	240	CU	20.3	4032	135.6	14329	0	0	25	No	1.3096	
28	SN5	12:00:44:32 12/9/20	54.59	D=A	240	CU	20.3	3982	144	15096	0	0	25	No	1.2934	
29	SN5	12:02:55:76 12/9/20	67.83	CB,Static	240	CU	30	4060	105.7	27932	0	0	25	No	1.9488	
30	SN5	12:04:35:01 12/9/20	61.68	D=A	240	CU	30	4000	117.6	25500	0	0	25	No	1.92	
31	SN5	12:06:34:03 12/9/20	581.06	Ctrl Logic & SEFI	240	CU	30	500000	915.4	67	0	0	25	No	240	4 Events
32	SN5	12:17:29:46 12/9/20	395.73	Ctrl Logic & SEFI	240	CU	20.3	500000	1359	34	0	0	25	No	162.4	2 Events
33	SN5	14:41:40:50 12/9/20	104.08	CB,Static	240	HE	1.3	100000	1285	5566	0	0	25	No	2.08	ION is Nitrogen
34	SN4	14:47:51:74 12/9/20	85.19	CB,Static	240	HE	1.3	74050	1342	3773	0	0	25	No	1.5402	
35	SN4	14:49:43:67 12/9/20	66.51	D=A	240	HE	1.3	60000	1356	3111	0	0	25	No	1.248	
36	SN3	14:54:36:76 12/9/20	97.66	CB,Static	240	HE	1.3	60060	1331	3383	0	0	25	No	1.2492	
37	SN3	14:56:36:22 12/9/20	71.62	D=A	240	HE	1.3	59800	1342	3178	0	0	25	No	1.2438	
38	SN2	15:00:52:83 12/9/20	110.78	CB,Static	240	HE	1.3	79930	1269	2814	0	0	25	No	1.6625	
39	SN2	15:03:06:41 12/9/20	77.83	D=A	240	HE	1.3	70310	1288	2506	0	0	25	No	1.4624	
40	SN1	15:07:12:48 12/9/20	83.6	CB,Static	240	HE	1.3	69370	1132	3078	0	0	25	No	1.4429	

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41	SN1	15:09:01:50	12/9/20	97.22	D=A	240	HE	1.3	80160	1117	2813	0	0	25	No	1.6673	
42	SN5	15:13:34:26	12/9/20	68.11	D=A	240	HE	1.3	50270	1102	2785	0	0	25	No	1.0456	
43	SN1	8:04:03:77	12/10/2	103.09	CB,Static	240	XE	53.1	2061	87.1	14787	0	0	25	No	1.751	
44	SN1	8:06:11:97	12/10/2	49.11	D=A	240	XE	53.1	2001	88.1	14016	0	0	25	No	1.7	
45	SN1	8:08:00:78	12/10/2	297.47	Ctrl Logic & SEFI	240	XE	53.1	500000	2063	25	0	0	25	No	424.8	2 Events
46	SN1	8:14:07:68	12/10/2	273.59	Ctrl Logic & SEFI	240	XE	60	500000	2015	24	0	0	25	No	480	2 Events
47	SN1	8:22:59:96	12/10/2	304.39	Ctrl Logic & SEFI	240	XE	70	500000	2246	165	0	0	25	No	560	5 Events
48	SN1	8:31:14:07	12/10/2	336.03	Ctrl Logic & SEFI	240	XE	80	500000	2210	62	0	0	25	No	640	3 Events
49	SN1	8:40:54:69	12/10/2	361.96	Ctrl Logic & SEFI	240	XE	94.1	499500	2321	118	0	0	25	No	752.05	3 Events
50	SN1	8:48:17:55	12/10/2	81.29	CB,Static	240	XE	94.1	2001	89.84	18072	0	0	25	No	3.0127	
51	SN1	8:50:05:70	12/10/2	68.33	D=A	240	XE	94.1	2029	80.48	18521	0	0	25	No	3.0549	
52	SN1	9:47:25:30	12/10/2	1648.54	LatchUp	240	XE	120.9	1.000E+07	14590	1509	0	0	125	No	19344	63 Events, TL=136, TR=130, C=124, BL=122, BR
53	SN2	10:23:35:35	12/10/2	38.61	CB,Static	240	XE	53.1	1940	138.2	10794	0	0	25	No	1.6482	
54	SN2	10:24:40:38	12/10/2	46.08	D=A	240	XE	53.1	2072	149.3	12348	0	0	25	No	1.7604	
55	SN2	10:28:03:83	12/10/2	140.17	Ctrl Logic & SEFI	240	XE	53.1	501800	4261	161	0	0	25	No	426.33	3 Events
56	SN2	10:34:24:84	12/10/2	215.86	Ctrl Logic & SEFI	240	XE	93.3	498900	4197	26	0	0	25	No	744.76	2 Events
57	SN2	10:38:36:51	12/10/2	71.35	CB,Static	240	XE	93.3	2026	130.5	18588	0	0	25	No	3.0244	
58	SN2	10:40:17:74	12/10/2	52.83	D=A	240	XE	93.3	1984	117.6	18972	0	0	25	No	2.9617	
59	SN2	10:42:50:21	12/10/2	962.35	LatchUp	240	XE	120	1.000E+07	82210	6E+06	0	0	125	No	19200	64 Events, TL=133, TR=133, C=125, BL=124, BR
60	SN3	11:06:00:49	12/10/2	46.8	CB,Static	240	XE	53.1	2020	134.9	21131	0	0	25	No	1.7162	
61	SN3	11:07:09:53	12/10/2	40.97	D=A	240	XE	53.1	2000.5	124.2	17813	0	0	25	No	1.6996	
62	SN3	11:08:58:39	12/10/2	138.35	Ctrl Logic & SEFI	240	XE	53.1	498100	4587	54	0	0	25	No	423.19	4 Events
63	SN3	11:15:22:65	12/10/2	211.84	Ctrl Logic & SEFI	240	XE	93.3	501300	4270	158	0	0	25	No	748.34	7 Events
64	SN3	11:19:51:68	12/10/2	52.23	CB,Static	240	XE	93.3	1996	122.6	25215	0	0	25	No	2.9796	
65	SN3	11:21:09:89	12/10/2	50.15	D=A	240	XE	93.3	2020	118.3	24312	0	0	25	No	3.0155	
66	SN3	11:22:57:38	12/10/2	918.36	LatchUp	240	XE	120	1.036E+07	72710	3043	0	0	125	No	19891	82 events, TL=133, TR=131, C=124, BL=118, BR=
67	SN4	11:48:12:44	12/10/2	42.62	CB,Static	240	XE	53.1	2048	106.2	19156	0	0	25	No	1.74	
68	SN4	11:49:21:38	12/10/2	45.48	D=A	240	XE	53.1	2049	98.4	19700	0	0	25	No	1.7408	
69	SN4	11:51:21:61	12/10/2	138.91	Ctrl Logic & SEFI	240	XE	53.1	499300	4294	85	0	0	25	No	424.21	1 Event
70	SN4	11:57:18:35	12/10/2	610.34	Ctrl Logic & SEFI	240	XE	93.3	154000	1381	20	0	0	25	No	229.89	1 Event
71	SN4	13:31:12:17	12/10/2	55.15	CB,Static	240	XE	93.3	1985	105.8	30876	0	0	25	No	2.9632	
72	SN4	13:32:41:15	12/10/2	61.9	D=A	240	XE	93.3	2000	118.7	28635	0	0	25	No	2.9856	
73	SN4	13:35:26:64	12/10/2	714.2	LatchUp	240	XE	120	1.000E+07	53500	2088	0	0	125	No	19200	73 Events, TL=128, TR=133, C=124, BL=124, BR
74	SN5	13:55:29:72	12/10/2	288.63	CB,Static	240	XE	53.1	2070	210	20314	0	0	25	No	1.7587	
75	SN5	14:00:45:60	12/10/2	37.56	D=A	240	XE	53.1	2118	240	18842	0	0	25	No	1.7995	
76	SN5	14:03:38:67	12/10/2	173.95	Ctrl Logic & SEFI	240	XE	53.1	300000	2079	8E+06	0	0	25	No	254.88	3 Events
77	SN5	14:10:34:68	12/10/2	438.58	Ctrl Logic & SEFI	240	XE	93.3	500000	1862	277	0	0	25	No	746.4	6 Events
78	SN5	14:18:51:15	12/10/2	75.53	CB,Static	240	XE	93.3	1994	123.3	23709	0	0	25	No	2.9766	
79	SN5	14:20:37:26	12/10/2	53.5	D=A	240	XE	93.3	2021	115.5	26763	0	0	25	No	3.0169	
80	SN5	14:23:50:38	12/10/2	1295.36	LatchUp	240	XE	120	1.389E+07	45480	3279	0	0	25	No	26669	102 Events, TL=128, TR=126, C=123, BL=126, BR

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