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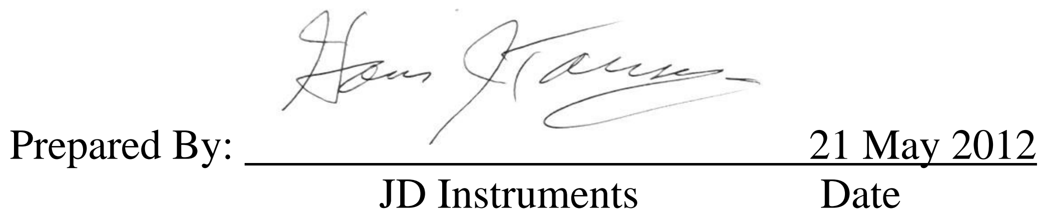
SEE-RLAT Test Report for Cypress 4Mb SRAMs (CYRS1049DV33)

Fab Lot 4126444

Date: 21 May 2012 Revision: A

Purchase Order: Cypress 2150257



Prepared By: ______________________ 21 May 2012
JD Instruments Date

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Executive Summary

Radiation Lot Acceptance Testing (RLAT) for Single Event Effects (SEE) was performed on 4Mb SRAMs (CYRS1049DV33), fab lot 4126444. Five devices were tested for SEL, SEFI, memory upset and control logic upset.

No latchups were observed on any device even when heated to 125^0C and irradiated at an LET of 120 (MeV*cm^2)/mg to a total fluence of 10^7 ions/cm^2.

No SEFIs were ever observed on any device over the course of the entire test.

Memory upsets were well behaved and all parts had very similar cross-sections. Multi-cell upsets were observed at higher LETs but, due to the physical arrangements of memory cells, a single ion strike never caused multiple upsets in the bits accessed by a read to any single address.

There was no discernable pattern sensitivity to memory upset cross-section.

Upset behavior at retention power level (Vcc = 2.0V) was not discernibly different from that seen at low-nominal power level (Vcc = 3.0V).

Testing was done in compliance with ASTM F1192, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices" and also in compliance with EIA/JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation".

1.0 Test Overview

Single Event Effects (SEE) testing was performed on Cypress Semiconductor 4Mb SRAMs (CYRS1049DV33), fab lot 4126444 on 16/17 May, 2012 at the Texas A&M University Cyclotron facility. Testing was performed by H. Jake Tausch of JD Instruments and Helmut Puchner of Cypress Semiconductor.

These devices have the architecture shown in Figure 1. This part is a pure static RAM with a power down function to insure low current consumption when it is not enabled.

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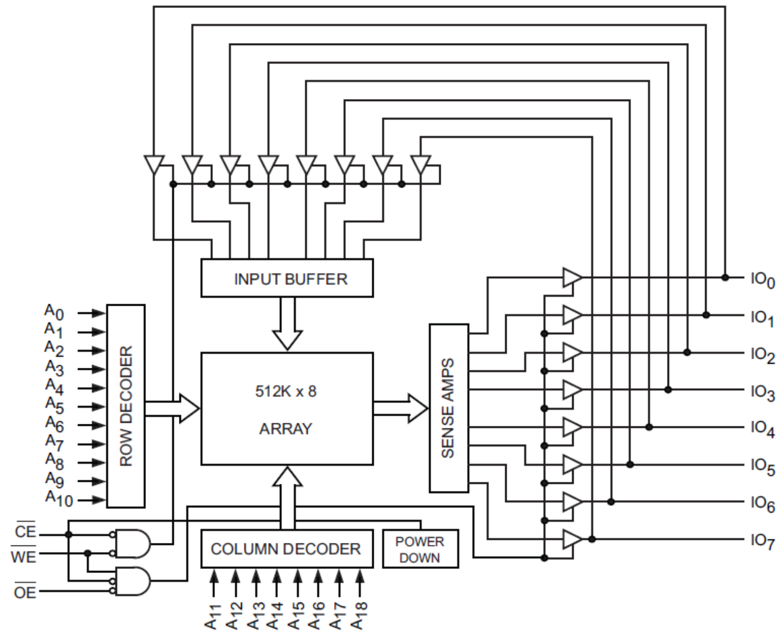

Figure 1. Functional Diagram for CYRS1049DV33

Devices were provided in 36 pin ceramic flat packages with pinout as shown in figure 2.

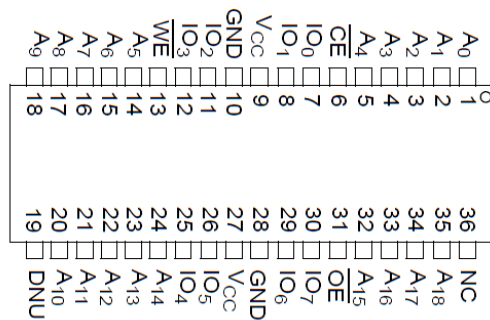

Figure 2. 36 Pin Flat Package Pinout

Tests was performed using an Algorithmic Test Vector (ATV) system from JD Instruments as shown in figure 3. This is a portable system containing many of the features found in larger main-frame test systems. For this application it is particularly useful in that it collects data in both primitive error logs and also records summary results in spreadsheet form, simplifying on-site understanding of results as the test proceeds.

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Figure 3. ATV Test System used for TID Testing

All testing was done with one device at a time inserted into a test card mounted on the ATV test head. Circuit schematics for the test card are shown in attachment 1. Figure 4 shows an overview of the test board.

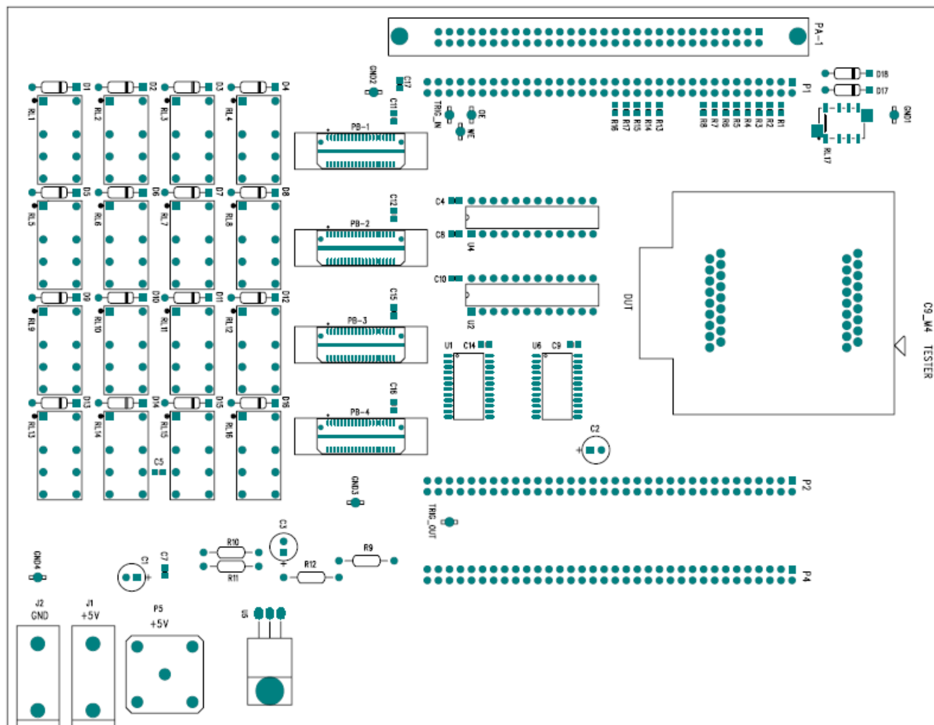

Figure 4. SEE Test Board for CYRS1049DV33

Testing was done in compliance with ASTM F1192, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices" and also in compliance with EIA/JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation".

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Five types of tests were performed:

1. Static Bit Upset at Vcc = nominal-low (3.0V)
    a. Checkerboard Pattern
    b. Data at each address = Lower 8 bits of address (D=A)
2. Static Bit Upset when Vcc = Retention Voltage (2.0V)
    a. Checkerboard Pattern
    b. Data at each address = Lower 8 bits of address (D=A)
3. Dynamic Test of Control Logic
4. Latchup
5. Single Event Functional Interrupt (SEFI)

Five parts were measured at every condition. Dynamic and SEL tests were performed with the parts being continuously clocked at 15MHz.

Three ion species were used for this test. Krypton (^{84}Kr) was used for LETs between 20.6 and 40 (MeV*cm^2)/mg, Nitrogen (^{14}N) for LETs of 1.3 and 2.6 (MeV*cm^2)/mg, and Xenon (^{129}Xe) for LETs between 53 and 60 (MeV*cm^2)/mg. Xenon was also used to generate 120 (MeV*cm^2)/mg equivalent ions by tilting the DUTs to a 60^0 degree angle and degrading the Xenon beam to an LET of 60 (MeV*cm^2)/mg.

Krypton was obtained using the 25 MeV SEE beam. The other 2 ions came from the 15 MeV SEE beam. Parts were irradiated in air at a distance of 30mm from the aramica window of the source. Figures 5 and 6 show the range vs. LET for various ions available with the 15 MeV beam. The minimum LET for Krypton was 20.6 (MeV*cm^2)/mg instead of the 28 (MeV*cm^2)/mg shown in these plots since it was generated with the 25MeV beam. Note that all ions used had a range >30u in silicon at the LETs used during this test.

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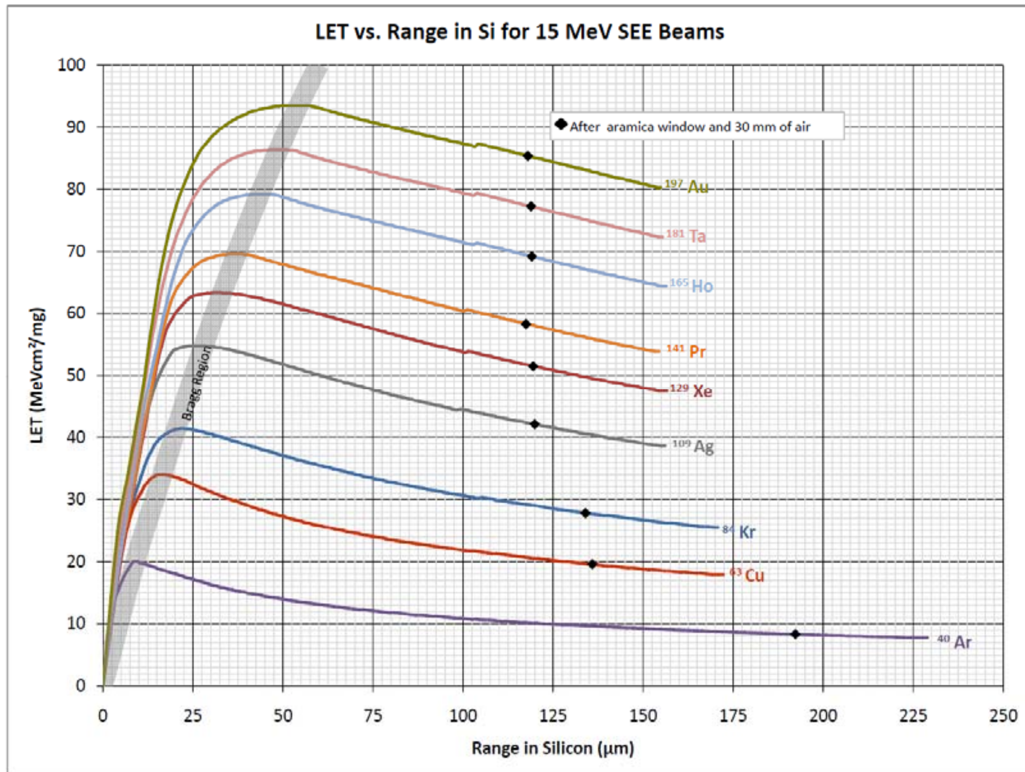

Figure 5. Ion Range vs. LET, Various Ions, 15 MeV beam, Texas A&M Cyclotron

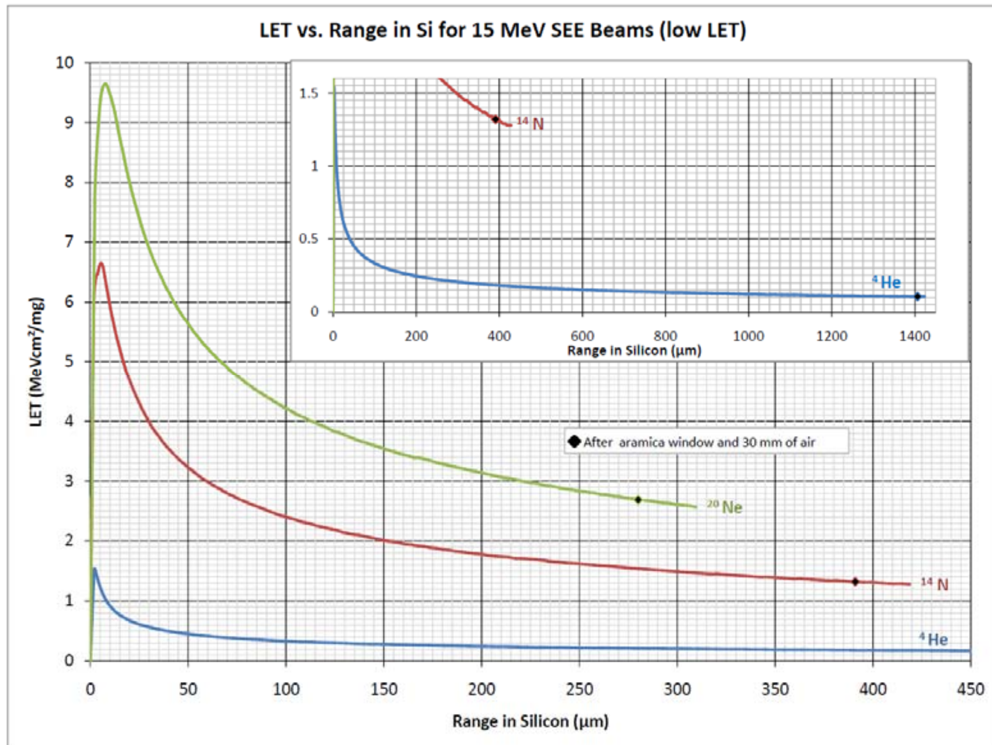

Figure 6. Ion Range vs. LET, low LET Ions, 15 MeV beam, Texas A&M Cyclotron

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Figure 7 shows a cross-section for devices manufactured at this technology node. Note that all parts were manufactured using 3u epi wafers and that the total thickness of all overlayers was 5.5u. Any sensitive nodes must be within the 3u silicon layer and underneath the overlayers. Thus, ions must have a penetration depth of at least 8.5u to insure they reach all sensitive nodes. Since the actual range for the all ions is >30u then they are sufficient for this test.

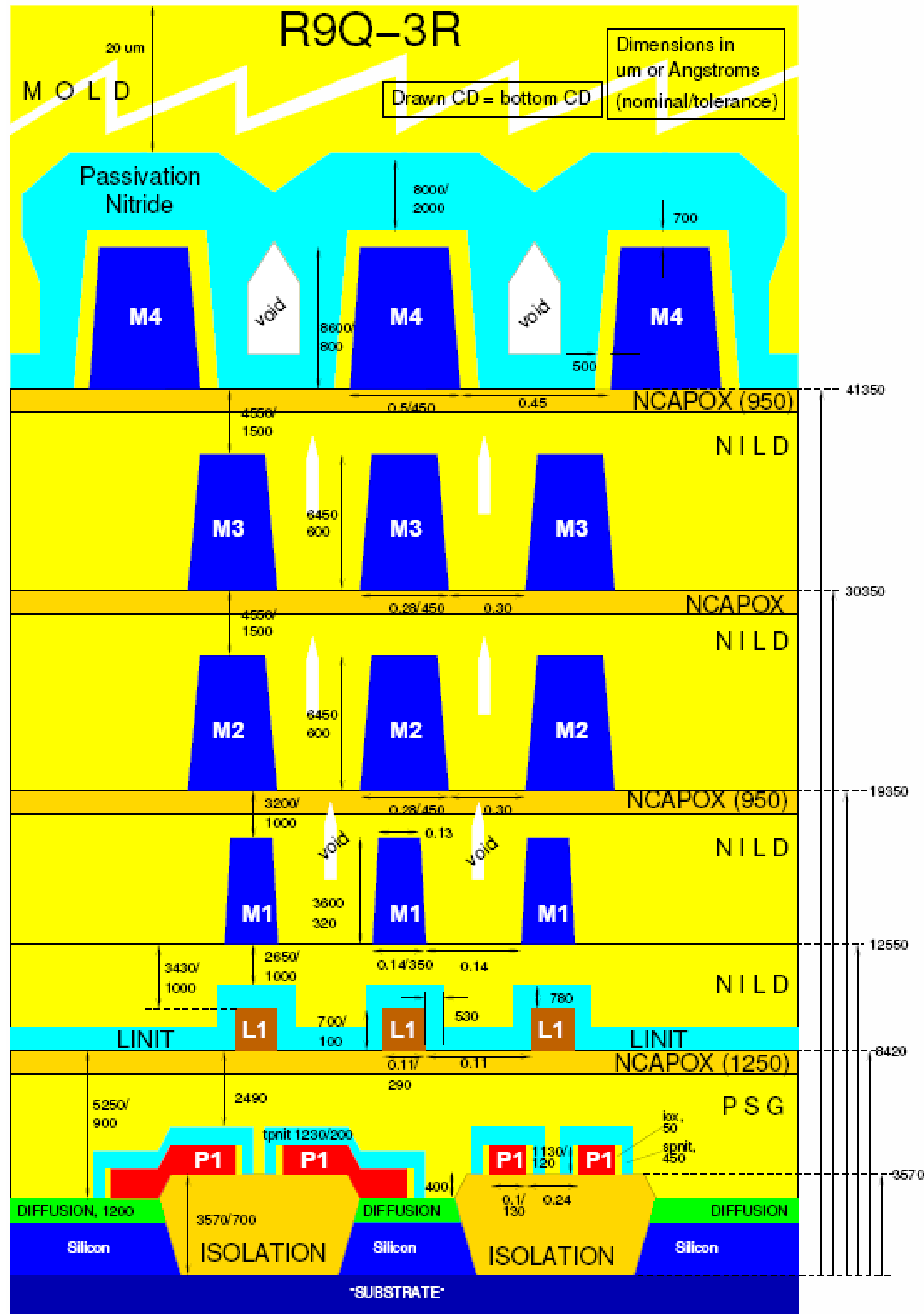

Figure 7. Device Cross-section in Angstroms

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Accumulated total dose was tracked for each DUT over the course of testing (see Attachment 2. Run Log). Dose was calculated in the Run Log as LET * Fluence * 1.602E-5 and this agreed exactly with the dose as reported by the TAMU facility in run sheets.

Since all 5 DUTs were subjected to the same test sequence their resultant accumulated dose was very similar, ranging from 21.7K rad(Si) to 22.8K rad(Si). The variation in dose was due to some test exposures being performed more than once on some parts.

These parts have previously been tested for total ionizing dose (TID) effects using ^{60}CO and have shown no sensitivity below doses of several hundred thousand rad(Si). The dose accumulated during these tests is not considered significant.

2.0 Latch-Up

These parts were tested for single event latch-up (SEL) at a single “worst case” condition of LET=120 (MeV*cm^2)/mg, Temp=125^0C and Vdd 3.6V. Latchup would be indicated by a sudden increase in Idd. Also, a pattern was repeatedly written/read to the entire memory during the SEL exposure runs so any occurrences of SEFI (Single Event Functional Interrupt) would have been detected (see section 5.0 for further discussion of SEFI test sequence).

The LET value of 120 (MeV*cm^2)/mg was achieved by degrading the Xe ion to a normal incident LET of 60 (MeV*cm^2)/mg and irradiating the DUT at an angle of 60 degrees.

A DUT temprature of 125^0C was achieved by placing strip heaters underneath the carrier card of each DUT and heating the carrier card/DUT from the back side. An infrared thermometer was used to measure the actual die temperature. The infrared thermometer had a calibrated accuracy of +/- 1^0C (see figure 8).

Figure 8. Infrared Thermometer

Each of the 5 DUTs were irradiated to 1E7 ions/cm^2 and none of them exhibited any increase in power supply currents.

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Combining results from all SEL runs, 5 devices were exposed a total of 5.0E7 ions/cm^2 at an LET of 120 (MeV*cm^2)/mg and temperature of 125^0C with no evidence of latchup. The conclusion is that these parts are not susceptible to latchup from heavy ion irradiation. Further, no SEFI failures were ever detected during this elevated temperature, high LET testing.

3.0 Static Memory Upsets

Static upset behavior was determined by loading parts with a fixed pattern, irradiating to some fluence and reading the pattern back. Two patterns were used: checkerboard and "D=A". The D=A pattern is one in which the data at any given address is the same as the lower 8 bits of the address. Static upset tests were performed with parts biased to their low-normal operating level (3.0V) and also at a reduced Vcc level (retention mode, Vcc = 2.0V).

3.1 Multi-Cell Upset Pattern

These parts are designed so that memory cells for any given bit position are "tiled". Thus, for example, all cells containing information that will be read out in the logical bit "0" position will be co-located in one physical array and this will be separated from other "tiles". The result is that a multi-cell upset event from one heavy ion strike will present itself, when the part is read, as multiple upsets, all at the same bit position, but at different logical addresses. Examples of this pattern are shown below in figure 9 where portions of recorded error logs are shown for a series of static tests with increasing LET values.

ADDR	DATA EXP	ERR	#BIT
0xddc	10101010	-----F--	1
0x21f8	10101010	-F------	1
0x2263	01010101	F-------	1
0x2fa5	01010101	---F----	1
0xa594	10101010	--F-----	1
0xa95b	01010101	-----F--	1
0xa95f	01010101	-----F--	1
0xbab4	10101010	--F-----	1
0x2365d	01010101	--F-----	1
0x246de	10101010	F-------	1
0x25a75	01010101	-------F	1
0x26e2f	01010101	---F----	1
0x27c93	01010101	------F-	1
0x28d4d	01010101	----F---	1
0x34c60	10101010	F-------	1
0x393c9	01010101	-----F--	1
0x39411	01010101	-------F	1
0x39d49	01010101	-----F--	1
0x3aae2	10101010	-F------	1
0x3cee5	01010101	-F------	1
0x410be	10101010	----F---	1
0x4409e	10101010	-------F	1
0x464a1	01010101	-----F--	1
0x46614	10101010	F-------	1
0x4ac18	10101010	-----F--	1
0x4beae	10101010	F-------	1
0x4d75a	10101010	F-------	1
0x4e5ff	01010101	-F------	1
0x50692	10101010	----F---	1
0x52353	01010101	----F---	1
0x561ee	10101010	------F-	1
0x58ba6	10101010	------F-	1

Fig 9.1, LET = 1.3

ADDR	DATA EXP	ERR	#BIT
0x16ad7	01010101	--F-----	1
0x17c24	10101010	------F-	1
0x21a60	10101010	--F-----	1
0x37d53	01010101	---F----	1
0x37d97	01010101	---F----	1
0x3be50	10101010	------F-	1
0x3be54	10101010	------F-	1
0x3fda9	01010101	F-------	1
0x3fdad	01010101	F-------	1
0x3fded	01010101	F-------	1
0x45c8d	01010101	----F---	1
0x45c91	01010101	----F---	1
0x470ac	10101010	-----F--	1
0x4af11	01010101	----F---	1
0x4af15	01010101	----F---	1
0x4af55	01010101	----F---	1
0x4fbec	10101010	------F-	1
0x50642	10101010	--F-----	1
0x5065a	10101010	---F----	1
0x525a5	01010101	---F----	1
0x584bb	01010101	--F-----	1
0x584bf	01010101	--F-----	1
0x584fb	01010101	--F-----	1
0x584ff	01010101	--F-----	1
0x5c616	10101010	----F---	1
0x5c652	10101010	----F---	1
0x5c656	10101010	----F---	1
0x68de4	10101010	---F----	1
0x68de8	10101010	---F----	1
0x6c852	10101010	-------F	1
0x6c856	10101010	-------F	1
0x6e347	01010101	--F-----	1

Fig 9.2, LET = 20.6

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ADDR	DATA		
	EXP	ERR	#BIT
0x10e89	01010101	---F----	1
0x10e8d	01010101	---F----	1
0x10ec9	01010101	---F----	1
0x10ecd	01010101	---F----	1
0x10f0d	01010101	---F----	1
0x10f89	01010101	---F----	1
0x10f8d	01010101	---F----	1
0x12188	10101010	----F---	1
0x121cc	10101010	----F---	1
0x17f74	10101010	--F-----	1
0x17fb4	10101010	--F-----	1
0x17ff0	10101010	--F-----	1
0x17ff4	10101010	--F-----	1
0x185f9	01010101	-------F	1
0x185fd	01010101	-------F	1
0x18679	01010101	-------F	1
0x186b9	01010101	-------F	1
0x186bd	01010101	-------F	1
0x186f9	01010101	-------F	1
0x186fd	01010101	-------F	1
0x18739	01010101	-------F	1
0x1a5fb	01010101	--F-----	1
0x1a5ff	01010101	--F-----	1
0x1a627	01010101	-F------	1
0x1a63b	01010101	--F-----	1
0x1a63f	01010101	--F-----	1
0x1a663	01010101	-F------	1
0x1a667	01010101	-F------	1
0x1a67b	01010101	--F-----	1
0x1a67f	01010101	--F-----	1
0x1a6bb	01010101	--F-----	1
0x1a6fb	01010101	--F-----	1

Fig 9.3, LET = 53.1

ADDR	DATA		
	EXP	ERR	#BIT
0x1022	10101010	-------F	1
0x1062	10101010	-------F	1
0x1066	10101010	-------F	1
0x10a2	10101010	-------F	1
0x10e6	10101010	-------F	1
0x1122	10101010	-------F	1
0x1166	10101010	-------F	1
0x11a2	10101010	-------F	1
0x1222	10101010	-------F	1
0x1226	10101010	-------F	1
0x1266	10101010	-------F	1
0x1c27	01010101	---F----	1
0x1ca3	01010101	---F----	1
0x5a67	01010101	---F----	1
0x5aa3	01010101	---F----	1
0x5aa7	01010101	---F----	1
0x5b27	01010101	---F----	1
0x5b67	01010101	---F----	1
0x5ba3	01010101	---F----	1
0x5ba7	01010101	---F----	1
0x5be7	01010101	---F----	1
0xb2cb	01010101	----F---	1
0xb2cf	01010101	----F---	1
0xb30b	01010101	----F---	1
0xb30f	01010101	----F---	1
0xb313	01010101	----F---	1
0xb34b	01010101	----F---	1
0xb34f	01010101	----F---	1
0xb353	01010101	----F---	1
0xb357	01010101	----F---	1
0xb397	01010101	----F---	1
0xb3cb	01010101	----F---	1

Fig 9.4, LET = 120

Figure 9. Multi-Cell Memory Upset Patterns With Increasing LET ions

The multi-cell upset patterns are clearly more distinct at higher LETs.

One interesting feature of the error logs recorded by the ATV test system is that the information for each failing address includes the logical address, expected pattern, pattern of failing bits and also a count of the number of bits that failed at that address ("#Bit" column in the error log). From this it is easily seen that, even though higher LET ions caused multiple cells to upset, there were no instances of multiple bits failing at any address.

In fact, for all static testing performed on these parts there was never an instance where 2 or more bits were upset at any address. It should be noted that all static tests were designed to limit the total number of bit upsets from any one exposure to 20,000 or less. This limited the probability of multiple bits being upset at any address from separate, random ion strikes. Thus, the conclusion is that multi-cell upsets from any single ion strike will never cause a multi-bit failure at any address and that these memories are well suited for use with EDAC.

3.2 Memory Upset – Normal Operation

Upset testing on these parts for normal operation was performed with Vdd at the lowest spec sheet level of 3.0V. Static upset results for the checkerboard pattern are plotted in figure 10 along with a Weibull fit to the data. Note that there is no clear saturation value to the cross-section in the classical sense, even with LETs as high as 120 MeV/(mg/cm^2). This is because of the multi-cell upset phenomena described above. Nonetheless the Weibull curve fits the experimental data nicely and so can be used to accurately predict the behavior of these parts in various environments.

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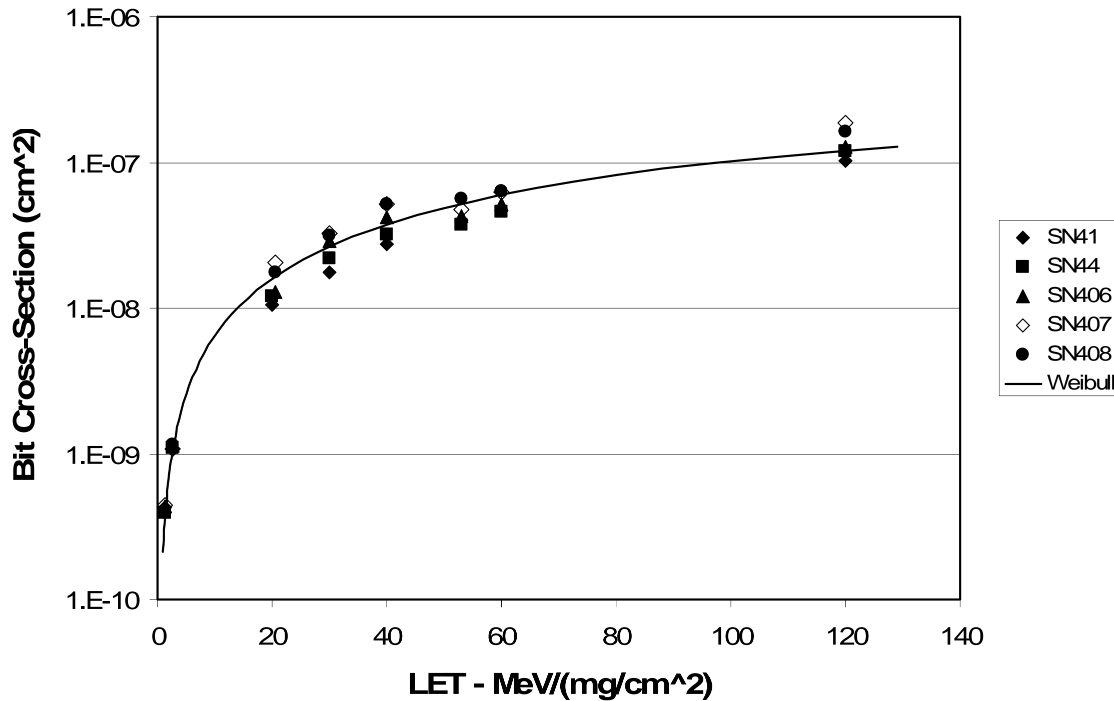

Figure 10. Static Upset Cross-Sections, Checkerboard Pattern

Weibull parameters for the curve shown above are as follows:

OnSet LET = 0. 3 MeV/(mg/(cm^2))
Width = 150
Exponent = 1.3
Saturated X-Section = 23 u^2 = 2.3e-7 cm^2

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3.3 Pattern Sensitivity

Pattern sensitivity was investigated using a limited number of parts. Figure 11 repeats all the CB data points shown previously and adds data points where the test pattern was D=A. For clarity all CB data points are plotted as empty circles and D=A data points are shown as solid symbols. There was no discernable pattern sensitivity for these parts.

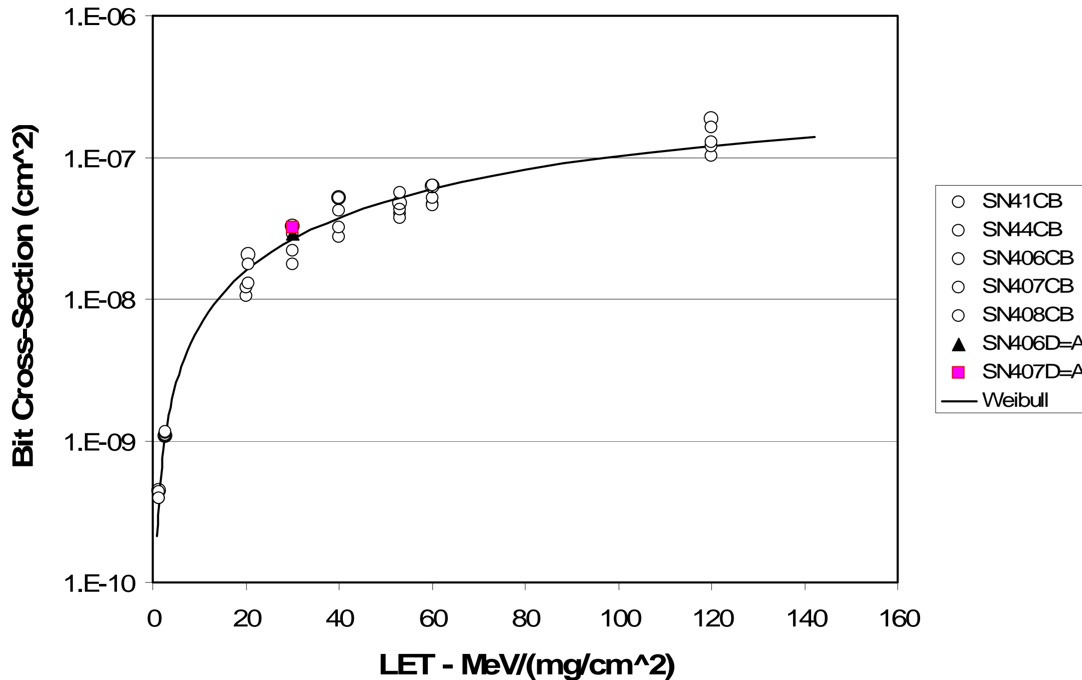

Figure 11. Static Upset Cross-Sections, Checkerboard and D=A Patterns

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3.4 Data Retention Cross-Section

Figure 12 compares normal upset measurements with data when the parts were put into "data retention" conditions (Vcc = 2.0V). Again the CB data points for normal bias are shown here as empty circles and data retention results are plotted as various solid symbols. There may have been a slight increase in upset cross-section when the parts were in retention mode, but not enough to clearly affect the cross-section curve.

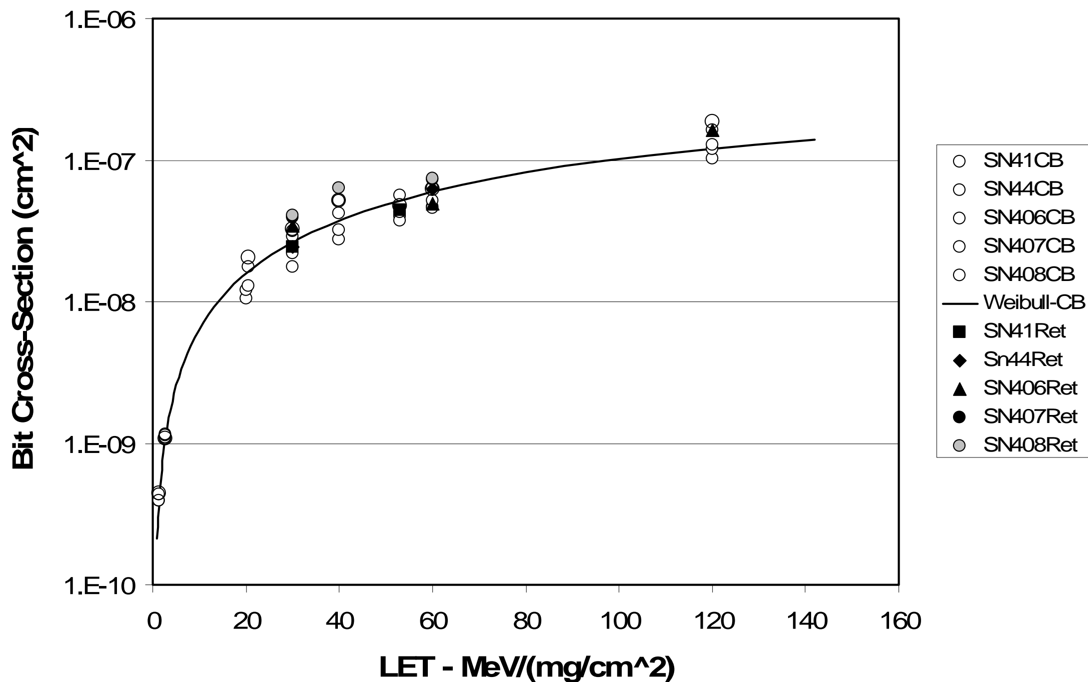

Figure 12. Static Upset Cross-Sections, Vcc = 3.0V (Normal) and 2.0V (Retention)

4.0 Control Circuitry Upsets

Control circuitry for these parts includes such things as address decoding logic, write strobes, sense amps, data latches, clock trees, etc. Special dynamic tests were performed to detect upsets in the control circuitry of these parts.

The dynamic test consisted of writing to a burst of 64 addresses and then immediately reading from those same addresses. This was started at address "0" and continued through the entire address space of the DUT. The pattern used for this test was "D=A" with a clock frequency of 15MHz. Since the data pattern was present for such a short time in memory (~5uS between write/read of any address) then very few upsets came from memory cell upsets. Occasionally an upset would occur that had an entirely different "signature" than a normal memory upset. These were considered to be upsets in the control circuitry as defined above.

Figure 13 shows a complete error log from one control logic test. In this log the "Test#" would increment by 1 every time a pass was made through the entire memory. For instance, in this error log the entire memory was written/read 46 times between test# 15 and test# 61 with no

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errors. The elapsed time for these 46 tests was ~1 minute. In test# 15, 3 bit errors were detected that look like they were caused by one ion strike (multi-cell upset as described above). Over the course of the test the part was exposed to a total of 1E6 ions/cm^2 and this took ~10 minutes. There were 2 error patterns that were distinctly different from all others in this log and these are highlighted. The conclusion was that there were 2 control logic errors during this test.

Test#	Time	Date	Total Errs	ADDR	DATA EXP	ERR	#BIT
15	16:56:54.751	5/16/2012	3	0x102400	01010101	F-------	1
				0x102404	01010101	F-------	1
				0x102408	01010101	F-------	1
61	16:58:04.619	5/16/2012	2	0x1d1f9	10101010	----F---	1
				0x1d1fd	10101010	----F---	1
91	16:58:50.023	5/16/2012	1	0x1cfbb9	10101010	---F----	1
94	16:58:54.499	5/16/2012	3	0x1247b9	10101010	---F----	1
				0x1247bd	10101010	---F----	1
				0x1247fd	10101010	---F----	1
146	17:00:13.374	5/16/2012	3	0xab973	10101010	-F------	1
				0x40974	01010101	----F---	1
				0xa9264	01010101	F-------	1
156	17:00:28.684	5/16/2012	1	0xf4867	10101010	---F----	1
158	17:00:31.781	5/16/2012	2	0xa6246	01010101	----F---	1
				0xa625e	01010101	-----F--	1
183	17:01:09.740	5/16/2012	1	0x12d6a0	01010101	--F-----	1
218	17:02:02.809	5/16/2012	3	0x1792b0	01010101	F-------	1
				0x1792b4	01010101	F-------	1
				0x10919e	01010101	F-F-F-F-	4
229	17:02:19.668	5/16/2012	2	0xc9abf	10101010	-----F--	1
				0xc9ac0	01010101	FFFFFFFF	8
237	17:02:31.663	5/16/2012	1	0x87aef	10101010	------F-	1
274	17:03:27.751	5/16/2012	2	0x4d30	01010101	------F-	1
				0x4d34	01010101	------F-	1
277	17:03:32.307	5/16/2012	1	0x5848b	10101010	-F------	1
282	17:03:39.837	5/16/2012	1	0x1fe41d	10101010	----F---	1
292	17:03:55.003	5/16/2012	1	0x1775e9	10101010	---F----	1
293	17:03:56.492	5/16/2012	1	0x17141c	01010101	--F-----	1
299	17:04:05.557	5/16/2012	1	0x81bfa	01010101	--F-----	1
310	17:04:22.184	5/16/2012	1	0x1f229d	10101010	-F------	1

Figure 13. Control Logic Memory Upsets, Run #12,
LET = 30, Fluence = 1e6 ions/cm^2

Even though every control logic test exposed a part to 1e6 ions/cm^2 there were very few control logic upsets. Table 1 summarizes the results for all control logic tests performed on these parts.

	Number of Control Errors							
LET	SN41	SN44	SN406	SN407	SN408	Total Errs	Fluence	Cross-Section
20.6	0	0	0	0	0	0.5*	5.00E+06	1.00E-07
30	0	1	2	2	1	6	5.00E+06	1.20E-06
40	1	0	2	2	2	7	5.00E+06	1.40E-06
60	3					3	1.00E+06	3.00E-06
120		4	4	4	2	14	4.00E+06	3.50E-06

* Use 0.5 errors instead of 0. Actual cross-section may be lower, but can't be determined by this limited data

Table 1. Summary of Control Logic Test Results

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If all upsets are added together then an upset cross-section curve can be plotted for control logic upsets as shown in figure 14.

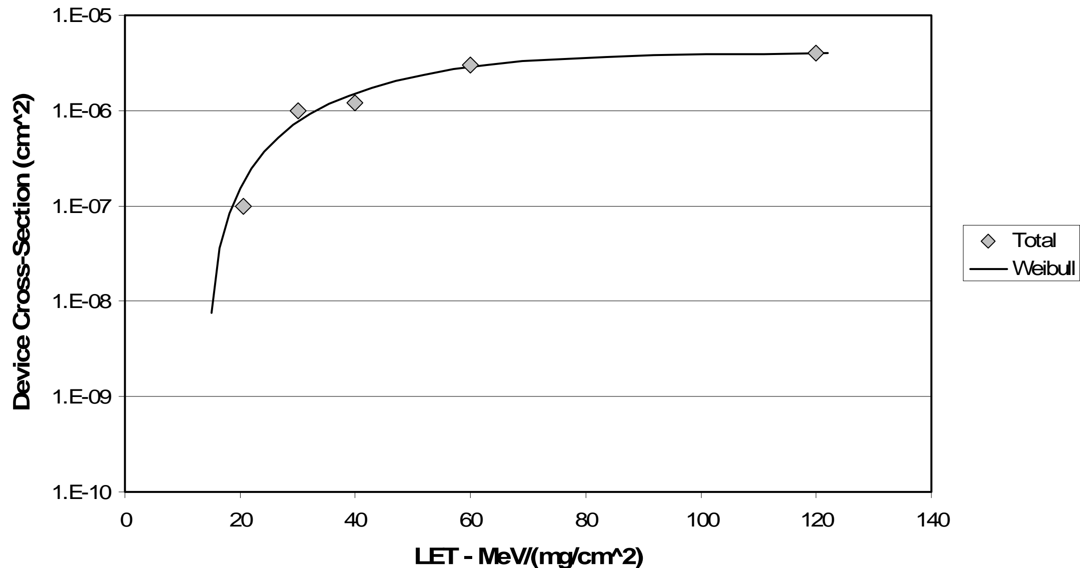

Figure 14. Control Logic Device Level Cross-Sections

Figure 14 also shows a Weibull curve fitted to the control upset data. Weibull parameters for this curve are as follows:

OnSet LET = 14 MeV/(mg/(cm^2))
Width = 40
Exponent = 1.7
Saturated X-Section = 400 u^2 = 4.0e-6 cm^2

Note that figure 14 shows the device level cross-section as opposed to the bit level cross-sections shown in all previous plots. When considered at a device level the saturated cross-section for control logic errors is ~6 orders of magnitude smaller than that for memory upsets. The threshold upset level is also quite a bit higher (14 MeV/(mg/(cm^2)) vs. 0. 3 MeV/(mg/(cm^2))). Taken together, the probability of a control logic upset is very small.

5.0 SEFI Behaviour

A Single Event Functional Interrupt (SEFI) is an upset in some portion of the device which causes continuing device failure until the device is reset or power cycled. No SEFIs were ever observed on any of these devices over the course of the entire test. Even when the devices were being tested for SEL they were being constantly exercised with the control logic upset algorithm (Write/Read, D=A, 64 address burst) to insure that they were functioning correctly.

Since no SEFIs were ever observed over the course of this test then we can combine the fluences from all devices and say that no SEFIs were observed when irradiated with various ions that had a combined fluence of 7.31E7 ions/cm^2.

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6.0 Calculated Upset Rates

The Weibull fit for these devices had the following values:

Memory Upsets (bit):

OnSet LET = 0. 3 MeV/(mg/(cm^2))
Width = 150
Exponent = 1.3
Saturated X-Section = 23 u^2 = 2.3e-7 cm^2

Control Upsets (device):

OnSet LET = 14 MeV/(mg/(cm^2))
Width = 40
Exponent = 1.7
Saturated X-Section = 400 u^2 = 4.0e-6 cm^2

Using these values the following device upset rates were calculated for various orbits using CREME96.

	SEUs/Device/Day	CTRL Upsets/Device/Day
Space Station, Solar Minimum	8.23E-02	3.20E-08
Space Station, Worst Day (Flare)	2.88E+01	3.74E-05
Geosynchronous, Solar Minimum	7.03E-01	7.10E-07
Geosynchronous, Worst Day (Flare)	2.64E+03	6.13E-04

Figure 15. Upset Rates for Various Orbits

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8.0 Pre/Post Radiation Characterization

All 5 DUTs and 2 reference devices were characterized before and after SEE testing to insure that no parameters changed as a result of this testing. Results of these characterization tests are shown in figure 16. Note that DUTs with serial numbers 305 and 405 were the reference devices. No part showed any detectable change as a result of this SEE testing. Irradiated devices were tested within 1 hour after the conclusion of SEE testing.

DUT	Time Stamp	Func Errs	Retention Errs	Idd Retention	Idd CB	Idd CB*	Idd D=A	Vih	Vil	Voh	Vol	Iih	Iil	Ioz-h	Ioz-l
41 Pre	14:09:06:36 5/12/2012	0	0	1.72E-02	2.99E-02	2.99E-02	2.98E-02	1.62E+00	1.29E+00	3.02E+00	1.75E-01	4.11E-11	-2.46E-11	-6.15E-11	-2.62E-10
44 Pre	14:11:41:96 5/12/2012	0	0	1.69E-02	3.14E-02	3.15E-02	3.14E-02	1.62E+00	1.34E+00	3.01E+00	1.76E-01	6.21E-11	-1.03E-11	-3.46E-11	-1.77E-10
406 Pre	14:12:56:22 5/12/2012	0	0	1.60E-02	2.97E-02	2.98E-02	2.99E-02	1.52E+00	1.29E+00	3.02E+00	1.75E-01	6.02E-11	-1.20E-11	-5.46E-11	-2.14E-10
407 Pre	14:14:09:65 5/12/2012	0	0	1.55E-02	3.06E-02	3.05E-02	3.04E-02	1.62E+00	1.29E+00	3.01E+00	1.73E-01	5.77E-11	-1.21E-11	-5.63E-11	-2.48E-10
408 Pre	14:15:01:78 5/12/2012	0	0	1.57E-02	3.14E-02	3.14E-02	3.14E-02	1.62E+00	1.34E+00	3.02E+00	1.74E-01	5.90E-11	-1.21E-11	-5.62E-11	-2.92E-10
305 Pre	14:15:51:16 5/12/2012	0	0	1.63E-02	3.00E-02	2.99E-02	2.98E-02	1.57E+00	1.29E+00	3.00E+00	1.77E-01	6.08E-11	-1.19E-11	-5.08E-11	-1.99E-10
405 Pre	14:16:36:09 5/12/2012	0	0	1.55E-02	3.08E-02	3.09E-02	3.08E-02	1.66E+00	1.34E+00	3.01E+00	1.72E-01	6.18E-11	-1.17E-11	-5.31E-11	-2.58E-10
41 Post	6:50:07:00 5/17/2012	0	0	1.71E-02	2.99E-02	2.98E-02	2.99E-02	1.62E+00	1.29E+00	3.02E+00	1.81E-01	4.11E-11	-3.44E-11	-7.54E-11	-2.49E-10
44 Post	6:52:36:51 5/17/2012	0	0	1.67E-02	3.17E-02	3.17E-02	3.17E-02	1.66E+00	1.34E+00	3.01E+00	1.81E-01	6.21E-11	-2.22E-11	-4.75E-11	-1.72E-10
406 Post	6:55:20:41 5/17/2012	0	0	1.58E-02	2.97E-02	2.96E-02	2.97E-02	1.57E+00	1.24E+00	3.02E+00	1.81E-01	6.02E-11	-1.83E-11	-6.74E-11	-2.07E-10
407 Post	6:56:30:71 5/17/2012	0	0	1.54E-02	3.05E-02	3.04E-02	3.03E-02	1.62E+00	1.29E+00	3.02E+00	1.79E-01	5.77E-11	-2.04E-11	-6.58E-11	-2.34E-10
408 Post	6:57:57:11 5/17/2012	0	0	1.56E-02	3.17E-02	3.15E-02	3.15E-02	1.62E+00	1.34E+00	3.02E+00	1.80E-01	5.90E-11	-2.03E-11	-6.70E-11	-2.69E-10
305 Post	6:59:11:70 5/17/2012	0	0	1.62E-02	3.00E-02	2.99E-02	2.99E-02	1.57E+00	1.29E+00	3.01E+00	1.85E-01	6.08E-11	-2.28E-11	-6.61E-11	-1.95E-10
405 Post	7:00:40:46 5/17/2012	0	0	1.53E-02	3.11E-02	3.11E-02	3.09E-02	1.62E+00	1.29E+00	3.01E+00	1.80E-01	6.08E-11	-2.13E-11	-6.67E-11	-2.46E-10

Figure 16. Pre and Post Irradiation DUT Parametrics

8.0 Conclusions

All parts all behaved very similarly when exposed to heavy ion radiation. Upset behavior was simple and repeatable. None of the parts latched up and none of the parts showed SEFI behavior. No single ion strike ever caused multiple bit upsets at one logical address so these memories should behave very well when used with a simple EDAC scheme such as Hamming.

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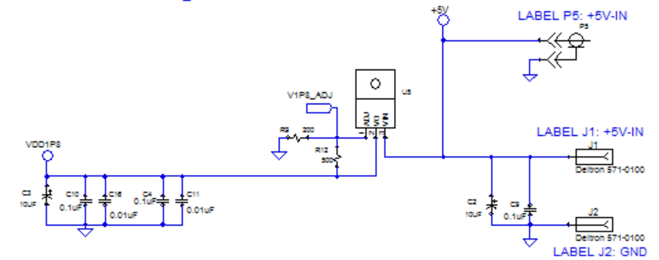
Attachment 1. Test Board Schematic

NOTE:P1, P2,P4 CONNECTOR PINS SHOWN FROM TOP VIEW AND IS THE WAY THE SIGNALS SHOULD BE ROUTED. CONNECTOR WILL ACTUALLY BE MOUNTED ON UNDER SIDE TO MATE WITH CONNECTORS ON MOTHERBOARD. ADD APPROPRIATE ASSEMBLY NOTES.

NOTE: EN_ALL is High Voltage Strobe from TVP set to 2.5V to accomodate Diode Drop

NOTE: LAYOUT U5 WITH CLEARANCE FOR HEATSINKS

NOTE: USE HEAVY TRACES FOR VDD1P8, +5V AND DUT_VDD



C9_4M
MULTI-SITE TEST BOARD
Nov 2011

JD INSTRUMENTS LLC

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Attachment 2. Run Log

RUN#	DUT	Start Time	Duration (Seconds)	Test	Ion	LET	Fluence	Flux	#Errs	#SEFI	#Pwr Cycles	Temp	High Current Latch?	Dose	Comment
1	SN41	16:14:34:99 5/16	79.21	CB,Static	Kr	50	7460	120	508	0	0	25	No	5.968	
2	Sn407	16:20:32:34 5/16	70.69	CB,Static	Kr	30	2418	48.6	751	0	0	25	No	1.1606	
3	Sn407	16:27:05:22 5/16	86.62	CB,Static	Kr	20.6	7831	123.7	671	0	0	25	No	2.5811	
4	Sn407	16:31:42:15 5/16	35.49	CB,Static	Kr	40	0.001	123.7	346	0	0	25	No	6E-07	Beam count too low ... Op had to adjust Voltage on Detec
5	Sn407	16:35:11:04 5/16	80.3	CB,Static	Kr	40	5372	87.6	1159	0	0	25	No	3.4381	
6	Sn407	16:38:50:74 5/16	104.8	CB,Static	Kr	30	7507	86.2	1027	0	0	25	No	3.6034	
7	Sn407	16:43:46:02 5/16	71.51	All 1s, Static	Kr	30	10000	194.3	1210	0	0	25	No	4.8	
8	Sn407	16:45:38:62 5/16	67.88	D=A, Static	Kr	30	7883	146.8	1068	0	0	25	No	3.7838	
9	Sn407	16:47:32:20 5/16	82.61	CB, Retention	Kr	30	6944	116.8	1140	0	0	25	No	3.3331	
10	Sn407	16:49:21:72 5/16	86.56	All 1s, Retention	Kr	30	6948	110.2	1055	0	0	25	No	3.335	
11	Sn407	16:51:27:34 5/16	82.93	D=A, Retention	Kr	30	6735	119.2	1113	0	0	25	No	3.2328	
12	Sn407	16:56:33:05 5/16	499.38	Ctrl Logic	Kr	30	1000000	2078	21	0	0	25	No	480	2 Ctrl Logic Errors
13	Sn407	17:10:16:33 5/16	596.82	Ctrl Logic	Kr	40	1000000	1720	41	0	0	25	No	640	2 Ctrl Logic Errors
14	Sn407	17:23:57:47 5/16	541.51	Ctrl Logic	Kr	20.6	1000000	2620	6	0	0	25	No	329.6	0 Ctrl Logic Errors
15	SN406	17:40:35:24 5/16	441.44	Ctrl Logic	Kr	20.6	1000000	2622	6	0	0	25	No	329.6	0 Ctrl Logic Errors
16	SN406	17:50:11:63 5/16	461.1	Ctrl Logic	Kr	30	1000000	2246	17	0	0	25	No	480	1 Ctrl Logic Error
17	SN406	17:59:06:66 5/16	553.16	Ctrl Logic	Kr	40	1000000	1859	45	0	0	25	No	640	0 Ctrl Logic Errors
18	SN406	18:10:24:22 5/16	62.62	CB,Static	Kr	40	6439	130.6	1135	0	0	25	No	4.121	
19	SN406	18:13:00:81 5/16	124.08	CB,Static	Kr	30	10000	170.3	1212	0	0	25	No	4.8	
20	SN406	18:15:26:53 5/16	75.14	All 1s, Static	Kr	30	10000	169.3	1137	0	0	25	No	4.8	
21	SN406	18:17:08:97 5/16	64.53	D=A, Static	Kr	30	9080	177.3	1110	0	0	25	No	4.3584	
22	SN406	18:18:45:91 5/16	65.8	CB, Retention	Kr	30	10000	191.3	1437	0	0	25	No	4.8	
23	SN406	18:20:19:45 5/16	74.2	All 1s, Retention	Kr	30	10000	183.4	1320	0	0	25	No	4.8	
24	SN406	18:22:06:72 5/16	70.19	D=A, Retention	Kr	30	9025	184.4	1255	0	0	25	No	4.332	
25	SN406	18:25:29:34 5/16	70.96	CB,Static	Kr	20.6	10000	201	540	0	0	25	No	3.296	
26	SN408	18:33:19:39 5/16	42.9	CB,Static	Kr	20.6	10000	341	735	0	0	25	No	3.296	
27	SN408	18:36:05:27 5/16	66.07	CB,Static	Kr	30	10000	183	1312	0	0	25	No	4.8	
28	SN408	18:37:38:47 5/16	56.96	CB, Retention	Kr	30	8550	237	1453	0	0	25	No	4.104	
29	SN408	18:42:57:15 5/16	48.61	CB, Retention	Kr	40	5000	151.9	1338	0	0	25	No	3.2	
30	SN408	18:44:09:49 5/16	68.11	CB,Static	Kr	40	8660	159.4	1870	0	0	25	No	5.5424	
31	SN408	18:47:19:70 5/16	236.01	Ctrl Logic	Kr	40	1000000	4728	49	0	0	25	No	640	2 Ctrl Logic Errors
32	SN408	18:53:51:48 5/16	186.58	Ctrl Logic	Kr	30	1000000	5862	20	0	0	25	No	480	1 Ctrl Logic Error
33	SN408	18:59:00:55 5/16	187.35	Ctrl Logic	Kr	20.6	1000000	5906	3	0	0	25	No	329.6	0 Ctrl Logic Errors
34	SN44	19:07:57:00 5/16	175.7	Ctrl Logic	Kr	20.6	1000000	6125	5	0	0	25	No	329.6	0 Ctrl Errors
35	SN44	19:13:09:42 5/16	199.49	Ctrl Logic	Kr	30	1000000	5339	17	0	0	25	No	480	1 Ctrl Logic Error
36	SN44	19:17:44:10 5/16	208.61	Ctrl Logic	Kr	40	1000000	4868	52	0	0	25	No	640	2 Ctrl Logic Errors
37	SN44	19:22:40:42 5/16	56.36	CB,Static	Kr	40	8076	181.6	1094	0	0	25	No	5.1686	
38	SN44	19:26:05:19 5/16	67.55	CB,Static	Kr	30	10000	183.6	915	0	0	25	No	4.8	
39	SN44	19:27:48:89 5/16	61.18	CB, Retention	Kr	30	10000	217.8	1025	0	0	25	No	4.8	
40	SN44	19:30:39:05 5/16	53.33	CB,Static	Kr	20	10000	267.2	507	0	0	25	No	3.2	
41	SN41	19:48:17:95 5/16	53.45	CB,Static	Kr	20	10000	390.6	440	0	0	25	No	3.2	
42	SN41	19:52:01:39 5/16	51.74	CB,Static	Kr	30	10000	256.8	739	0	0	25	No	4.8	
43	SN41	19:53:39:76 5/16	52.9	CB, Retention	Kr	30	10000	265.3	1028	0	0	25	No	4.8	
44	SN41	19:56:26:96 5/16	52.23	CB,Static	Kr	40	10000	235	1154	0	0	25	No	6.4	

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45	SN41	19:59:10:03	5/16	238.05	Ctrl Logic	Kr	40	1000000	4669	39	0	0	25	No	640	1 Ctrl Logic Error
46	SN41	20:04:27:44	5/16	185.32	Ctrl Logic	Kr	30	1000000	5923	13	0	0	25	No	480	0 Ctrl Logic Errors
47	SN41	20:09:13:06	5/16	164.66	Ctrl Logic	Kr	20.6	1000000	6616	4	0	0	25	No	329.6	0 Ctrl Logic Errors
48	SN41	21:39:17:89	5/16	48.39	CB,Static	XE	53.1	6671	194	1125	0	0	25	No	5.6677	
49	SN41	21:40:52:14	5/16	48.61	CB, Retention	XE	53.1	5457	178	1007	0	0	25	No	4.6363	
50	SN41	21:43:57:95	5/16	48.67	CB,Static	XE	60	5792	154	1138	0	0	25	No	5.5603	
51	SN41	21:52:23:10	5/16	61.25	CB,Static	XE	120	3666	155	1582	0	0	25	No	7.0387	
52	SN41	22:21:45:77	5/16	915.78	SEL	XE	120	10000000	22360	1553	0	0	125	No	19200	Idd = 62mA
53	SN41	22:43:09:71	5/16	70.03	Ctrl Logic	XE	60	1000000	19650	82	0	0	25	No	960	3 Ctrl Logic Errors
54	SN44	22:49:12:17	5/16	59.65	CB,Static	XE	53.1	7578	183.4	1179	0	0	25	No	6.4383	
55	SN44	22:52:28:52	5/16	59.59	CB,Static	XE	60	6557	154	1269	0	0	25	No	6.2947	
56	SN44	22:53:58:44	5/16	57.56	CB, Retention	XE	60	5877	143	1536	0	0	25	No	5.6419	
57	SN44	23:00:30:82	5/16	56.02	CB,Static	XE	120	3263	144.6	1630	0	0	25	No	6.265	
58	SN44	23:03:03:30	5/16	79.04	Ctrl Logic	XE	120	1000000	41220	126	0	0	25	No	1920	2 Ctrl Logic Errors
59	SN44	23:10:05:35	5/16	558.59	SEL	XE	120	10000000	37270	1680	0	0	125	No	19200	Idd = 55mA
60	SN406	23:25:10:74	5/16	47.02	CB,Static	XE	53.1	7179	208.9	1287	0	0	25	No	6.0993	
61	SN406	23:27:23:00	5/16	48.72	CB,Static	XE	60	6824	202.1	1470	0	0	25	No	6.551	
62	SN406	23:28:53:35	5/16	48.61	CB, Retention	XE	60	6935	218.1	1441	0	0	25	No	6.6576	
63	SN406	23:33:52:53	5/16	44.44	CB, Retention	XE	120	2306	171.1	1581	0	0	25	No	4.4275	
64	SN406	23:35:02:89	5/16	48.89	CB,Static	XE	120	3599	196.5	1924	0	0	25	No	6.9101	
65	SN406	23:36:50:05	5/16	65.25	Ctrl Logic	XE	120	993600	42070	117	0	0	25	No	1907.7	4 Ctrl Logic Errors
66	SN406	23:42:13:56	5/16	574.85	SEL	XE	120	10000000	35780	1554	0	0	125	No	19200	Idd=61mA
67	Sn407	23:57:13:02	5/16	50.53	CB,Static	XE	53.1	7084	222.9	1411	0	0	25	No	6.0186	
68	Sn407	23:59:20:01	5/16	-86345.62	CB,Static	XE	60	7815	201.3	2063	0	0	25	No	7.5024	
69	Sn407	0:00:37:67	5/17/	48.5	CB, Retention	XE	60	6929	203.3	2107	0	0	25	No	6.6518	
70	Sn407	0:04:51:37	5/17/	39.82	CB,Static	XE	120	2369	188.1	1859	0	0	25	No	4.5485	
71	Sn407	0:06:45:02	5/17/	59.1	Ctrl Logic	XE	120	1000000	49870	110	0	0	25	No	1920	4 Ctrl Logic Errors
72	Sn407	0:34:12:56	5/17/	630.87	SEL	XE	120	10000000	33510	1786	0	0	125	No	19200	Idd = 52mA
73	SN408	0:51:20:66	5/17/	43.72	CB,Static	XE	53.1	8037	280.5	1911	0	0	25	No	6.8282	
74	SN408	0:53:33:74	5/17/	39.87	CB,Static	XE	60	6479	353.1	1740	0	0	25	No	6.2198	
75	SN408	0:54:48:49	5/17/	36.58	CB, Retention	XE	60	6863	267.9	2143	0	0	25	No	6.5885	
76	SN408	0:58:46:38	5/17/	30.86	CB,Static	XE	120	3090	278.2	2124	0	0	25	No	5.9328	
77	SN408	1:00:14:09	5/17/	70.03	Ctrl Logic	XE	120	1000000	40370	136	0	0	25	No	1920	2 Ctrl Logic Errors
78	SN408	1:14:13:57	5/17/	550.85	SEL	XE	120	10110000	38000	1801	0	0	125	No	19411	
79	SN408	5:06:10:16	5/17/	142.31	CB,Static	N	2.6	106600	875.8	519	0	0	25	No	4.4346	
80	SN408	5:18:04:63	5/17/	28.45	CB,Static	N	1.3	323800	17640	538	0	0	25	No	6.735	
81	Sn407	5:23:09:19	5/17/	28.29	CB,Static	N	1.3	306100	19070	565	0	0	25	No	6.3669	
82	Sn407	5:26:41:09	5/17/	29.93	CB,Static	N	2.6	164000	14860	740	0	0	25	No	6.8224	
83	SN406	5:32:15:64	5/17/	23.12	CB,Static	N	2.6	161600	14870	775	0	0	25	No	6.7226	
84	SN406	5:34:30:10	5/17/	26.59	CB,Static	N	1.3	388800	32720	709	0	0	25	No	8.087	
85	SN44	5:38:07:44	5/17/	26.53	CB,Static	N	1.3	351700	20530	579	0	0	25	No	7.3154	
86	SN44	5:40:26:57	5/17/	71.84	CB,Static	N	2.6	245200	30530	1121	0	0	25	No	10.2	
87	SN41	5:45:57:82	5/17/	19.77	CB,Static	N	2.6	198800	19690	907	0	0	25	No	8.2701	
88	SN41	5:48:15:63	5/17/	110.9	CB,Static	N	1.3	349500	23910	626	0	0	25	No	7.2696	

TID per DUT

SN41	SN44	SN406	SN407	SN408
21673.21	22629.72	22638.07	22636.78	22838.48

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