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TID-RLAT Test Report for Cypress 144Mb QDR SRAMs (CYRS1643KV18)

Fab Lot:
L9729013

Date: 29 May 2019 Revision: A

Purchase Order:
Cypress Semiconductor Corporation 4700007161

Prepared By: _____ 20 Jun 2016
JD Instruments Date

Executive Summary

Radiation Lot Acceptance Testing (RLAT) for Total Ionizing Dose (TID) was performed on 144Mb QDR SRAMs (CYRS1643KV18), fab (diffusion) lot L9729013. This lot will be referred to as TV1 for the rest of this report.

TV1 parts were provided in ceramic column grid array (CGA) packages.

Irradiation and testing was performed in accordance with MIL-STD 883 Method 1019.8 Condition A. Radiation induced changes were evaluated using KTL statistics with Probability of Survival (Ps) of 99% and Confidence Level of 90%.

"ON-SITE RLAT Tests" were performed before and immediately after the parts were exposed to radiation. These consisted of functional tests as well as DC parametric measurements on device pins in their normal mode of operation. All parameters monitored on-site stayed well within spec sheet limits up to 250K rad(Si)

"PRODUCTION RLAT Tests" were performed pre- and post-irradiation at the Cypress Semiconductor facility in San Jose, CA. After irradiation and on-site testing the parts were transported back to the Cypress facility using the TM1019 dry ice procedure.

All devices passed the full suite of AC, parametric and functional tests performed on the production tester with devices in their normal operating modes.

All lots passed RLAT analysis to 250K rad(Si) Testing was performed by Mr. Jake Tausch of JD Instruments and monitored by Mr. Helmut Puchner of Cypress Semiconductor.

1.0 PART DESCRIPTION

Total Ionizing Dose (TID) Testing was performed by JD Instruments on one lot of1442Mb QDR SRAMs (CYRS1643KV18). A total of 13 devices were used for this testing. Twelve devices were irradiated and one device was used as control/reference. All parts were serialized by the manufacturer.

These devices have the architecture shown in Figure 1. Internally read and write operations are 72 bits wide. Control logic and latches convert the internal memory architecture to the "X18" architecture seen externally.

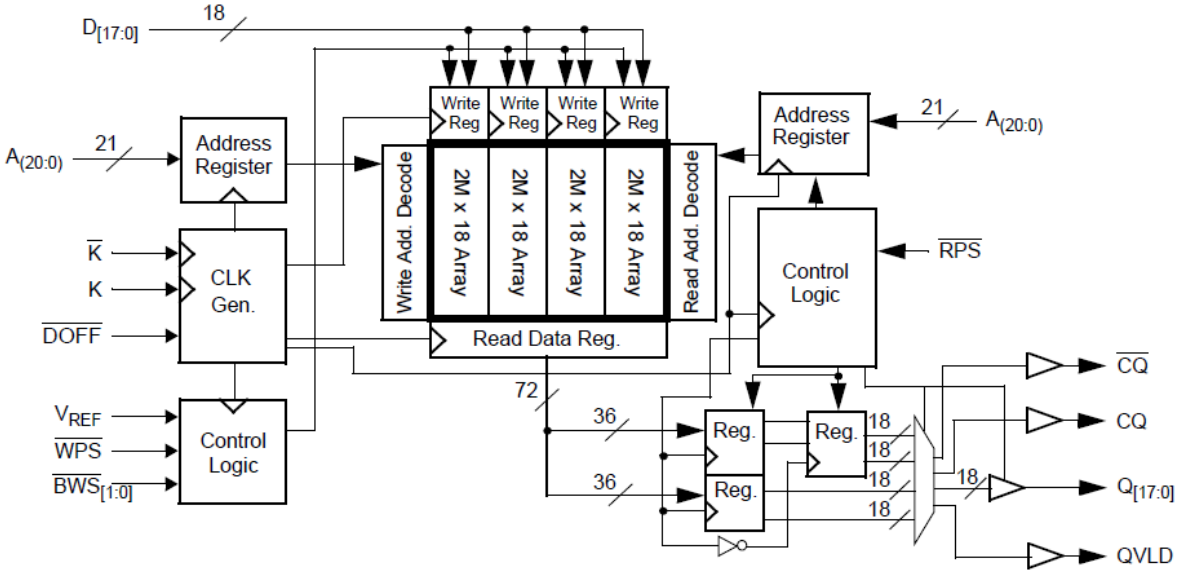


Figure 1. Functional Diagram for CYRS1643KV18

2.0 TEST DESCRIPTION

Devices were provided in 165 position CGA packages. These were inserted into sockets for bias and test. A picture of an open socket is shown in Figure 2 alongside a test device that is flipped over to show the column grid pattern on its bottom surface.

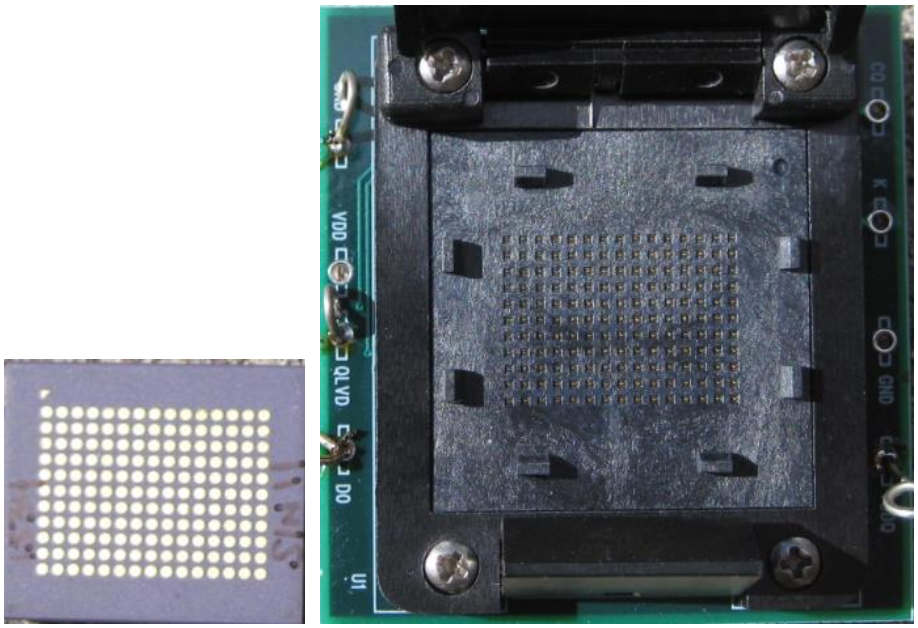


Figure 2. Bottom Surface of DUT and Open Socket

Special bias boards were used in which devices were arranged in a 2 X 2 matrix to minimize dose rate variation across the pattern. Figure 3 shows one of the boards for TV1 parts.

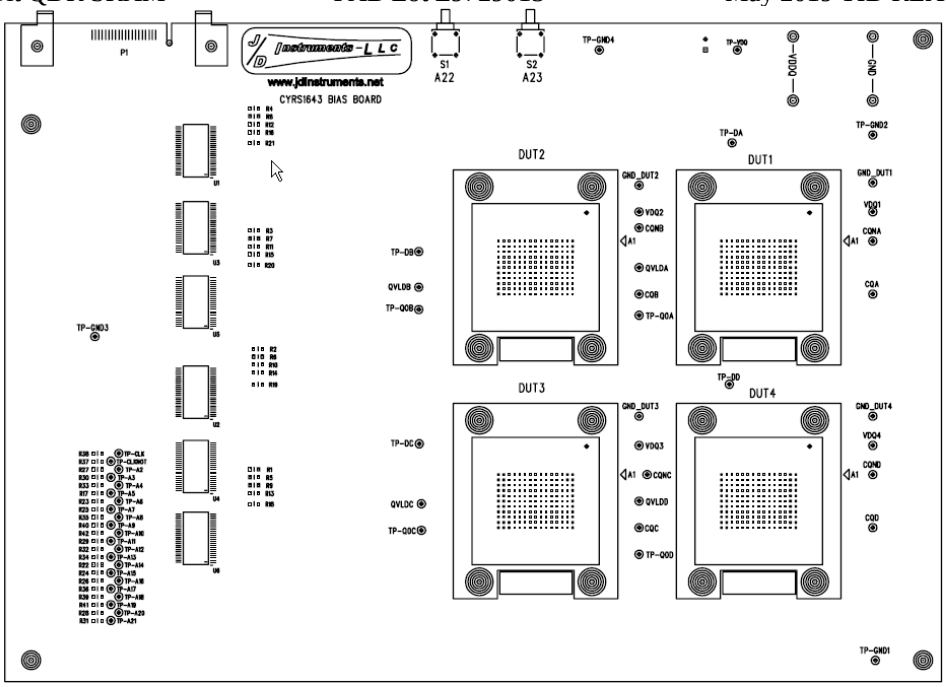


Figure 3. QDR Bias Board

A special “Stimulation” card was used along with the bias boards to provide high speed clocks and dynamic operation of the parts during irradiations. Figure 4 shows an overview of the stimulation board

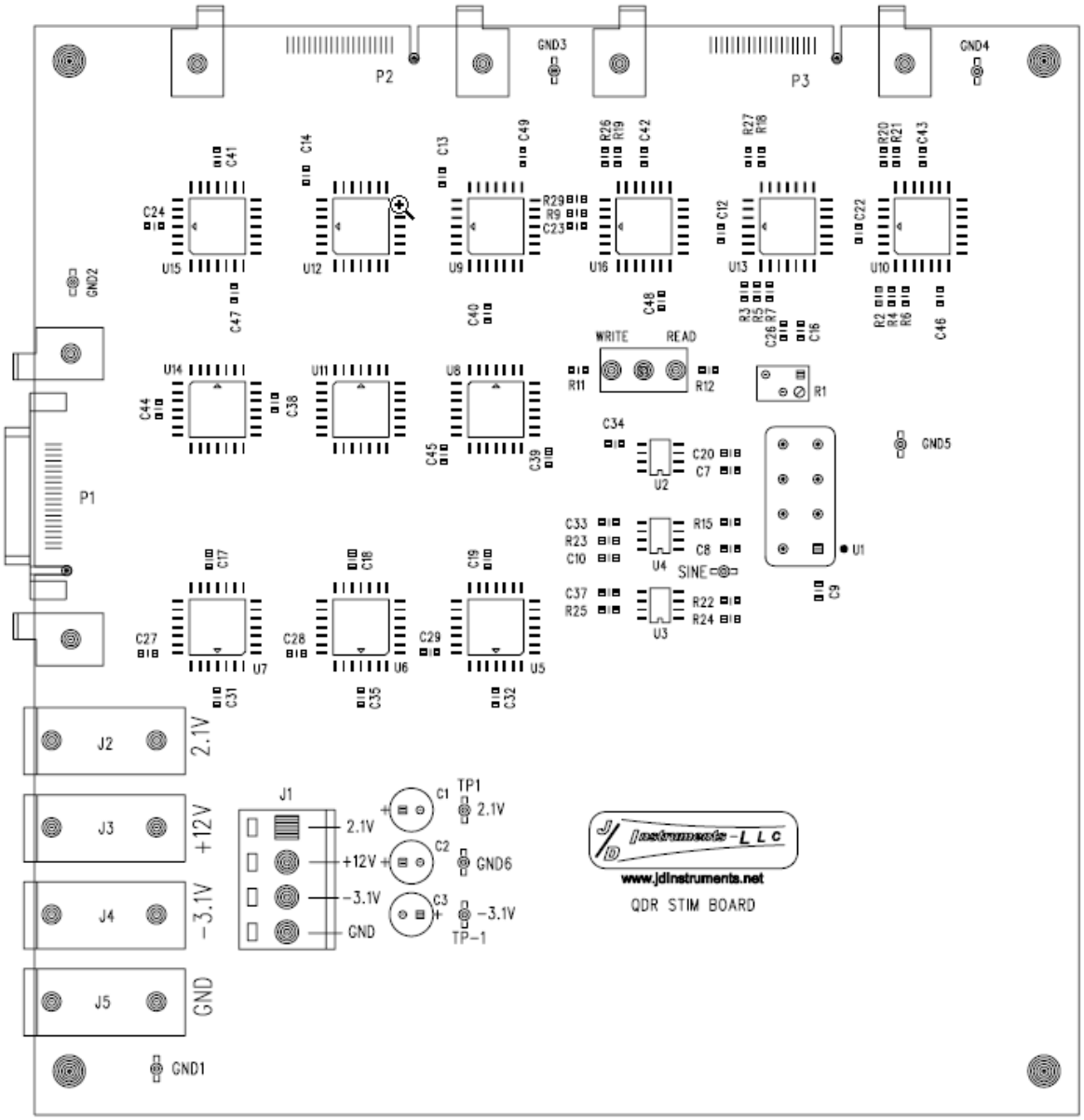


Figure 4. QDR Stimulation Board

The stimulation board provided high speed clocks along with address, data and control signals to 3 bias boards so 12 DUTs could be irradiated simultaneously. The address pattern was a simple count so that all memory addresses would be covered. Data patterns were a logical checkerboard. Note on the stimulation board that there is a 3 position switch just to the right of and just above the center. When this switch was toggled to its left position the checkerboard pattern would be written to memories. When it was toggled to its right position all DUTs would be read and the output pattern could be probed on the bias boards. When the switch was in the center position no write or read operations would be performed but a constant clock signal would be maintained.

Figure 5 shows the 3 bias boards in lead-aluminum boxes arranged around the CO-60 shroud of the radiation facility.

Figure 5. Three Bias Boards in Lead-Aluminum Boxes Surrounding CO-60 Shroud

Irradiations were performed with devices loaded with a checkerboard pattern and with the devices biased to their maximum supply voltages (Vdd = Vddq = 1.9V). Later testing was performed with devices biased to their nominal voltages (Vdd =1.8V, Vddq = 1.5V). This was considered the worst case combination of bias conditions since more radiation damage will be induced at a higher bias and AC performance (e.g. race conditions) are worse at lower biases.

After each radiation interval parts were removed from the bias boards and tested using a JD Instruments Algorithmic Test Vector (ATV) system.

In order to test these parts at 250MHz operating frequency a special test board was designed that contains an FPGA to provide the high speed interface to the DUT. The ATV system provided the patterns to be written to the DUT and the FPGA performed the actual write operation. Similarly, ATV initiated a read operation by issuing a command to the FPGA. The FPGA then read a burst of 4 memory locations from the DUT and passed the information to the ATV at a slower speed.

Because of their high frequency of operation CYRS1643KV18 QDR SRAMs present unique measurement problems for RLAT. Many AC parameters (e.g. data set-up and hold) have limits of only +/- 0.5nS at 250MHz clock frequency and these are difficult to measure “on-site” at a radiation facility. These parameters can only be measured at facilities remote from the radiation source where it would not be possible to test the parts within the time limit imposed by TM1019. For these parameters the TM1019 dry ice procedure was used to evaluate the

pre/post radiation performance of all AC parameters listed in the SMD. AC testing was carried out for pre/post radiation samples at Cypress Semiconductor's production test floor utilizing an Advantest T5592 production grade tester.

Therefore, RLAT testing was divided into 2 sets of tests: tests performed on-site at the radiation facility (ON-SITE RLAT TESTS) and tests performed remotely at the Cypress Semiconductor production facility (PRODUCTION RLAT TESTS).

Testing was performed by Jake Tausch of JD Instruments and Helmut Puchner of Cypress Semiconductor.

2.1 DOSIMETRY

Dosimetry was provided by AFRL personnel using a NIST traceable ion chamber. Dose rates for these tests were 53 rad(Si)/sec.

2.2 ON-SITE RLAT TESTS

Tests performed on-site at the radiation facility included all DC parameters listed in the data sheet for these aprts. Specifically these included: Voh, Vol, Voh(low Current), Vol(low Current), Vih, Vil, Iih, Iil, Ioz(h), Ioz(l), Idd. Idd was measured using 2 memory patterns which include CB, CB*. Part functionality was verified using a MarchX algorithm over the entire memory space.

A detailed listing of tests, conditions and limits for ON-SITE RLAT TESTS is shown in Appendix A.

On-Site testing was performed using an Algorithmic Test Vector (ATV) system from JD Instruments as shown in figure 6. This is a portable system containing many of the features found in larger main-frame test systems. For this application it is particularly useful in that it collects data in both primitive error logs and also records summary results in spreadsheet form, simplifying on-site understanding of results as the test proceeds.

Figure 6. ATV Test System used for SEE Testing

All irradiations and tests were performed on these parts while they are operating at their maximum clock frequency of 250MHz. Devices were loaded with a checkerboard pattern during irradiation. The SRAM portion

of the devices were in a static condition even though the rest of the device was operating at it's maximum frequency.

In order to achieve a 250MHz operating frequency a special test board was designed that contains an FPGA to provide the high speed interface to the DUT. The ATV system provided the patterns to be written to the DUT and the FPGA performed the actual write operation. Similarly, ATV initiated a read operation by issuing a command to the FPGA. The FPGA then read a burst of 4 memory locations from the DUT and passed the information to the ATV at a slower speed.

Irradiations were performed with devices biased to their maximum supply voltages (Vdd = Vddq = 1.9V). Parametric testing was performed with devices biased to their nominal voltages (Vdd =1.8V, Vddq = 1.5V). This was considered the worst case combination of bias conditions since more radiation damage will be induced at a higher bias and AC performance (e.g. race conditions) are worse at lower biases.

The part "travelers" and "Run Logs" that documented irradiation and test times is shown in Appendix C.

2.3 PRODUCTION RLAT TESTS

The full suite of production tests were performed on these devices both pre- and post-irradiation.

AC characterization tests were performed using the 4 functional algorithms specified in SMD 5962-11201, Appendix A. Specifically these are: CB/CB*, March, XY March and CEDES. Each algorithm was performed while measuring AC parameters so a set of measurements was collected for each parameter pre- and post-radiation.

AC tests included all standard manufacturing parameters. These are listed in table 1. Some parameters are measured relative to several inputs or conditions. Thus, for instance, Tsc was measured relative to the RPS, WPS and BWS pins. In the table these pins/conditions are shown in parentheses.

Parameter	Description
Tcyc	K Clock Cycle Time
Tkhkh	K Clock Rise to K* Clock Rise
Tas	Address Setup to K Clock Rise
Tsc (_Rps#, _Wps#, _Bws#)	Control Setup to K Clock Rise
Tds (_ /1 /2)	Data Setup to Clock Rise
Tah (_/1)	Address Hold after K Clock Rise
Thc(_Rps#, _Wps#, _Bws#)	Control Hold after K Clock Rise
Tdh (_ /1 /2)	Data Hold after Clock Rise
Tco (1 /2)	Clock Rise to Data Valid
Tdoh (1 /2)	Data Output Hold after Clock Rise
Tccqo (1 /2)	K/K* Clock Rise to Echo Clock Valid

Table 1. Standard Manufacturing AC Measurements

One of the standard production tests puts all pins of the device in an "off" condition and measures the leakage current of each pin. This special test mode is programmed via the JTAG interface on each device.

3.0 Lot Acceptance Technique

Parameters were measured and recorded in an excel format spread sheet. The measured values at each radiation step were analyzed using the Radiation Lot Acceptance Test (RLAT) "variables method" (see MIL-HDBK-814, Appendix Section 50, especially Table IXB).

In the RLAT variables method the average (Avg) and standard deviation (Std) of each parameter are calculated for the group of parts being irradiated. A value is then calculated and compared to the part limits using this average and standard deviation along with a one sided tolerance factor, KTL.

For parameters where the limit is higher than measured values the lot is acceptable if

$$Avg + KTL * Std < Limit \qquad \text{(eq. 1)}$$

For parameters where the limit is lower than measured values the lot is acceptable if

$$Avg - KTL * Std > Limit \qquad \text{(eq. 2)}$$

Values for KTL vary depending on sample size, Probability of Survival (Ps) and confidence level. For this test, with a radiation sample size of 12, Ps of 0.99 and a confidence level of 0.9, the value for KTL was 3.372 (MIL-HDBK-814, Table IXB).

Figure 7 shows test results for one of the parameters that changed with radiation. This is a plot of Idd when a logical checkerboard pattern was loaded in memory and memories were continuously read.

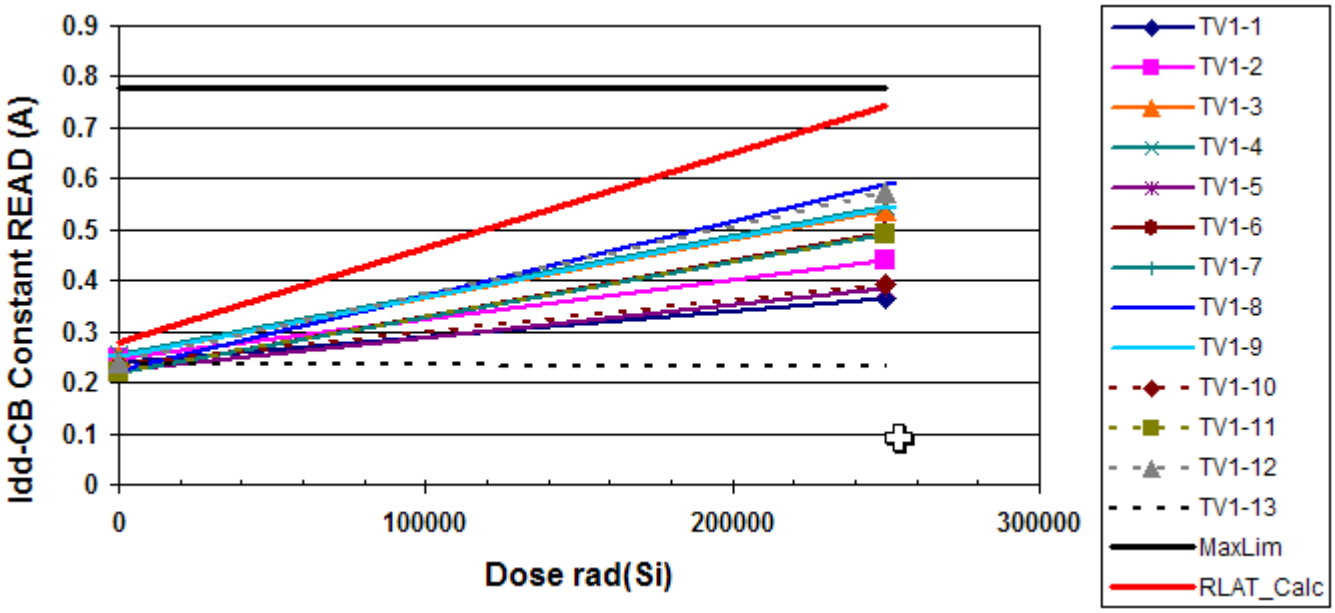


Figure 7. Idd Continuous READ – CheckerBoard

In this plot first note that the limit is plotted as a solid, bold BLACK line, 0.78A in this case. Second, note that the reference device (TV1-13) is plotted as a black dotted line with no symbols. The reference device was not irradiated and its value remained the same across the plot. Each irradiated part is plotted as a separate line with varying symbols. The RLAT value calculated for the set of irradiated parts is shown as a solid, bold RED line.

The plot shows a significant increase in Idd immediately after the radiation dose of 250K rad(Si) but no part nor the RLAT calculation came close to the limit.

4.0 ON-SITE RLAT Analysis Results

No memory bits on any device ever failed during this testing and are therefore not discussed further. Results of the other parameters are presented below.

4.1 Idd CB

Power supply current was measured with 2 different patterns statically loaded into memory and with the DUTs being continuously read. The DUTs were clocked at 250MHz for all tests. The results for TV1 were previously presented. Idd did increase with total dose, but the increase was well balanced within each lot. Calculated RLAT values stayed well below the limit of 0.78A for all lots.

4.2 Idd CB*

Figure 8 shows Idd (continuous READ) when a logical checkerboard-not pattern was loaded into memories. As with Idd-Checkerboard the currents did increase, but the increase was well balanced within each lot. Calculated RLAT values stayed well below the limit of 0.78A for all lots.

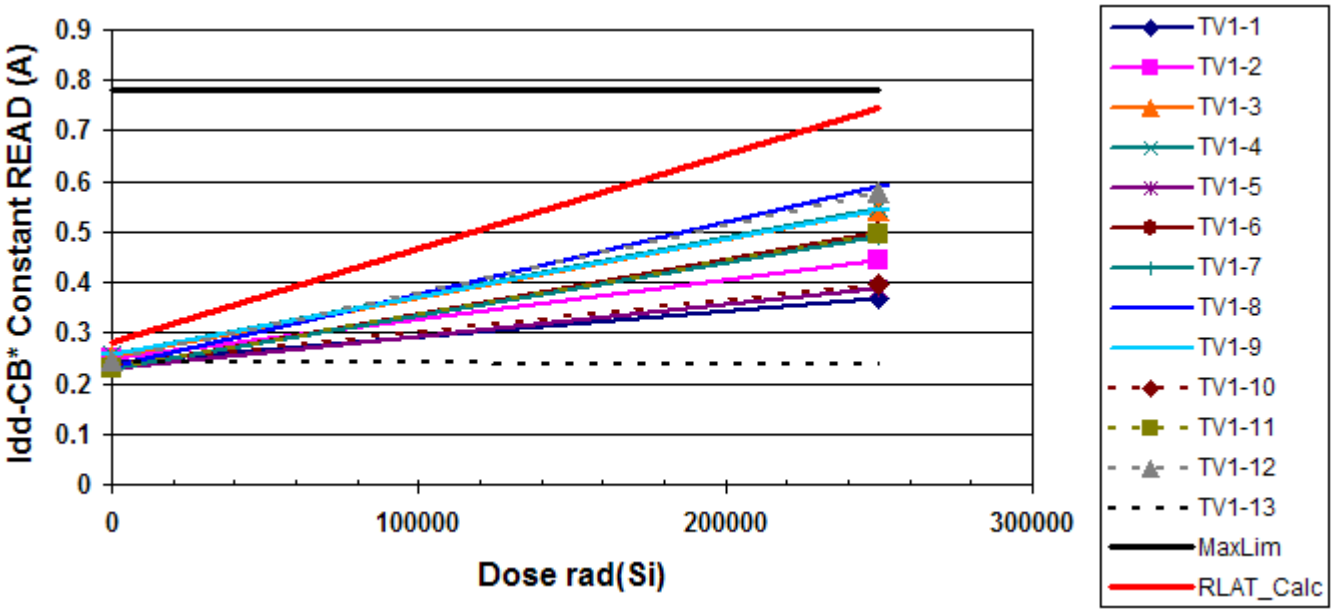


Figure 8. Idd Continuous READ – CheckerBoardNot

4.2 Vih and ViL

Vih and Vil have limits of +/-0.1V relative to the VRef applied to the part. VRef in this case was 0.75V so the limits were 0.85V for Vih and 0.65V for Vil. In other words, the DUTs must respond to an input voltage as a logic high at some level below 0.85V and as a logic low at some level above 0.65V.

These parameters were tested by varying the input logic level of signals applied to the DUT and executing a write/read test over a portion of the memory. Logic high and logic low voltages were varied in a binary search sequence with the smallest step being ~14mV. Figure 9 shows measurements and RLAT analysis for Vih. Figure 10 shows measurements and RLAT analysis for Vil. There was no significant change in these parameters with increasing radiation and all lots pass RLAT analysis for both parameters.

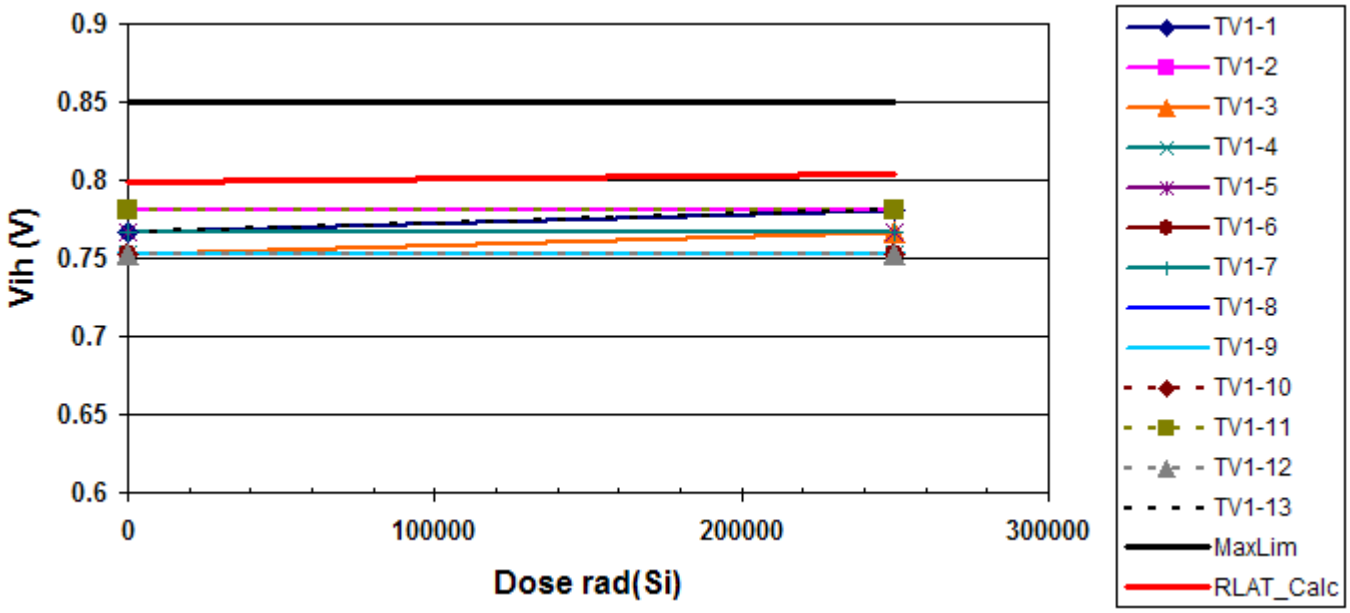


Figure 9. RLAT Results for Vih

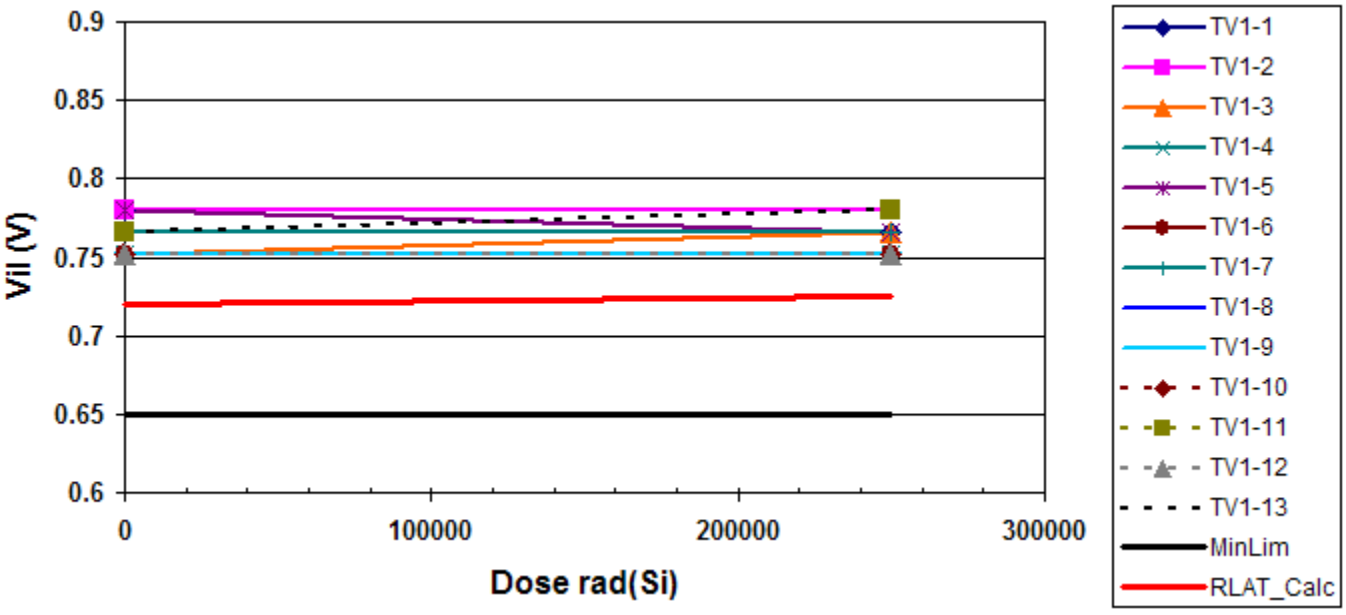


Figure 10. RLAT Results for ViL

4.3 Voh and Vol (Low Current)

These parts have 2 specifications for Voh and Vol. A load current of +/-0.1mA was used for "low current" testing and +/-2mA was used for high current testing. Figures 11 and 12 show measurements and RLAT analysis for Voh and Vol with the lower load currents. With these load currents there is a lower limit of 1.3V for Voh and an upper limit of 0.2V for Vol. There was no detectable change in these parameters with increasing radiation and all lots pass RLAT analysis for both parameters.

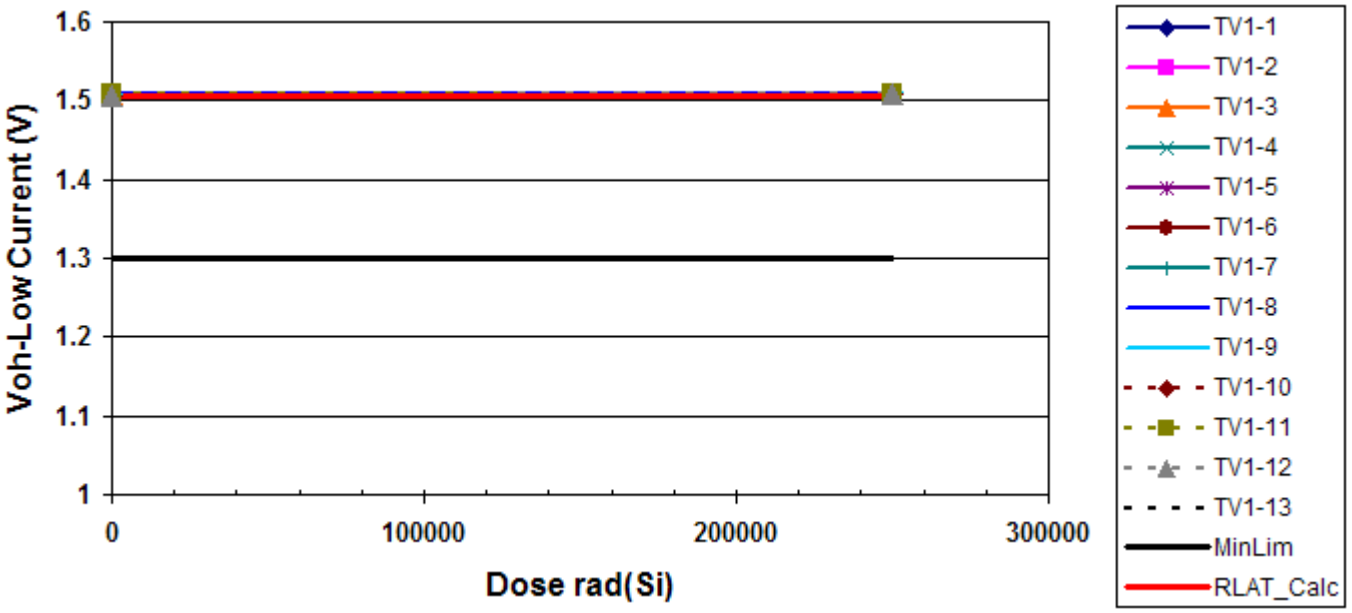


Figure 11. RLAT Results for Voh (Low Current)

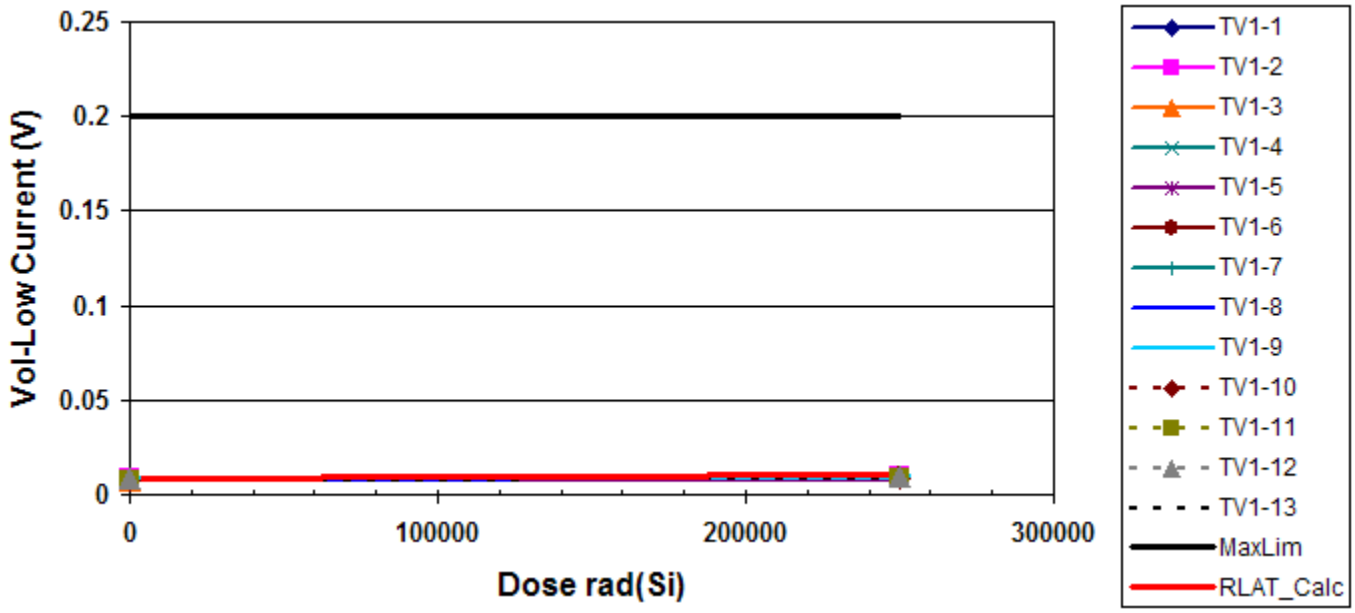


Figure 12. RLAT Results for Vol (Low Current)

4.4 Voh and Vol

Figures 13 shows measurements and RLAT analysis for Voh with a higher load current of -2mA. Figure 14 shows measurements and RLAT analysis of Vol with a load current of 2mA. With these load currents there is a lower limit of 0.87V for Voh and an upper limit of 0.63V for Vol. There was very little change in these parameters with increasing radiation and all lots pass RLAT analysis for both parameters.

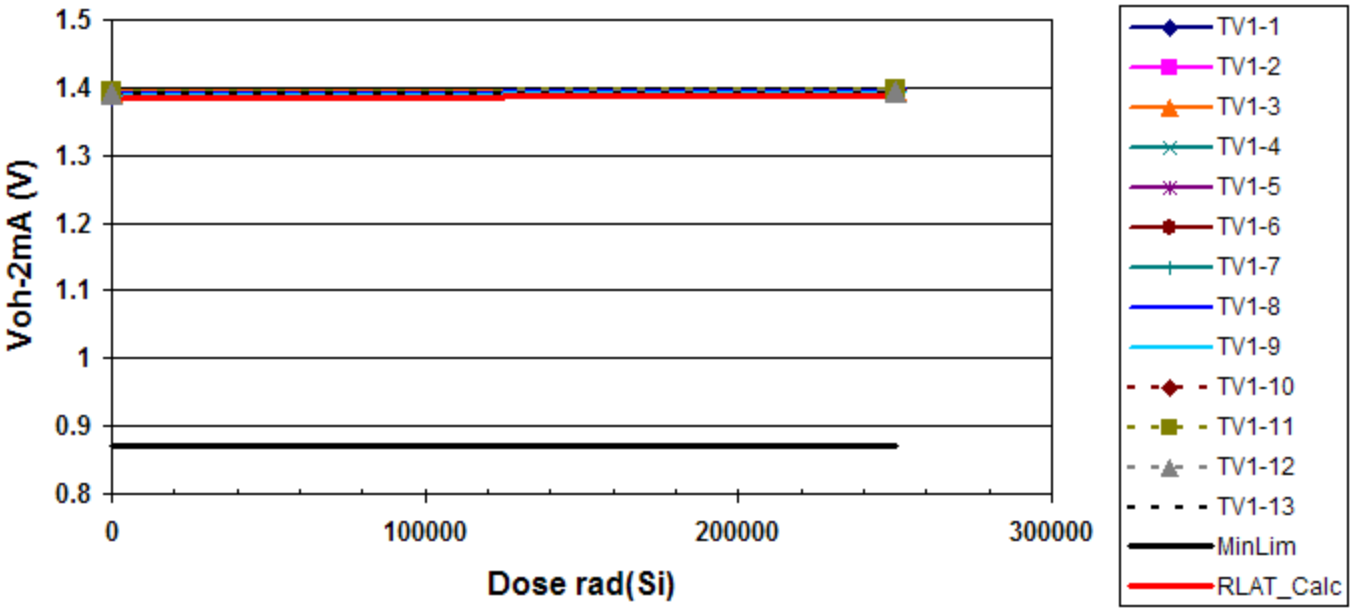


Figure 13. RLAT Results for Voh

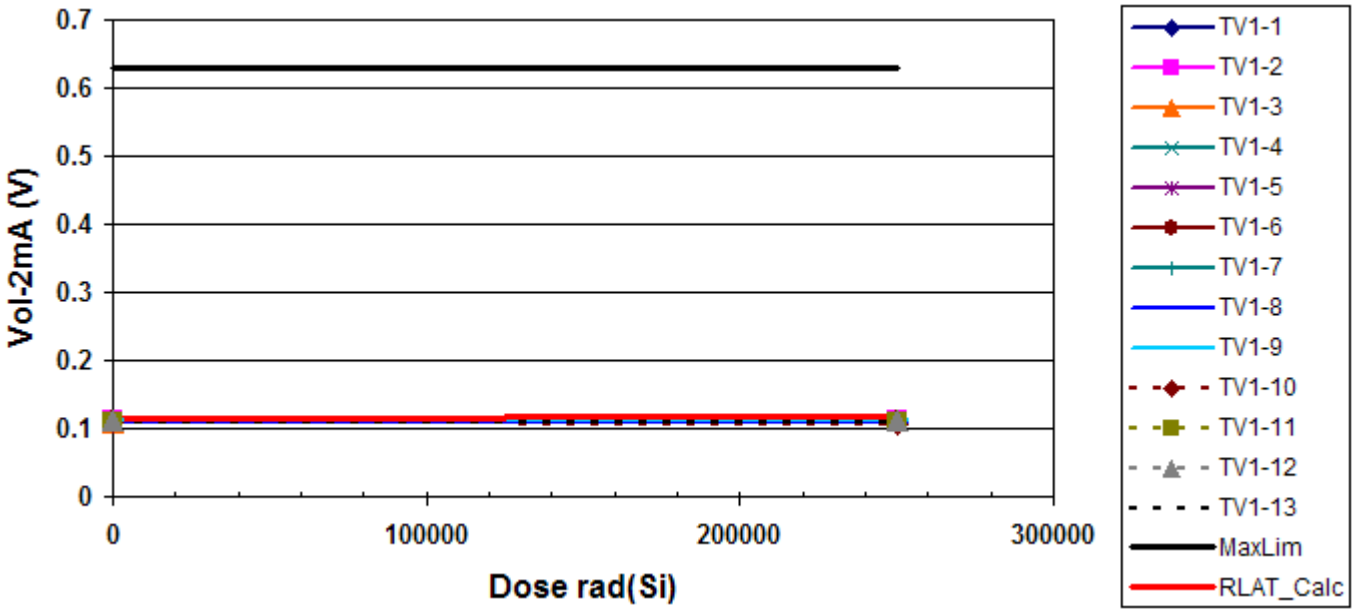


Figure 14. RLAT Results for Vol

4.5 Iih and IiL

Iih and Iil are the input leakage currents when the inputs are biased to a logic high and logic low. Both have a limit of 20uA. Iih results are shown in figure 15. Iil results are shown in figure 16. Both parameters easily pass RLAT analysis for all lots.

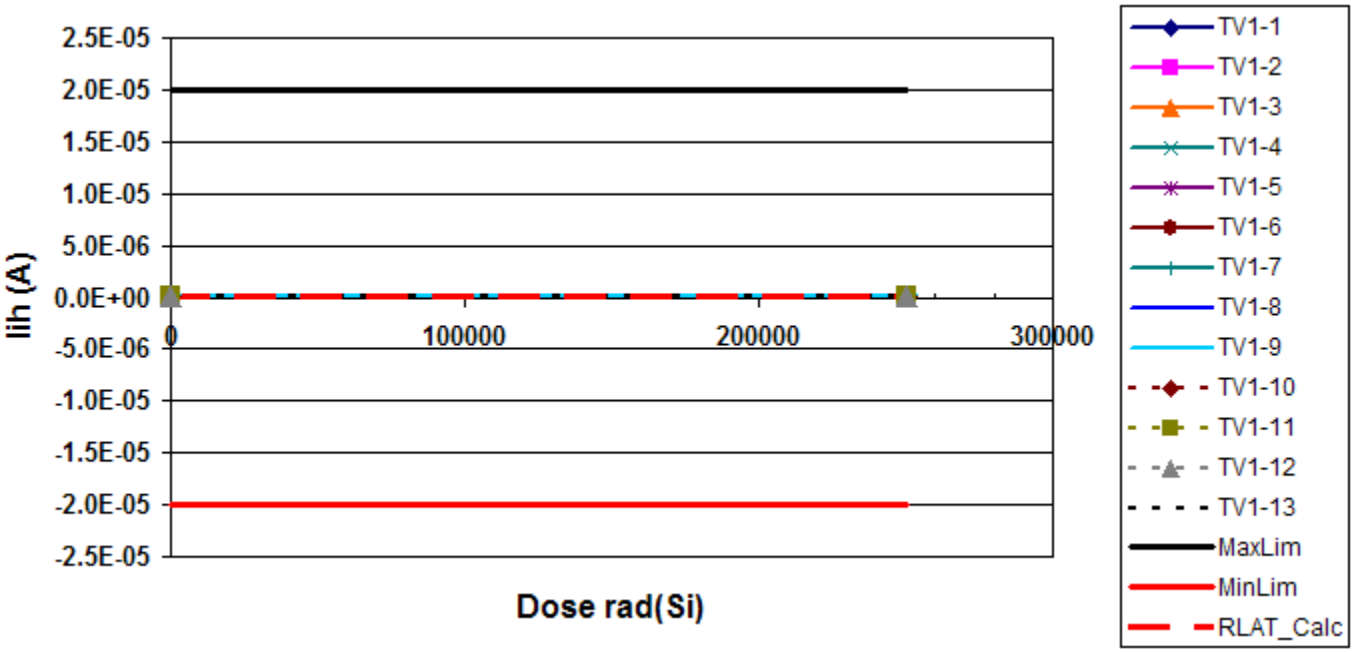


Figure 15. RLAT Results for Iih

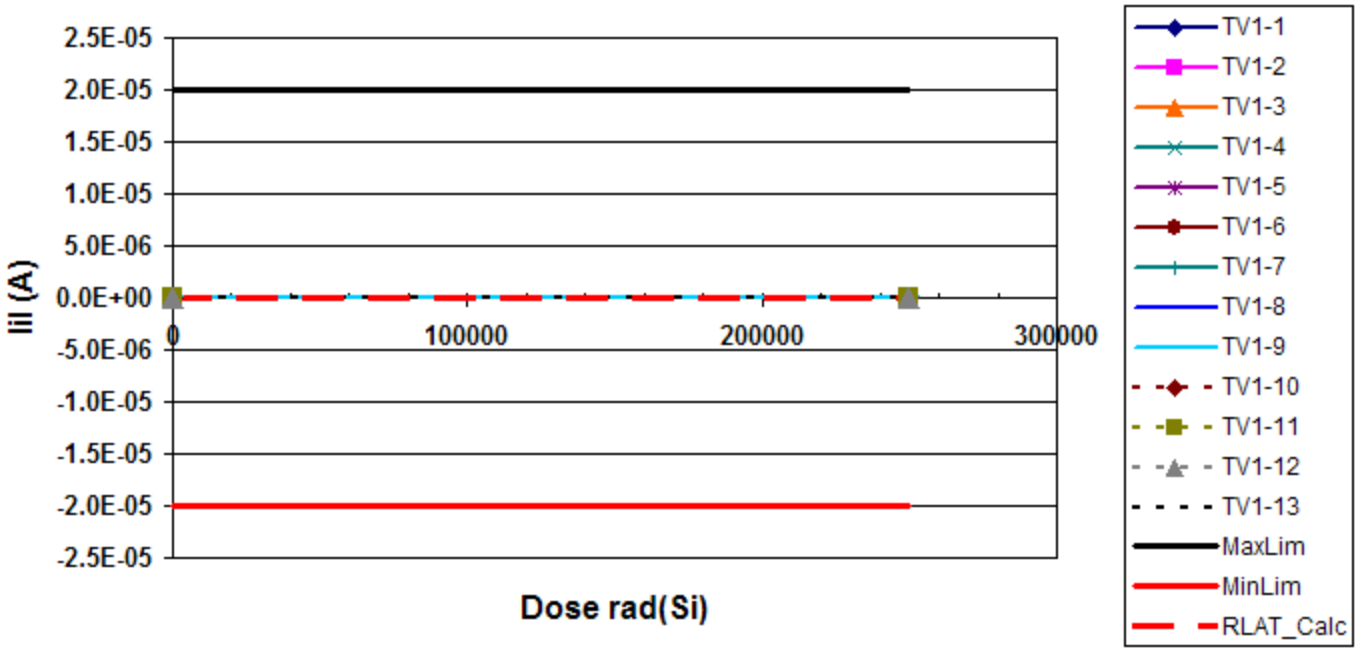


Figure 16. RLAT Results for IiL

4.6 Iozh and IozL

Iozh and Iozl are the output leakage currents when devices are tri-stated and voltages equal to logic high and logic low are applied to the outputs. Limits are 20uA for both parameters. Iozh measurements are shown in figures 17. Iozl measurements are shown in figure 18. Both parameters easily pass RLAT analysis for all lots.

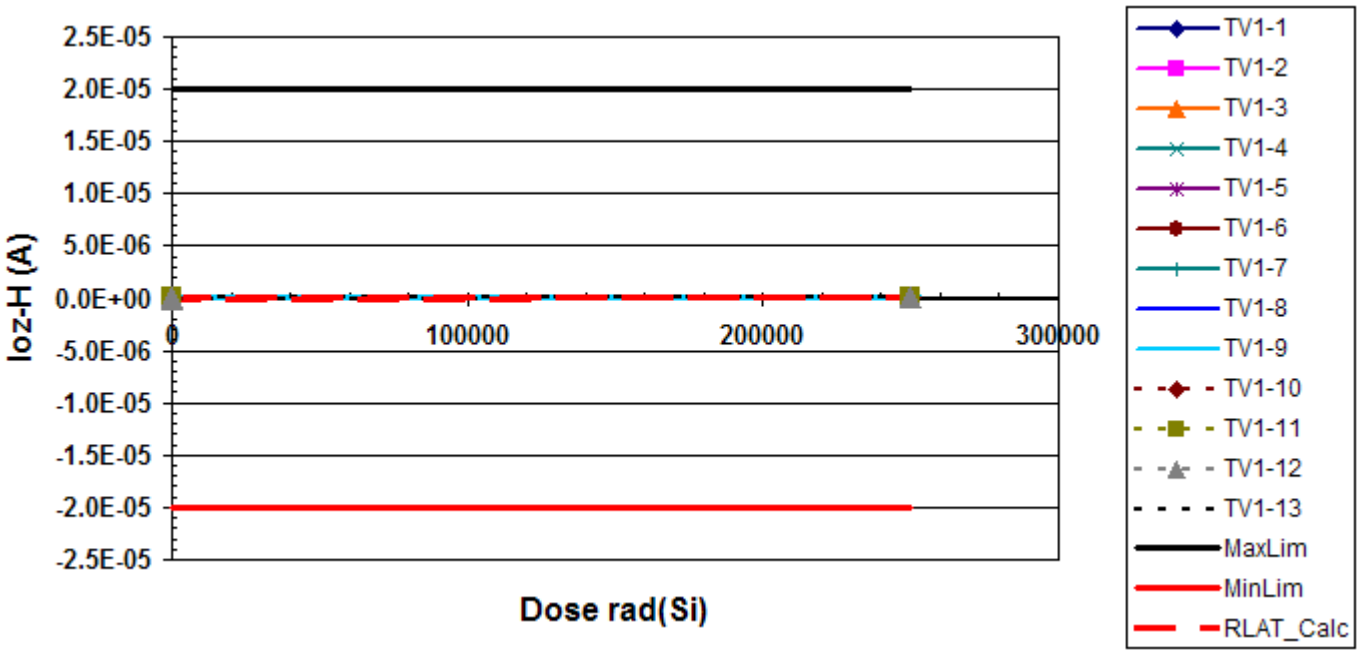


Figure 17. RLAT Results for Iozh

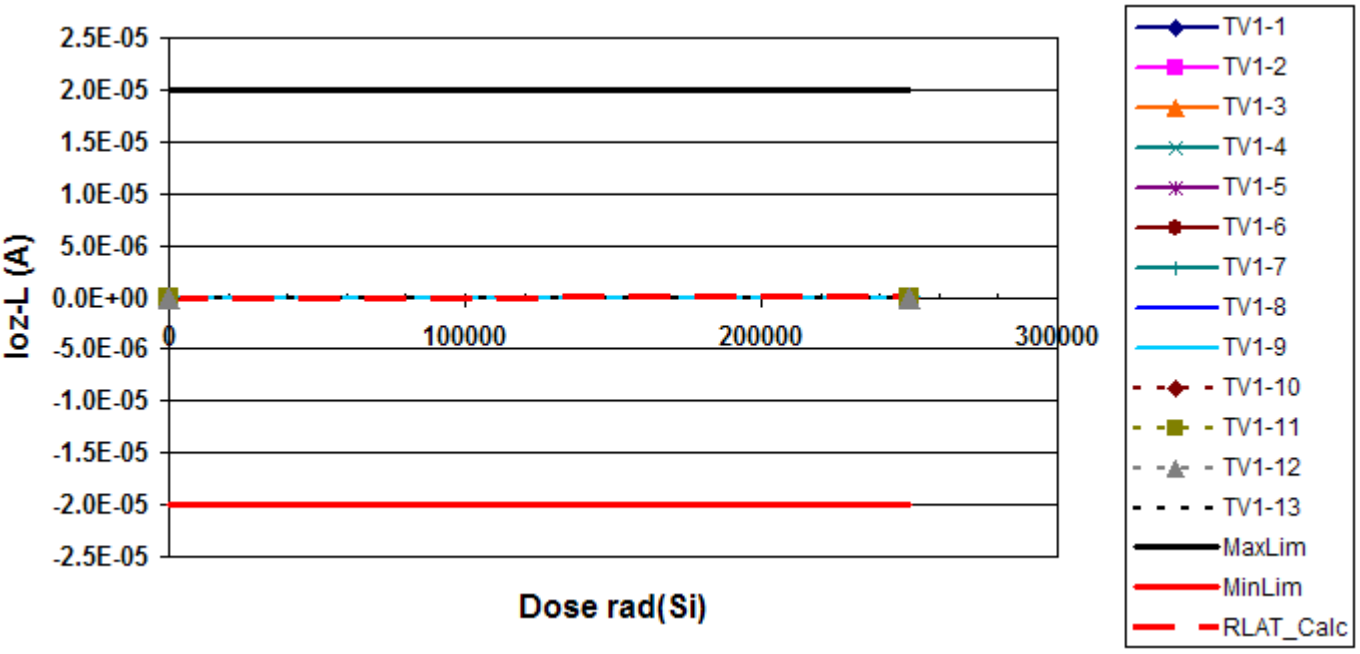


Figure 18. RLAT Results for IozL

5.0 PRODUCTION RLAT Analysis Results

5.1 PRODUCTION RLAT AC RESULTS

A full suite of AC tests were performed pre- and post-irradiation on these parts. These tests included many variations of bias conditions, test patterns, reference voltages, threshold voltages for output rise/fall measurements, etc. No significant changes were detected at any combination of conditions and all measurement subsets easily passed RLAT analysis. Results for a subset of tests are shown below as examples of radiation induced changes in AC parameters.

	Irradiated Parts														
SMD Name	1	2	3	4	5	6	7	8	9	10	11	12	RLAT	Limit (pS)	Pass/Fail
tCCQ0	950	837.5	887.5	887.5	825	937.5	862.5	875	850	862.5	812.5	837.5	1010.819	<1350	P
tCYC	2500	2500	2500	2500	2500	2500	2500	2500	2500	2500	2500	2500	2500	<4000	P
tCO	550	462.5	537.5	537.5	500	512.5	537.5	525	500	537.5	487.5	512.5	603.4663	<850	P
tDOH	225	87.46	187.5	187.5	175	162.5	187.5	175	175	187.5	137.4	162.5	283.5133	<850	P
tSA	175	175	175	175	175	225	150	175	200	175	175	200	244.7935	<500	P
tHA	300	300	300	300	250	300	300	300	300	300	250	300	357.2941	<500	P
tSD	100	100	125	100	150	125	125	125	125	125	125	150	179.2761	<500	P
tHD	225	225	225	225	225	250	225	225	200	225	225	225	260.9456	<500	P
tSC	125	100	125	100	125	150	100	125	125	100	125	150	181.3389	<500	P
tHC	75	100	75	100	50	75	100	75	75	100	100	50	144.7935	<500	P
tKC Var *	425	375	375	375	375	375	375	425	425	400	375	375	313.685	>200	P

* tKC Var is the amount of jitter the part can tolerate on the input clock and still operate/phase-lock properly

Figure 19. Production RLAT AC Results

6.0 Conclusions

Fab lot L9729013 of CYRS1643KV18 devices passed RLAT analysis to 250K rad(Si) on all parameters listed in the data sheet after the application of 99/90 KTL statistics.

Appendix A. On-Site RLAT Test Conditions and Specifications

Common Test Conditions:

VDDq During Measurements = 1.5V
VDD During Measurements = 1.8V

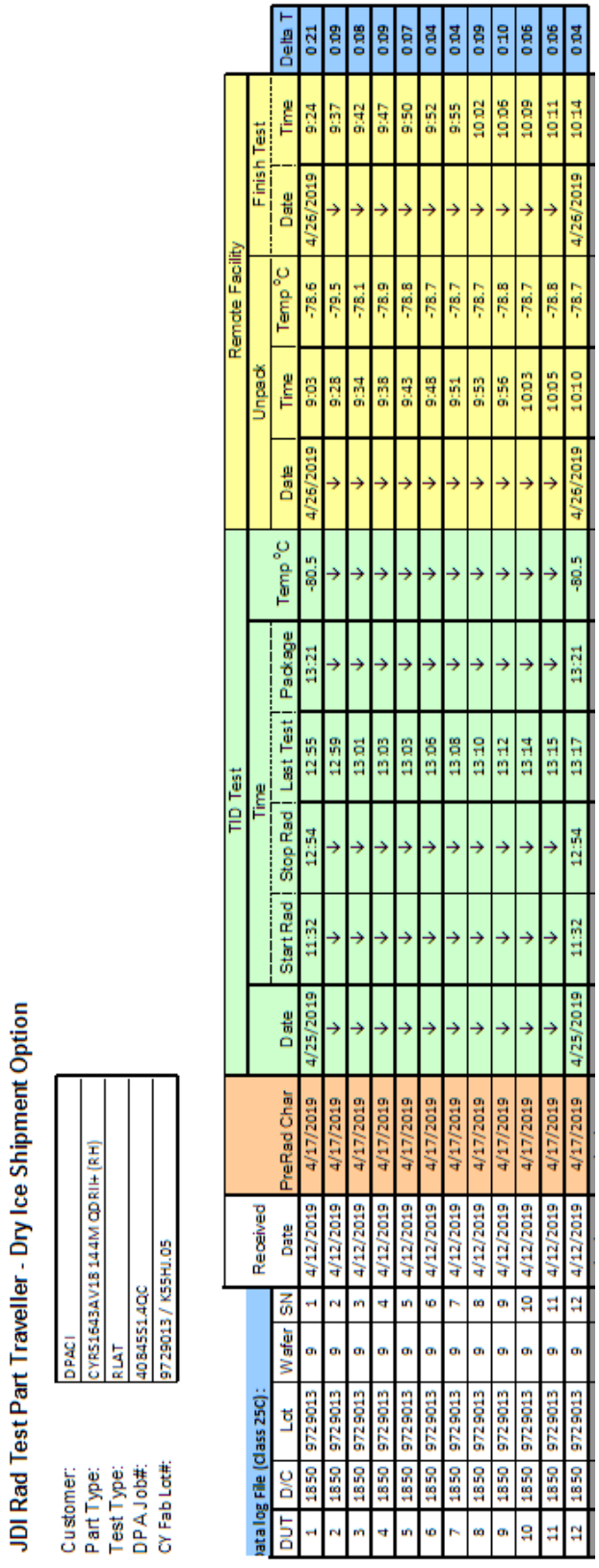
1. Idd Checkerboard and Checkerboard* (1.275A)
    a. Pattern will be loaded into memory
    b. Current will be measured while DUT is being continuously read
2. IiL/Iih – Input Leakage Current (+/-20uA)
    a. 0V & Vddq applied to all Address Pins
    b. Measure Input Currents
    c. Record Highest Value
3. Iozl/Iozh – Output Leakage Current (+/-20uA)
    a. 0V & Vddq applied to all I/O Pins
    b. Measure Output Currents
    c. Record Highest Value
4. Voh(Low)– Output High Voltage (min) (>1.3V)
    a. Load 4 successive memory location with all 1's
    b. Continuously Read Pattern
    c. Measure outputs with -0.1mA load current
    d. Record lowest reading
5. Voh– Output High Voltage (min) (>0.87V)
    a. Load 4 successive memory location with all 1's
    b. Continuously Read Pattern
    c. With Rq = 250 ohms, force load current Ioh = -2mA
    d. Record lowest reading
6. Vol(Low) – Output Low Voltage (max) (<0.2V)
    a. Load 4 successive memory location with all 0's
    b. Continuously Read Pattern,
    c. Measure outputs with +0.1mA load current
    d. Record highest reading
7. Vol – Output Low Voltage (max) (<0.63V)
    a. Load 4 successive memory location with all 0's
    b. Continuously Read Pattern,
    c. With Rq = 250 ohms, force load current Ioh = 2mA
    d. Record highest reading
8. Vih - Input Logic Voltage for Proper Operation (<0.85V)
    a. VRef = Vary Vih in binary search sequence
    b. For every voltage level perform write/read of entire memory
    c. Record highest input voltage for which all memory locations pass

9. Vil - Input Logic Voltage for Proper Operation (>0.65V)
    a. Vary Vil in binary search sequence
    b. For every voltage level perform write/read of entire memory
    c. Record lowest input voltage for which all memory locations pass

Appendix B. Bias Conditions During Irradiation

VDD and VDDQ Pins = 1.9V
VSS Pins = 0V
Load Checkerboard pattern into all DUTs
Clock Frequency = 250MHz

Appendix C. Part Traveler and RunLog



JDI Rad Test Part Traveller - Dry Ice Shipment Option

Customer: DPAC1
Part Type: CYRS1643AV18 144M QDRII+ (RH)
Test Type: RLAT
DPA Job#: 40845514QC
CY Fab Lot#: 9729013 / K55HJ.05

Data log File (class 25C):							TID Test						Remote Facility					
								Time					Unpack			Finish Test		
DUT	D/C	Lot	Wafer	SN	Received Date	PreRad Char	Date	Start Rad	Stop Rad	Last Test	Package	Temp °C	Date	Time	Temp °C	Date	Time	Delta T
1	1850	9729013	9	1	4/12/2019	4/17/2019	4/25/2019	11:32	12:54	12:55	13:21	-80.5	4/26/2019	9:03	-78.6	4/26/2019	9:24	0:21
2	1850	9729013	9	2	4/12/2019	4/17/2019	→	→	→	12:59	→	→	→	9:28	-79.5	→	9:37	0:09
3	1850	9729013	9	3	4/12/2019	4/17/2019	→	→	→	13:01	→	→	→	9:34	-78.1	→	9:42	0:08
4	1850	9729013	9	4	4/12/2019	4/17/2019	→	→	→	13:03	→	→	→	9:38	-76.9	→	9:47	0:09
5	1850	9729013	9	5	4/12/2019	4/17/2019	→	→	→	13:03	→	→	→	9:43	-78.8	→	9:50	0:07
6	1850	9729013	9	6	4/12/2019	4/17/2019	→	→	→	13:06	→	→	→	9:48	-78.7	→	9:52	0:04
7	1850	9729013	9	7	4/12/2019	4/17/2019	→	→	→	13:08	→	→	→	9:51	-78.7	→	9:55	0:04
8	1850	9729013	9	8	4/12/2019	4/17/2019	→	→	→	13:10	→	→	→	9:53	-78.7	→	10:02	0:09
9	1850	9729013	9	9	4/12/2019	4/17/2019	→	→	→	13:12	→	→	→	9:56	-78.8	→	10:06	0:10
10	1850	9729013	9	10	4/12/2019	4/17/2019	→	→	→	13:14	→	→	→	1003	-78.7	→	10:09	0:06
11	1850	9729013	9	11	4/12/2019	4/17/2019	→	→	→	13:15	→	→	→	1005	-78.8	→	10:11	0:06
12	1850	9729013	9	12	4/12/2019	4/17/2019	4/25/2019	11:32	12:54	13:17	13:21	-80.5	4/26/2019	1010	-78.7	4/26/2019	10:14	0:04

TV1 Traveler

RUN#	Start Date/Time	SN	Bin# (1=Pass)	Radiation Level	Operator
7	17:43:39:60 - 4/22/2019	TV1-1	1	1	Jake Tausch
8	17:46:02:73 - 4/22/2019	TV1-2	1	1	Jake Tausch
9	17:48:08:35 - 4/22/2019	TV1-3	1	1	Jake Tausch
10	17:50:05:92 - 4/22/2019	TV1-4	1	1	Jake Tausch
11	17:51:58:98 - 4/22/2019	TV1-5	1	1	Jake Tausch
12	17:54:48:94 - 4/22/2019	TV1-6	1	1	Jake Tausch
13	17:56:59:20 - 4/22/2019	TV1-7	1	1	Jake Tausch
14	17:59:36:53 - 4/22/2019	TV1-8	1	1	Jake Tausch
15	18:01:26:72 - 4/22/2019	TV1-9	1	1	Jake Tausch
16	18:03:22:38 - 4/22/2019	TV1-10	1	1	Jake Tausch
17	18:05:13:78 - 4/22/2019	TV1-11	1	1	Jake Tausch
18	18:08:49:30 - 4/22/2019	TV1-12	1	1	Jake Tausch
19	18:10:54:58 - 4/22/2019	TV1-13	1	1	Jake Tausch
20	18:12:49:57 - 4/22/2019	TV1-14	1	1	Jake Tausch
21	18:15:01:36 - 4/22/2019	TV1-15	1	1	Jake Tausch
22	11:29:42:37 - 4/25/2019	TV1-13	1	250000	Jake Tausch
23	12:57:11:87 - 4/25/2019	TV1-1	1	250000	Jake Tausch
24	12:59:13:65 - 4/25/2019	TV1-2	1	250000	Jake Tausch
25	13:01:02:59 - 4/25/2019	TV1-3	1	250000	Jake Tausch
26	13:02:50:40 - 4/25/2019	TV1-4	1	250000	Jake Tausch
27	13:04:58:53 - 4/25/2019	TV1-5	1	250000	Jake Tausch
28	13:06:41:08 - 4/25/2019	TV1-6	1	250000	Jake Tausch
29	13:08:27:52 - 4/25/2019	TV1-7	1	250000	Jake Tausch
30	13:10:11:82 - 4/25/2019	TV1-8	1	250000	Jake Tausch
31	13:11:56:27 - 4/25/2019	TV1-9	1	250000	Jake Tausch
32	13:13:37:18 - 4/25/2019	TV1-10	1	250000	Jake Tausch
33	13:15:25:40 - 4/25/2019	TV1-11	1	250000	Jake Tausch
34	13:17:08:25 - 4/25/2019	TV1-12	1	250000	Jake Tausch
35	13:19:11:74 - 4/25/2019	TV1-14	1	250000	Jake Tausch
36	13:21:07:03 - 4/25/2019	TV1-15	1	250000	Jake Tausch
37	15:32:47:10 - 4/25/2019	TV1-13	1	400000	Jake Tausch
38	15:34:51:42 - 4/25/2019	TV1-14	1	400000	Jake Tausch
39	15:36:44:27 - 4/25/2019	TV1-15	1	400000	Jake Tausch

TV1 Run Log

Appendix D. Board Circuit Schematics

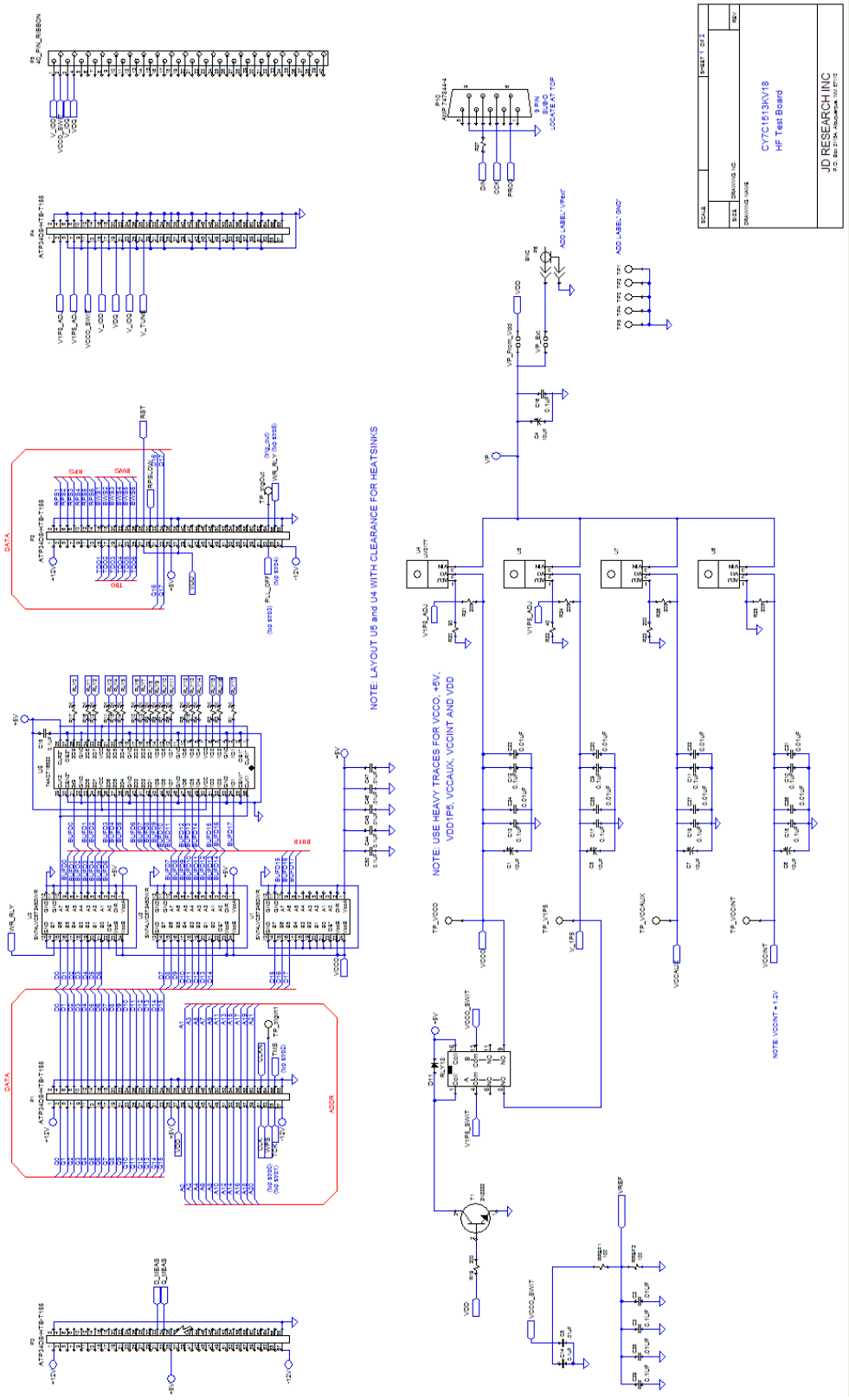


Figure D1. Test Board, Schematic 1 of 2

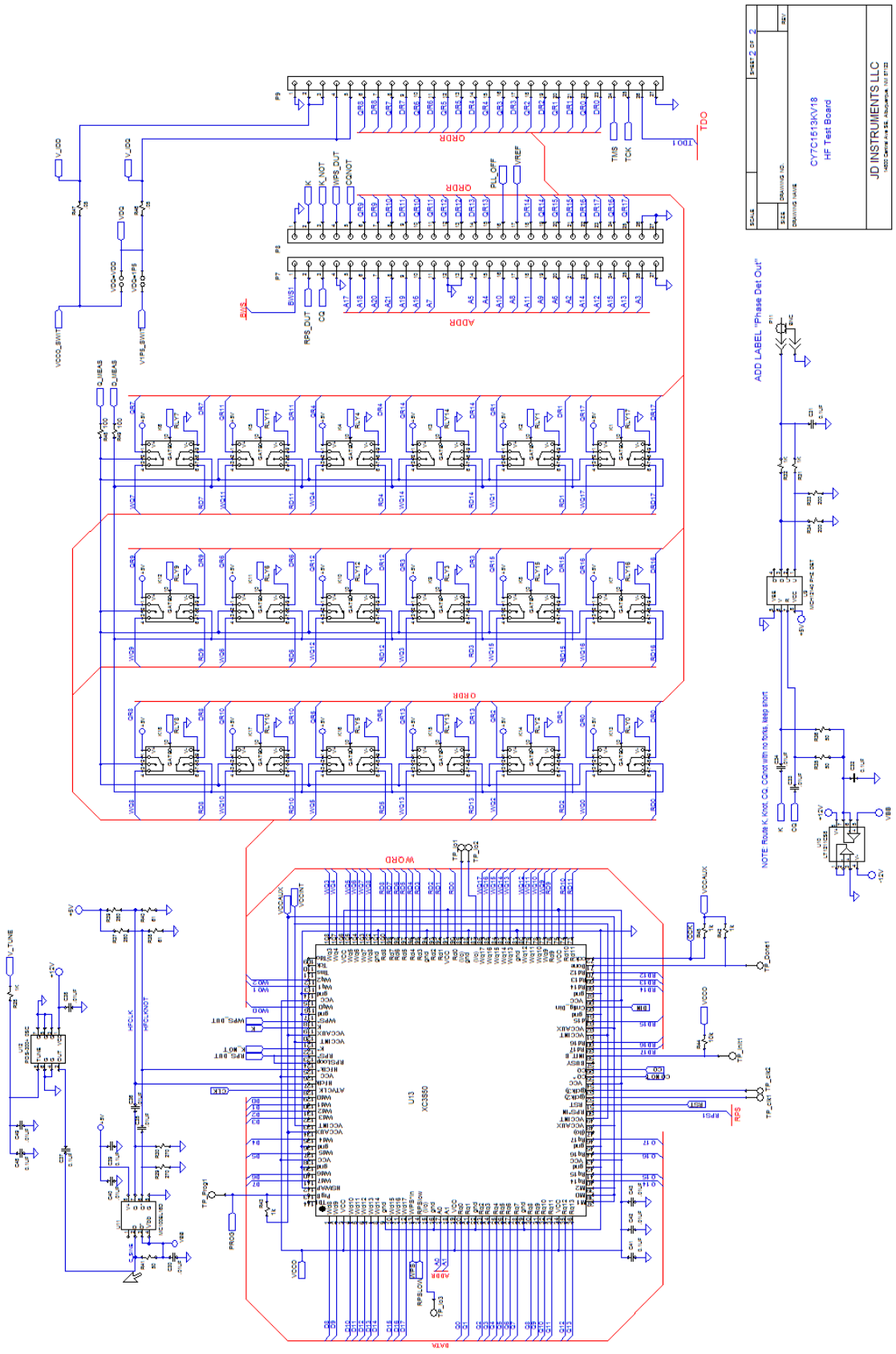


Figure D2. Test Board, Schematic 2 of 2

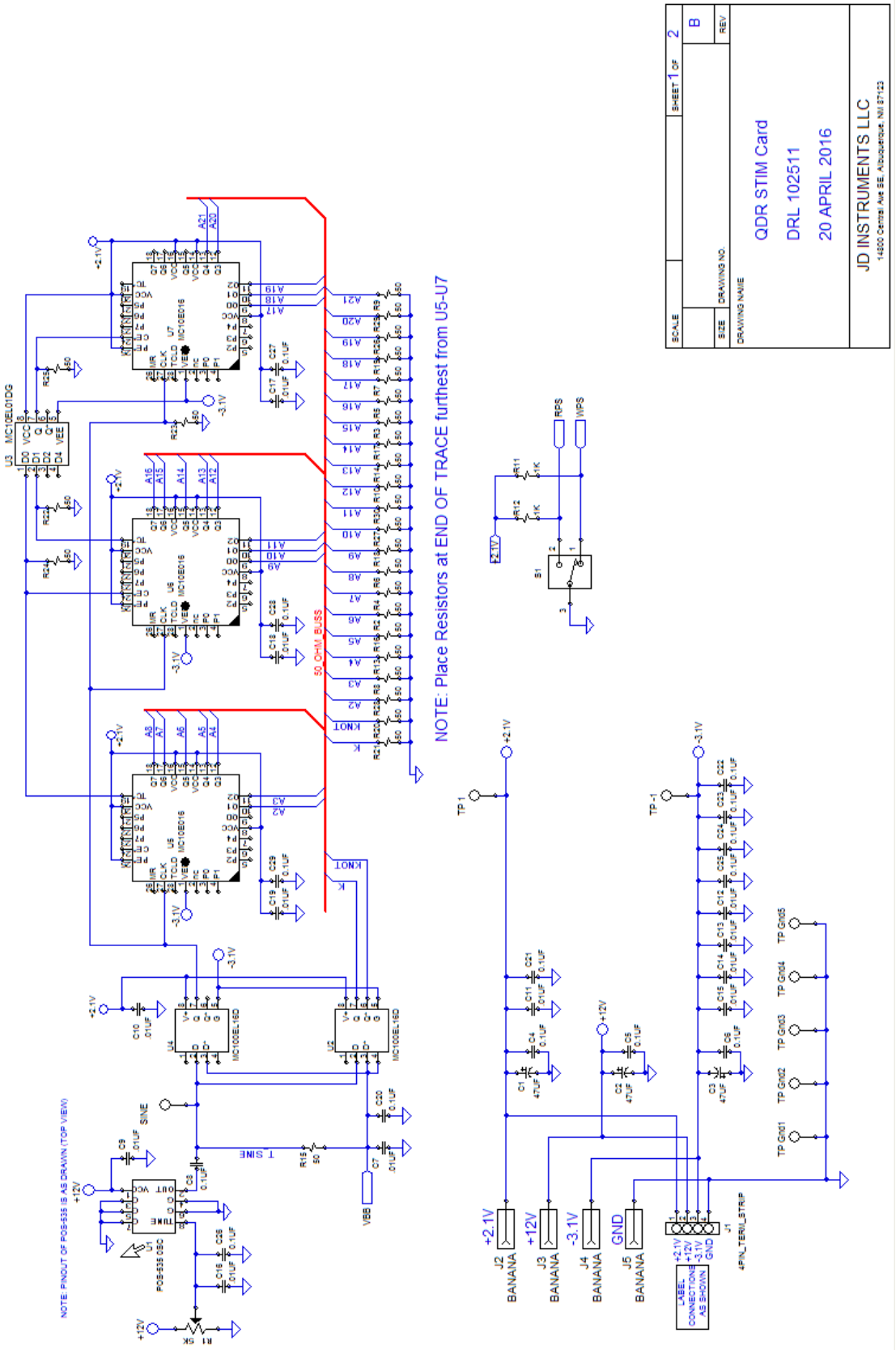


Figure D3. Stim Board, Schematic 1 of 2

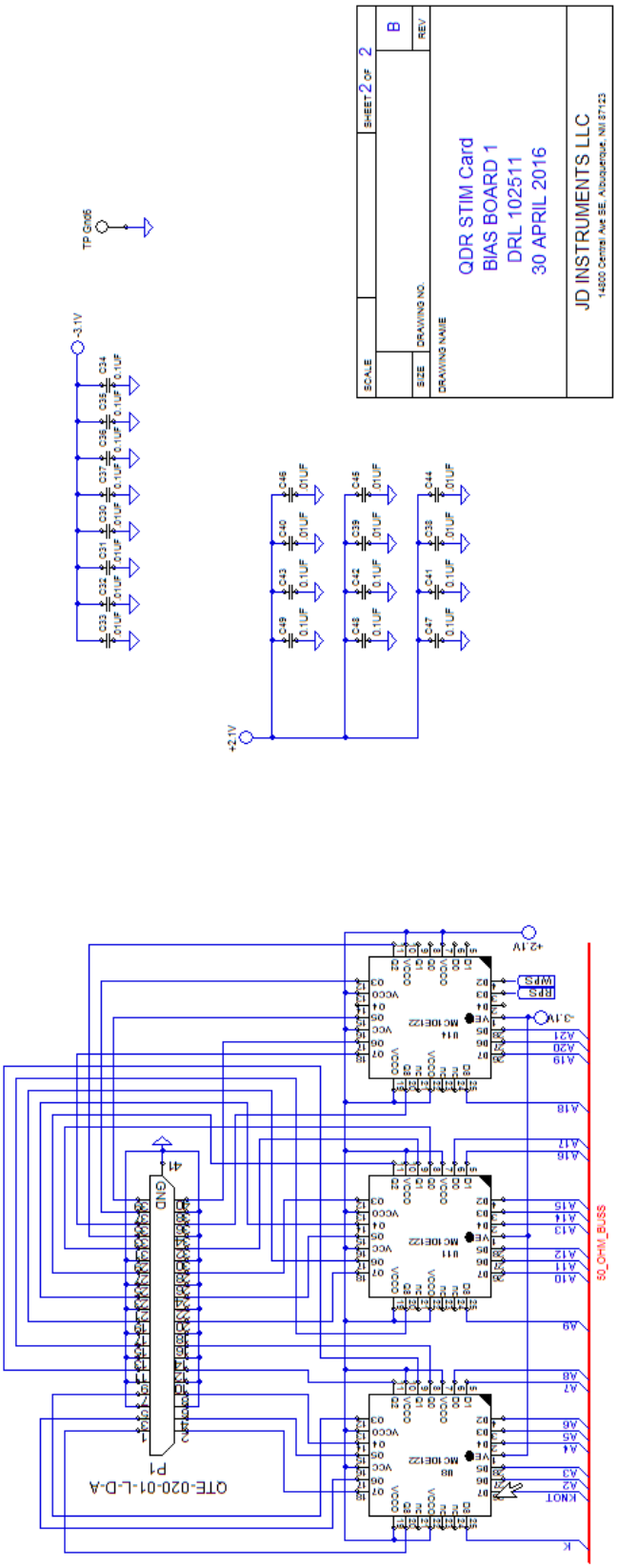


Figure D4. Stim Board, Schematic 2 of 2, Typical for each Channel

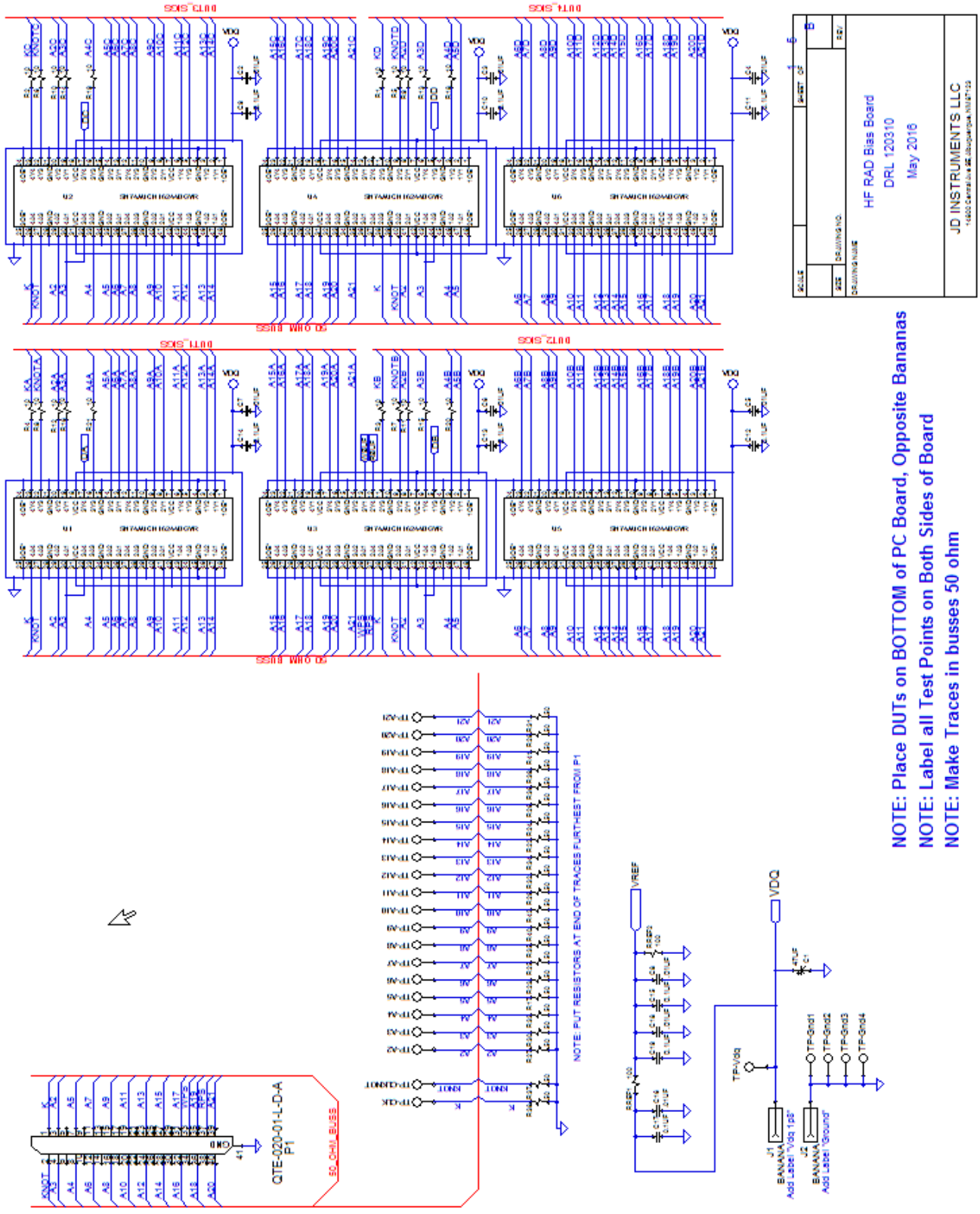


Figure D5. Bias Board, Schematic 1 of 2

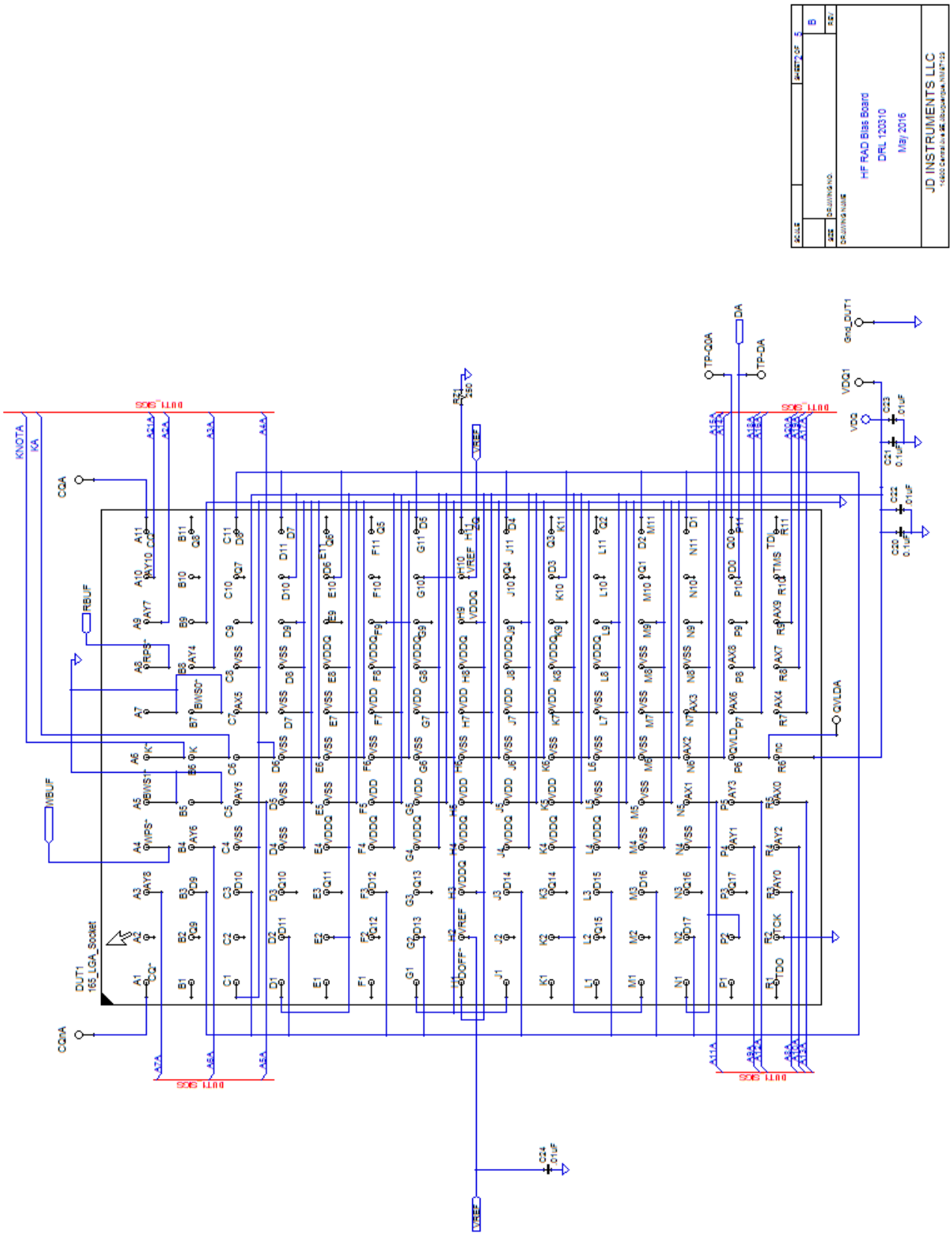


Figure D6. Bias Board, Schematic 2 of 2, Typical for each Socket