Cypress Semiconductor
Qualification Report

QTP# 98368
June 2013

SYNCHRONOUS/ASYNCHRONOUS DUAL PORT SRAM (3.3V AND 5V) R42HD TECHNOLOGY, FAB 4	
CY7C09079(V) CY7C09179(V)	32K x 8/9 Synchronous DP SRAM
CY7C09089(V) CY7C09189(V)	64K x 8/9 Synchronous DP SRAM
CY7C09099(V) CY7C09199(V)	128K x 8/9 Synchronous DP SRAM
CY7C09269(V) CY7C09369(V)	16K x16/18 Synchronous DP SRAM
CY7C09279(V) CY7C09379(V)	32K x 16/18 Synchronous DP SRAM
CY7C09289(V) CY7C09389(V)	64K x 16/18 Synchronous DP SRAM
CY7C008(V) CY7C018(V)	64K x 8/9 Asynchronous DP SRAM
CY7C009(V) CY7C019(V)	128K x 8/9 Asynchronous DP SRAM
CY7C027(V) CY7C037(V)	32K x 16/18 Asynchronous DP SRAM
CY7C028(V) CY7C038(V)	64K x 16/18 Asynchronous DP SRAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
98064	R42HD Technology qualified in Fab4 using 1 Meg SRAM product, die size 99 mils x 341mils	
98248	R42HD qualified with larger die size using 4 Meg SRAM product, die size 191 mils x 583 mils	

PRODUCT DESCRIPTION (for qualification)			
To qualify Synchronous/Asynchronous Dual Port SRAM in R42HD technology. Qualification			
Marketing Part #:	CY7C09389		
Device Description:	100 pins TQFP		
Cypress Division:	Cypress Semiconductor Corporation		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev A.	
What ID markings on Die:	7C0389A		

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al -5%Cu/1200Å TiW Metal 2: 500Å TiW/8000Å Al -5%Cu/300Å TiW
Passivation Type and Materials:		7000Å SiO_2 + 6000Å Si_3N_4	
Free Phosphorus contents in top glass layer(%):		0%	
Generic Process Technology/Design Rule (□-		CMOS, Double Metal /0.42 m	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 110Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor - Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R42HD	

PLASTIC PACKAGE/ASSEMBLY DESCRIPTION			
Package Outline, Type, or Name:	100-pin TQFP		
Mold Compound Name/Manufacturer:	Hitachi CEL 9200		
Lead Frame material:	Copper Alloy 194		
Lead Finish, composition:	Solder Plated, 90%Sn, 10%Pb		
Die Attach Area Plating:	Silver Spot		
Die Attach Method:	Epoxy	Die Attach Material:	Ablestik 8361H
Wire Bond Method:	Thermosonic	Wire Material/Size:	Gold / 1.0 mil
JESD22-A112 Moisture Sensitivity Level:	Level 3		
Name/Location of Assembly (prime) facility:	ASE, Taiwan (TAIWAN-G)		

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 5.75V 150 C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65 C to 150 C Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30C/60%RH)	P
High Temperature Storage	165C, No Bias	
Electrostatic Discharge Human Body Model (ESD-HBM)	1,100V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	1,000V JESD22-C101C	P
Latchup Sensitivity	12V, In accordance with JEDEC 17	P
Pressure Cooker Test	121^0C, 100%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH	P

RELIABILITY FAILURE RATE SUMMARY

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate[4]
High Temperature Operating Life Early Failure Rate[1]	1523 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[2,3] Long Term Failure Rate	791,500 DHRs	0	0.7	170	7 FIT

[1] Assuming an ambient temperature of 55□C and a junction temperature rise of 15□C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[5] Long Term Failure Rate is based on R42HD technology, 1 Meg/4 Meg SRAM qualifications.

Reliability Test Data

QTP #: 98368

Device	Assy-Loc	Fablot#	Assylot#	Duration	S/S	Rej	Fail Mode
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.75V)							
CY7C09389-AC	TAIWN-G	4818845	619806813	48	289	0	
CY7C09389-AC	TAIWN-G	4821104	619808005	48	1234	0	
STRESS: ESD-CHARGE DEVICE MODEL (1,000V)							
CY7C09389-AC	TAIWN-G	4818845	619806221	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (1,100V)							
CY7C09389-AC	TAIWN-G	4818845	619806221	COMP	3	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C09389-AC	TAIWN-G	4818845	619806221	168	44	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C09389-AC	TAIWN-G	4818845	619806221	300	48	0	
CY7C09389-AC	TAIWN-G	4818845	619806221	1000	48	0	

Reliability Test Data

QTP #: 98064

Device	Assy-Loc	Fablot#	Assylot#	Duration	S/S	Rej	Fail Mode
STRESS: ESD-CHARGE DEVICE MODEL, 1000V							
CY7C109-VC	INDNS-O	4738602	519712560	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2200V							
CY7C109-VC	INDNS-O	4738602	519712560	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (140C, 5.5V, 85% RH), PRECOND. 192 HRS 30C/60%RH							
CY7C109-VC	INDNS-O	4738602	519712560	128	46	0	
CY7C109-VC	INDNS-O	4738564	519712898	128	46	0	
CY7C109-VC	INDNS-O	4738564	519712898	256	46	0	
CY7C109-VC	INDNS-O	4739644	519714390	128	46	0	
STRESS: HIGH TEMPERATURE STORAGE (165C, NO BIAS)							
CY7C109-VC	INDNS-O	4738602	519712560	336	46	0	
CY7C109-VC	INDNS-O	4738602	519712560	500	46	0	
CY7C109-VC	INDNS-O	4738602	519712560	1000	46	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 5.75V)							
CY7C109-VC	INDNS-O	4738602	519712560	80	78	0	
CY7C109-VC	INDNS-O	4738602	519712560	168	78	0	
CY7C109-VC	INDNS-O	4739644	519714390	80	78	0	
CY7C109-VC	INDNS-O	4739644	519714390	168	78	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 5.75V)							
CY7C109-VC	INDNS-O	4739644	519714390	80	528	0	
CY7C109-VC	INDNS-O	4739644	519714390	500	527	0	
CY7C109-VC	INDNS-O	4745042	519800651L1	80	529	0	
CY7C109-VC	INDNS-O	4745042	519800651L1	500	529	0	
STRESS: EXTENDED DYNAMIC BURN-IN (150C, 5.75V)							
CY7C109-VC	INDNS-O	4739644	519714390	1000	527	0	
STRESS: COLD LIFE TEST (-30C, 6.5V)							
CY7C109-VC	INDNS-O	4738602	519712560	500	45	0	
CY7C109-VC	INDNS-O	4738602	519712560	1000	45	0	

Reliability Test Data

QTP #: 98064

Device	Assy-Loc	Fablot#	Assylot#	Duration	S/S	Rej	Fail Mode
STRESS:	***READ & RECORD LIFE TEST (150C, 5.75V)***						
CY7C109-VC	INDNS-O	4738602	519712560	48	10	0	
CY7C109-VC	INDNS-O	4738602	519712560	500	10	0	
STRESS:	***TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH***						
CY7C109-VC	INDNS-O	4738602	519712560	300	46	0	
CY7C109-VC	INDNS-O	4738602	519712560	1000	46	0	
CY7C109-VC	INDNS-O	4738564	519712898	300	46	0	
CY7C109-VC	INDNS-O	4739644	519714390	300	46	0	

Document History Page

Document Title: QTP # 98368 : SYNCHRONOUS/ASYNCHRONOUS DUAL PORT SRAM (3.3V AND 5V) , 7C0xxxx, R42HD TECHNOLOGY, FAB 4
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Rev.	ECN No.	Orig. of Change	Description of Change
**	4026931	ILZ	Initial Spec Release Qualification report published on Cypress.com is not in spec format. Initiated spec for QTP 98368 and removed all Cypress reference spec and replaced with Industry standard. Updated package availability based on current qualified assembly

Distribution: WEB

Posting: None