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Cypress Semiconductor Product Qualification Report

**QTP# 144504 VERSION*B
August 2016**

36 Meg Standard Synchronous and NoBL Family LL65P-25ODR Technology, UMC Fab 12A	
CY7C1440KV25	36-Mbit (1M x 36) Pipelined Sync SRAM
CY7C1440KV33	
CY7C1440KVE33	36-Mbit (1M x 36) Pipelined Sync SRAM (with ECC)
CY7C1441KV25	36-Mbit (1M x 36) Flow-through SRAM
CY7C1441KV33	
CY7C1441KVE33	36-Mbit (1M x 36) Flow-through SRAM (with ECC)
CY7C1442KV33	36-Mbit (2M x 18) Pipelined Sync SRAM
CY7C1443KV33	36-Mbit (2M x 18) Flow-through SRAM
CY7C1444KV33	36-Mbit (1M x 36) Pipelined DCD Sync SRAM
CY7C1445KV33	36-Mbit (2M x 18) Pipelined DCD Sync SRAM
CY7C1460KV25	36-Mbit (1M x 36) Pipelined SRAM with NoBL™ Architecture
CY7C1460KV33	
CY7C1460KVE25	36-Mbit (1M x 36) Pipelined SRAM with NoBL™ Architecture (with ECC)
CY7C1460KVE33	
CY7C1461KV33	36-Mbit (1M x 36) Flow-through SRAM with NoBL™ Architecture
CY7C1462KV25	36-Mbit (2M x 18) Pipelined SRAM with NoBL™ Architecture
CY7C1462KV33	
CY7C1462KVE25	36-Mbit (2M x 18) Pipelined SRAM with NoBL™ Architecture (with ECC)
CY7C1462KVE33	
CY7C1463KV33	36-Mbit (2M x 18) Flow-through SRAM with NoBL™ Architecture

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT

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QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date Comp
091706	Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device CY7C1553K Base Die Product Family	Aug 2009
144504	Qualification of 36 Meg Standard Synchronous and NoBL Family , LL65P-25ODR Technology at UMC Fab 12A	April 2015
160902	Qualification of LL65 Sync NoBL 36M Family for New Military Temperature Range (-55C to 125C) at Backend Testing	June 2016

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify 36 Meg Standard Synchronous and NoBL Family , LL65P-25ODR Technology at UMC Fab 12A
Marketing Part #:	CY7C1440KV25/ CY7C1440KV33/ CY7C1440KVE33/ CY7C1441KV25/CY7C1441KV33/ CY7C1441KVE33/ CY7C1442KV33/ CY7C1443KV33/CY7C1444KV33/ CY7C1445KV33/ CY7C1460KV25/ CY7C1460KV33/ CY7C1460KVE25/ CY7C1460KVE33/ CY7C1461KV33/ CY7C1462KV25/CY7C1462KV33/ CY7C1462KVE25/ CY7C1462KVE33/ CY7C1463KV33
Device Description:	LL65 36 Meg Sync/NoBL SRAM
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65P-18R			
Number of Metal Layers:	5+RDL	Metal Composition:	Metal 1: Cu 0.18um Metal 2: Cu 0.22um Metal 3: Cu 0.22um Metal 4: Cu 0.36um Metal 5: Cu 1.25um Metal 6 (RDL): Al 1.2um
Passivation Type and Materials:	0.4um Oxide / 0.5um Nitride		
Number of Transistors in Device	~600M		
Number of Logic Gates in Device	~300M		
Generic Process Technology/Design Rule (μ-drawn):	65nm		
Gate Oxide Material/Thickness (MOS):	19.5A		
Name/Location of Die Fab (prime) Facility:	UMC Fab 12		
Die Fab Line ID/Wafer Process ID:	LLL65P-25ODR		

PACKAGE AVAILABILITY

PACKAGE	WIRE MATERIAL	ASSEMBLY FACILITY SITE	QTP NUMBER
165 FBGA	CuPd	CML-RA	QTP# 144603
100L TQFP	CuPd	CML-RA	QTP# 150503

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165/BW165
Package Outline, Type, or Name:	165-Fine Ball Grid Array (15x17x1.4mm)
Mold Compound Name/Manufacturer:	GR9810/Henkel
Mold Compound Flammability Rating:	UL-94 V0
Oxygen Rating Index:	54% (typical) / 28 (min. value)
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	SAC405
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Saw
Die Attach Supplier:	Henkel
Die Attach Material:	ATB125-US1 Die Attach Film
Bond Diagram Designation:	001-95407/ 001-69504
Wire Bond Method:	Thermosonic
Wire Material/Size:	CuPd, 0.8 mil
Thermal Resistance Theta JA °C/W:	14.24°C/W
Package Cross Section Yes/No:	No
Assembly Process Flow:	11-21099
Name/Location of Assembly (prime) facility:	CML-RA
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-RA

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	AZ100
Package Outline, Type, or Name:	100L-Thin Quad Flat Package (14x20x1.4mm)
Mold Compound Name/Manufacturer:	G700SY/Sumitomo
Mold Compound Flammability Rating:	UL-94 V0
Oxygen Rating Index:	54% (typical) / 28 (min. value)
Leadframe Material:	Copper
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Saw
Die Attach Supplier:	Henkel
Die Attach Material:	QMI 509
Bond Diagram Designation:	001-69322/001-95403
Wire Bond Method:	Thermosonic
Wire Material/Size:	CuPd, 0.8 mil
Thermal Resistance Theta JA °C/W:	35.36°C/W
Package Cross Section Yes/No:	No
Assembly Process Flow:	11-21099
Name/Location of Assembly (prime) facility:	CML-RA
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-RA

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Dynamic Latch-up	JESD78	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V/750V/1,000V/1,250V/1,500V/2,000V JESD22-C101	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1,100V/2,200V/3,300V/4,000V/5,000V/6,000V JESD22-A114	P
Electrostatic Discharge Machine Model (ESD-MM)	200V, JESD22-A115	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 85%RH, 2.25V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C Dynamic Operating Condition, 2.5V, 150°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C /150°C Dynamic Operating Condition, 2.5V, 150°C JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V, 150°C JESD22-A108	P
High Temperature Storage	JESD22-A103:150°C No bias	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.25V, -30°C Dynamic Operating Condition, Vcc = 3.3V, -55°C JESD22-A108	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at LFR 0hr,80hrs, 500hrs & 1000hrs	P
Soft Error (Alpha Particle)	JESD89	P
Static Latch-up	85°C , ± 140mA/85°C , ± 200mA 125°C , ± 140mA/125°C , ± 240mA JESD78	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Temperature Humidity Bias Test (THB)	JESD22-A101: 85°C/ 85% RH , 2.25V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF ³	Failure Rate
High Temperature Operating Life Early Failure Rate ¹	1,261 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life ² Long Term Failure Rate (150°C)	187,000 DHRs	0	0.7	170	18 FIT
High Temperature Operating Life ² Long Term Failure Rate (125°C)	356,000 DHRs	0	0.7	55	

¹ Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

² Chi-squared 60% estimations used to calculate the failure rate..

³ Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[\frac{E_A}{k} \left[\frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E_A =The Activation Energy of the defect mechanism.

K = Boltzmann's constant = 8.62x10⁻⁵ eV/Kelvin.

T₁ is the junction temperature of the device under stress and T₂ is the junction temperature of the device at use conditions.

¹Early Failure Rate was computed from QTP# 160902 data.

² Long Term Failure Rate was computed from QTP# 091706, QTP# 144504 and QTP# 160902 data.

Reliability Test Data

QTP #:091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	

Reliability Test Data

QTP #:091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
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STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V

CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	500	178	0	
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STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V

CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
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CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	
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STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max

CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	
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STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C

CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
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STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc

CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
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STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
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CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
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CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	
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STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR

CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
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STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA

CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
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CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
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CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
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CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	
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STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
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CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
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CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	
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STRESS: TEMPERATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
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Reliability Test Data

QTP #:091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
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STRESS: SER – ALPHA PARTICLE, 3-TEPM, 3-VOLTAGE, @ 85C, Vcc Nom

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
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STRESS: X-SECTION/STEM XY AUDIT

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		
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Reliability Test Data

QTP #:144504

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	COMP	15	0	
STRESS: ESD-CHARGE DEVICE MODEL							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	500	9	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	750	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	1000	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	1250	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	1500	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	1750	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	2000	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	1100	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	2200	8	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	3300	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	4000	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	5000	3	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	6000	3	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	COMP	5	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.5V							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	48	1499	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE –REG-ON, 150C, 2.5V							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	48	45	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.5V							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	80	116	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	500	116	0	

Reliability Test Data

QTP #:144504

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRE/POST LFR CRITICAL PARAMETERS							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	0	10+2	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	80	10+2	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	500	10+2	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	168	80	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	288	80	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.4V, +/-140mA							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	COMP	6	0	
STRESS: STATIC LATCH-UP TESTING, 85C, 5.94V, +/-200mA							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, +/-140mA							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	COMP	3	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	500	79	0	
CY7C1460KVE25 (7CP14602K)	9441004	611446421	CML-RA	1000	79	0	

Reliability Test Data

QTP #:160902

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
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STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.5V

CY7C1441KV33 (7CP1441KO)	9551005	611613848N	CML-RA	48	350	0	
CY7C1461KV33 (7CP1461KO)	9441005	611521359P1	CML-RA	48	283	0	
CY7C1441KV33 (7CP1441KO)	9441004	611505210P2	CML-RA	48	196	0	
CY7C1441KVE33 (7CP1441KO)	9441004	611523764P2	CML-RA	48	432	0	

STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.5V

CY7C1441KV33 (7CP1441KO)	9551005	611613848N	CML-RA	500	80	0	
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STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -55C, 3.3V

CY7C1441KV33 (7CP1441KO)	9441005	611521356	CML-RA	1000	32	0	
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Document History Page

Document Title: QTP# 144504: 36 MEG SYNCHRONOUS NOBL FAMILY,LL65P-25ODR TECHNOLOGY, UMC
FAB 12A
Document Number: 001-97372

Rev.	ECN No.	Orig. of Change	Description of Change
**	4744116	JYF	Initial spec release.
*A	4798763	JYF	Changed QTP title from "36 Meg Synchronous NoBL Family LL65P-25ODR Technology, UMC Fab 12A" to "36 Meg Standard Synchronous and NoBL Family LL65P-25ODR Technology, UMC Fab 12A" in QTP title page (page 1); Aligned qualification purpose in pages 2 & 3.
*B	5391821	JYF	Added QTP# 160902 data (LL65 Sync NoBL 36M Family for New Military Temperature Range).
		SLLO	Updated CY logo with new tag line. Removed Distribution and Posting from the document history page.

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