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Cypress Semiconductor
Product Qualification Report

QTP#140303
January 2014
Simtek: 05-51-029

Simtek 256K 5V nvSRAM Product Qualification 0.8*u*m Technology, Chartered Semiconductor Fab2	
STK11C88-N	**256K (32kx8) 5V nvSRAM**
STK11C88-S	**256K (32kx8) 5V nvSRAM**
STK11C88-P	**256K (32kx8) 5V nvSRAM**
STK11C88-W	**256K (32kx8) 5V nvSRAM**
STK14C88-N	**256K (32kx8) 5V nvSRAM**
STK14C88-W	**256K (32kx8) 5V nvSRAM**
STK15C88-N	**256K (32kx8) 5V nvSRAM**
STK15C88-S	**256K (32kx8) 5V nvSRAM**
STK15C88-P	**256K (32kx8) 5V nvSRAM**
STK15C88-W	**256K (32kx8) 5V nvSRAM**
STK16C88-W	**256K (32kx8) 5V nvSRAM**

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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
05-51-029		Semtek CSM2 256K 5V nvSRAM Products		Mar 2005
140303		Simtek Qualification Report Integration – Paper Qualification		Dec 2008

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PRODUCT QUALIFICATION REPORT

Fab Line Change: 256K 5V nvSRAM Products

SUMMARY

Simtek is changing the production line at its Chartered Semiconductor Manufacturing wafer supplier in Singapore from its older Fab 1 line to its newer Fab 2 line at the same location. As the fab line changes, the revision level will change from Rev. C (Fab 1) to Rev D (Fab 2). There is no change in the design of the die and the process used in Fab 2 will continue to be the same .8 micron process that has been used in Fab 1. There are no changes to any electrical or mechanical data sheet specifications. To ensure consistency of product characteristics, Simtek has done a comparison of the electrical performance between devices manufactured in Fab 1 and Fab 2. This report details the results of this comparison and confirms the consistent characteristics of product built on both Fab lines.

PRODUCT AFFECTED

Simtek 256K 32Kx8 5V nvSRAM.

PART NUMBERS AFFECTED

STK11C88-N	STK15C88-N
STK11C88-S	STK15C88-S
STK11C88-P	STK15C88-P
STK11C88-W	STK15C88-W
STK14C88-N	STK16C88-W
STK14C88-W	

- All speed grades.
- All temperature grades.

NEW PRODUCT DESIGN REV ID

Products out of Fab 2 will be marked "**Simtek D**" on the first line of the topside mark. The previous revision ID was "Simtek C".

CHANGE DETAIL

- ❑ This line move is from Chartered Semiconductor's Fab 1 [CSM1] to Fab 2 [CSM2].
- ❑ The Simtek nvSRAM design has been transferred to the new line without change.
- ❑ The product is being built to the same 0.8 micron design as in CSM1.
- ❑ The CSM2 product meets the current datasheet specifications as published on the Simtek website [www.Simtek.com].
- ❑ No changes are being made in assembly or final test & burn-in.

DATA SUPPORTING CHANGE

Appendix A - Process Characterization Report:
Comparison of CSM1 and CSM2 key process parameters affecting device functionality.

Appendix B - Product Characterization Report:
Comparison of key product datasheet parameters between the CSM1 and CSM2 products.

Appendix C - Qualification Lifetest Schedule:
Life test methods, conditions and readpoint schedule.

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Appendix A

Process Characterization Report

Comparison of CSM1 and CSM2 key process parameters affecting device functionality.

Parameter	Unit	% Change	Comments
NLLS Vtlin	Volt	6%	
NLLS Idsat	mA	-3%	
NLLS Bvdss	Volt	3%	
PLLS Vtlin	Volt	4%	
PLLS Idsat	mA	-5%	
PLLS Bvdss	Volt	2%	
NHLS Vtlin	Volt	10%	
NHLS Idsat	mA	-5%	
NHLS Bvdss	Volt	8%	
PHLS Idsat	mA	-3%	
PHLS Bvdss	Volt	4%	
SNOS Icell Ik	uA	0%	
VMG Positive Vstop	Volt	1%	
VMG Negative Vstop	Volt	1%	
NLV Bkn	Volt	1%	
PLV Bkn	Volt	0%	
NHV Bkn	Volt	3%	
PHV Bkn	Volt	2%	
NLP1 Vtsat	Volt	-7%	
NHP 2 Vtsat	Volt	-6%	
Ndiff	Ohm/Sq	-4%	
Pdiff	Ohm/Sq	-5%	
Npoly1	Ohm/Sq	-3%	
NPoly2	Ohm/Sq	8%	
N Contact	Ohm	4%	
P Contact Ohm/con	Ohm	27%	* Due to use of different/better barrier metal material
M1/M2 Via	Ohm	-8%	
Buried Contact 1 Rcon	Ohm	4%	
Buried Contact 2 Rcon ohm/con	Ohm	2%	

Summary

Absolute wafer level e-parameter values are proprietary to Simtek and the Wafer Foundry.

All values Rev D [CSM2] process correlate well with the original Rev C [CSM1] process and remain well within the original CSM1 process specification limits.

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Appendix B

Product Characterization Report

Comparison of key product datasheet parameters between CSM1 [Fab 1, Rev C] and CSM2 [Fab 2, Rev D] products.

Product Tested

- STK14C88
- Package: "N" type Plastic 32-pin 300mil SOIC

Test Conditions

- Standard set of all characterization parameters
- 5 temperatures (-40C, 0C, 25C, 70C, 85C).
- 5 voltages (4.0V, 4.5V, 5.0V, 5.5V, 6.0V).

Applicable Devices
The characterization data applies to all devices listed on page 1 of this report. All devices are built from the same die with different bond-outs.

Data Analysis
The following table shows the datasheet parameters, specification limits, the CSM2 [Product Revision D] margin to specification and the change in margin to spec from CSM1 to CSM2. Where the change in margin to spec column shows a positive number that indicates FAB2 material has more margin than FAB1. Negative numbers in the margin to spec column indicate less margin to spec for FAB2 compared to FAB1. The parameter values are derived from the worst case averages of commercial temperature (0C to 70C) and voltage (4.5V to 5.5V) conditions for samples from each fab. All testing was performed at the same time on the same tester, hardware, and program.

Summary
Rev D product remains well within the current datasheet specifications with adequate margin on all parameters. Value changes between product revision parameters are nominal and should not affect in-system performance.

Comparison to the -45ns spec the following parameters do not meet the minimum Cpk requirement of 1.3, or are out of datasheet specification.

1. HLQZ	Cpk is 0.6	Adjust to improve process margin
2. ICC4	Cpk is 1.1	Adjust to improve process margin
3. VOL	Cpk is 1.0	Adjust to improve process margin

Corrective Actions
Minor design and Process adjustments to improve process capability measure on the above parameters.

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Symbol	#	Parameter	35ns Spec		Margin to spec Fab2	Difference Fab2 to Fab1	Fab2 Cpk	Comment
			MIN	MAX				
READ CYCLE								
ELQV	1	Chip Enable Access Time		35ns	12.3ns	1.7	10.2	
AVAV	2	Read Cycle Time	35ns		14.3ns	1.3	11.9	
AVQV	3	Address Access Time		35ns	10.8ns	2.2	9.0	
GLQV	4	Output Enable to Data Valid		15ns	9.9ns	0.7	6.6	
AXQX	5	Output Hold after Address Change	5ns		10.7ns	1.0	4.4	
ELQX	6	Chip Enable to Output Active	5ns		11.4ns	1.1	9.5	
EHQZ	7	Chip Enable to Output Inactive		13ns	8ns	0.4	4.4	
GLQX	8	Output Enable to Output Active	0ns		4.5ns	0.9	3.7	
GHQZ	9	Output Enable to Output Inactive		13ns	7.8ns	0.6	8.6	
ELICCH	10	Chip Enable to Power Active	0ns		See Note	N/A	N/A	Guaranteed not tested
EHICCL	11	ChipDisable to Power Standby		35ns	See Note	N/A	N/A	Guaranteed not tested
WRITE CYCLE #1								
AVAV	12	Write Cycle Time	35ns		14.3ns	1.3	11.9	
WLWH	13	Write Pulse Width	25ns		12.2ns	0.1	8.1	
ELWH	14	Chip Enable to End of Write	25ns		13.6ns	0.0	11.3	
DVWH	15	Data Set-up to End of Write	12ns		5.4ns	0.0	9.0	
WHDX	16	Data Hold after End of Write	0ns		2.7ns	-0.3	3.0	
AVWH	17	Address Set-up to End of Write	25ns		15.3ns	0.7	6.3	
AVWL	18	Address Set-up to Start of Write	0ns		4.4ns	-0.1	4.8	
WHAX	19	Address Hold after End of Write	0ns		1.8ns	0.4	6.0	
WLQZ	20	Write Enable to Output Disable		13ns	5.9ns	0.4	9.8	
WHQX	21	Output Active after End of Write	5ns		12.9ns	-6.3	14.3	
WRITE CYCLE #2								
AVAV	12	Write Cycle Time	35ns		14.3ns	1.3	11.9	
WLEH	13	Write Pulse Width	25ns		12.1ns	0.3	13.4	
ELEH	14	Chip Enable to End of Write	25ns		13.1ns	0.3	21.8	
DVEH	15	Data Set-up to End of Write	12ns		5.3ns	0.1	5.8	
EHDX	16	Data Hold after End of Write	0ns		2.9ns	-0.5	4.8	
AVEH	17	Address Set-up to End of Write	25ns		14.9ns	1.0	7.1	
AVEL	18	Address Set-up to Start of Write	0ns		3.1ns	-0.3	5.1	
EHAX	19	Address Hold after End of Write	0ns		2.7ns	-0.5	4.5	
HARDWARE STORE CYCLE								
HLHZ	22	Store Cycle Duration		10mS	4.1mS	-1.3	4.5	
HLQZ	23	Time allowed to complete SRAM cycle	1uS		0.18uS	-0.2	0.6	See corrective actions
HHQX	24	Hardware Store High to Inhibit Off		700ns	350ns	-55.0	2.3	
HLHX	25	Hardware Store Pulse Width	15ns		10.7ns	0.1	11.8	
HLBL	26	Hardware Store Low to Store Busy		300ns	201ns	-14.0	6.7	

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Symbol	#	Parameter	35ns Spec		Margin to spec Fab2	Difference Fab2 to Fab1	Fab2 Cpk	Comment
AUTOSTORE / POWER-UP RECALL								
RESTORE	27	Power-Up Recall Duration		550uS	N/A		N/A	Not tested
HLHZ	28	Store Cycle Duration		10mS	4.1mS	-1.3	4.5	
VSBL	29	Vswitch to HSB\ Low		300ns	201ns	-14.0	6.7	
BLQZ	30	Time to complete SRAM cycle	1uS		0.4uS	0.1	1.3	
VSWITCH	31	Low Voltage Trigger Level	4.0V	4.5V	0.2V	0.1	1.3	
VRESET	32	Low Voltage Reset Level		3.6V	1.7V	0.0	5.5	
SOFTWARE-CONTROLLED STORE / RECALL								
AVAV	12	Write Cycle Time	35ns		14.3ns	1.3	3.5	
AVEL	34	Address Setup Time	0ns		3.1ns	-0.3	5.1	
ELEH	35	Clock Pluse Width	25ns		13.1ns	0.3	14.5	
ELAX	36	Address Hold Time	20ns		8.1ns	0.3	13.5	
RECALL	37	Recall Duration		20us	8ns	-2.7	8.8	
DC CHARACTERISTICS								
ICC1		Ave Vcc Current @ AVAV=35ns		80mA	22.8mA	-13.8	3.8	
ICC2		Ave Vcc Current During Store		3mA	1.1mA	0.0	7.3	
ICC3		Ave Vcc Current @200ns, 3.3V, 25C		10mA	0.7mA	-0.4	N/A	Ave value measured
ICC4		Ave Vcap Current during Autostore		2mA	0.1mA	1.7	1.1	See corrective actions
ISB1		Ave Vcc Standby Current @AVAV = 35ns		25mA	6.4mA	-5.4	5.3	
ISB2		Vcc Standby Current		1.5mA	0.65mA	0.0	10.8	
ILKG		Input Leakage Current	-1uA	1uA	N/A	N/A	N/A	Not tested
IOLKG		Off-State Output Leakage Current	-5uA	5uA	N/A	N/A	N/A	Not tested
VIH		Input Logic "1" Level	2.2V		0.6V	0.0	1.9	
VIL		Input Logic "0" Level		0.8V	0.3V	-0.1	1.3	
VOH		Output Logic "1" Voltage	2.4V		1.5V	-0.1	25.6	
VOL		Output Logic "0" Voltage		0.4V	0.18V	0.0	1.0	See corrective actions
VOLBU		Logic "0" Voltage on HSB\ Output		0.4V	0.3V	0.0	10.2	

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Appendix C

Qualification Lifetest Report

CSM2 0.8µ CMOS/SNOS Process, Simtek 256K 5V nvSRAM

Test	Method	Conditions	Readpoint	Start Qty	# of Failures	Failure Detail
High Temperature Operating Life [HTOL]	JESD-22 A108	Dynamic Full SRAM Array 125C Vcc nom 4 Fab Lots	0 hrs	467	0	
			168 hrs	467	0	
			500 hrs	467	0	
			1000 hrs	467	0	3 lots. zero fails @ 1K hrs.
Retention	Simtek	Unbiased Bake 150C Store nv array at 0 hr Read stored data at read points 4 Fab Lots	0 hrs	400	0	
			48 hrs	400	0	
			168 hrs	400	1	1 fail at 10yr/70C equivalent[1] Corrective action: Adjust retention screen limit.
			500 hrs	399	1	1 fail at 10yr/85C equivalent[1] Corrective action: Adjust retention screen limit.
			1000 hrs	398	0	4 lots. 2 fails through 1K hrs[1] Corrective actions complete & verified.
Endurance	Simtek	Store/Recall cycles of nv array Recall and Functional check at read points	0 cycles	269	0	
			100K cycles	269	0	
			500K cycles	269	0	
			1M cycles	269	0	3 lots. Zero fails @ 1M cycles.
ESD	JEDSD22 A114	Human Body Model		5	0	Pass 1.8KV
Latch-Up Integrity	JEDEC 78	± 100mA, 70C		6	0	Pass ±100mA, 70C

Note 1: 2 failures recorded in retention testing [store NV array followed by unbiased bake with interim readpoints to verify stored data pattern is no corrupted and all cells read correct data state]. Wafer level retention screening limits adjusted to provide greater margin against Data Sheet Retention specification.

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**	4251901	ZIJ	Initial spec release.

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