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Cypress Semiconductor
Product Qualification Report

QTP#140302
January 2014
Simtek: 05-51-035

Simtek 64K 5V nvSRAM SMD Product Qualification 0.8um Technology, Chartered Semiconductor Fab2	
5962-9459903MXC	**STK12C68-5C35M**
5962-9459902MXC	**STK12C68-5C45M**
5962-9459901MXC	**STK12C68-5C55M**
5962-9459903MXA	**STK12C68-5K35M**
5962-9459902MXA	**STK12C68-5K45M**
5962-9459901MXA	**STK12C68-5K55M**
5962-9459903MYA	**STK12C68-5L35M**
5962-9459902MYA	**STK12C68-5L45M**

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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
05-51-035		CSM2 64K 5V SMD nvSRAM Products		Mar 2005
140302		Simtek Qualification Report Integration – Paper Qualification		Dec 2008

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PRODUCT QUALIFICATION REPORT

Fab Line Change: 64K 5V SMD nvSRAM Products

SMD 5962-94599 STK12C68

Issue 00 Date 31 March 2005

SUMMARY

The wafer foundry line for Simtek 64K nvSRAM SMD products has changed from Fab 1 to Fab 2 at Chartered Semiconductor Manufacturing in Singapore. The revision level of the product has changed from Rev. H (Fab 1) to Rev L (Fab 2). There are significant changes in the design or the manufacturing process.

The new products completed commercial qualification in mid-2004. Full Group C QCI die qualification testing has been completed. Results are presented in the paper.

There are no changes to any electrical or mechanical data sheet specifications. To ensure consistency of product characteristics, Simtek has completed a comparison of the electrical performance between devices manufactured in Fab 1 and Fab 2. This report details the results of this comparison and confirms the consistent characteristics of product built on both Fab lines.

PRODUCT AFFECTED

SMD Part Number	Simtek Part Number
5962-9459903MXC	STK12C68-5C35M
5962-9459902MXC	STK12C68-5C45M
5962-9459901MXC	STK12C68-5C55M
5962-9459903MXA	STK12C68-5K35M
5962-9459902MXA	STK12C68-5K45M
5962-9459901MXA	STK12C68-5K55M
5962-9459903MYA	STK12C68-5L35M
5962-9459902MYA	STK12C68-5L45M

NEW PRODUCT DESIGN REV ID

Products out of Fab 2 will be marked "**Simtek L**" on the first line of the topside mark. The previous revision ID was "Simtek H".

CHANGE DETAIL

- This line move is from Chartered Semiconductor's Fab 1 [CSM1] to Fab 2 [CSM2].
- The Simtek nvSRAM design has been transferred to the new line without change.
- The product is being built to the same 0.8 micron design as in CSM1.
- The CSM2 product meets the current DSCC SMD specifications for the part numbers listed above. Copies of the SMDs may be downloaded from the Simtek website at: http://www.simtek.com/Technology/techn-qualrel.html#simtekproductinfo
- The CSM2 product meets the current datasheet specifications as published on the Simtek website www.Simtek.com.
- No changes are being made in assembly or final test & burn-in.

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Process Characterization Report

Comparison of CSM1 and CSM2 key process parameters affecting device functionality.

Parameter	Unit	% Change	Comments
NLLS Vtlin	Volt	6%	
NLLS Idsat	mA	-3%	
NLLS Bvdss	Volt	3%	
PLLS Vtlin	Volt	4%	
PLLS Idsat	mA	-5%	
PLLS Bvdss	Volt	2%	
NHLS Vtlin	Volt	10%	
NHLS Idsat	mA	-5%	
NHLS Bvdss	Volt	8%	
PHLS Idsat	mA	-3%	
PHLS Bvdss	Volt	4%	
SNOS Ioell Ik	uA	0%	
VMG Positive Vstop	Volt	1%	
VMG Negative Vstop	Volt	1%	
NLV Bkn	Volt	1%	
PLV Bkn	Volt	0%	
NHV Bkn	Volt	3%	
PHV Bkn	Volt	2%	
NLP1 Vtsat	Volt	-7%	
NHP 2 Vtsat	Volt	-6%	
Ndiff	Ohm/Sq	-4%	
Pdiff	Ohm/Sq	-5%	
Npoly1	Ohm/Sq	-3%	
NPoly2	Ohm/Sq	8%	
N Contact	Ohm	4%	
P Contact Ohm/con	Ohm	27%	* Due to use of different/better barrier metal material
M1/M2 Via	Ohm	-8%	
Buried Contact 1 Rcon	Ohm	4%	
Buried Contact 2 Rcon ohm/con	Ohm	2%	

Summary

Absolute wafer level e-parameter values are proprietary to Simtek and the Wafer Foundry.

All values for the CSM2 process correlate well with the original CSM1 process and remain well within the original CSM1 process specification limits.

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QCI Group C Qualification Lifetest Report
Mil-Std-883 M5005
CSM2 0.8µ CMOS/SNOS Process, Simtek 64K 5V nvSRAM

Test	Method	Conditions	Readpoint	Start Qty	# of Failures	Failure Detail
High Temperature Operating Life [HTOL]	Mil-Std-883, M1005	Dynamic, Condition D Full SRAM Array, 140C, Vcc nom	0 hrs	45	0	
			168 hrs	45	0	
			352 hrs	45	0	Zero fails @ 1Khr/125C equivalent
Retention	Mil-Std-883 M1008	Unbiased 150C Store nv array at 0 hr Read stored data.	0 hrs	45	0	
			168 hrs	45	0	
			500 hrs	45	0	
			1000 hrs	45	0	Zero fails @ 1Khr
Endurance	Simtek	Store/Recall cycles of full nv array Functional check at read points	0 cycles	45	0	
			100K cycles	45	0	
			500K cycles	45	0	
			1M cycles	45	0	Zero fails @ 1M cycles
Construction Analysis	Mil-Std-883, M1005					Meets requirements.
Passivation Integrity	Mil-Std-883, M1005					Pass
Device Datasheet Characterization	SMD/Simtek	-55C through +125C				See Table
ESD	JEDEC 22-B A114	Human Body Model		6	0	Pass 1.8KV
Latch-Up Integrity	JEDEC 78	± 100mA, 85C		6	0	Pass ±100mA, 85C

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Product Characterization Report

Comparison of key product datasheet parameters between CSM1 [Fab 1, Rev H] and CSM2 [Fab 2, Rev L] products.

Product Characterization Report [preliminary]
Comparison of key product datasheet parameters between the CSM1 [Fab 1, Rev H] and CSM2 [Fab 2, Rev L] products

Product Tested

- Simtek PN STK12C68-C35M, SMD # 5962-9459903MXC

Test Conditions

- Standard set of all characterization parameters
- 7 temperatures (-55C, -40C, 0C, 25C, 70C, 85C, 125C).
- 5 voltages (4.0V, 4.5V, 5.0V, 5.5V, 6.0V).

Data Analysis
The following table shows the datasheet parameters, specification limits, the CSM2 [Product Revision L margin to specification and the change in margin to spec from CSM1 to CSM2. Where the change in margin to spec column shows a positive number that indicates FAB2 material has more margin than FAB1. Negative numbers in the margin to spec column indicate less margin to spec for FAB2 compared to FAB1. The parameter values are derived from the worst case averages of military temperature (-55C to +125C) and voltage (4.5V to 5.5V) conditions for samples from each fab. All testing was performed at the same time on the same tester, hardware, and program.

Summary
The current production product is now running well within datasheet specifications with adequate margin on all parameters. Value changes between product revision parameters are nominal and should not affect in-system performance.

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SMD 5962-94599 STK12C68 CHARACTERIZATION TABLE

Symbol	#	Parameter	Units	5962-94599 35ns Spec		Fab 2 Mean	Fab 2 Std Dev	Fab 2 Cpk	Fab 1 Mean	Fab 1 Std Dev	Delta Mean Fab 2 to Fab 1	Margin to spec Fab 2	Comment/ Worst Case Condition
				MIN	MAX								
READ CYCLE													
ELQV	1	Chip Enable Access Time	ns		35.0	24.2	0.4	9.0	23.0	0.4	1.2	10.8	125C / 4.5V
AVAV	2	Read Cycle Time	ns	35.0		23.1	0.3	13.2	22.5	0.4	0.6	11.9	125C / 4.5V
AVQV	3	Address Access Time	ns		35.0	25.4	0.5	6.4	24.6	0.5	0.8	9.6	125C / 4.5V
GLQV	4	Output Enable to Data Valid	ns		20.0	4.8	0.4	12.7	5.1	0.3	-0.3	15.2	125C / 4.5V
AXQX	5	Output Hold after Address Change	ns	5.0		12.0	0.3	7.8	11.6	0.4	0.4	7.0	55C / 5.5V
ELQX	6	Chip Enable to Output Active	ns	5.0		13.0	0.3	8.9	12.2	0.5	0.8	8.0	55C / 5.5V
EHQZ	7	Chip Disable to Output Inactive	ns		17.0	5.4	0.3	12.9	5.6	0.4	-0.2	11.6	125C / 4.5V
GLQX	8	Output Enable to Output Active	ns	0.0		3.6	0.2	6.0	3.8	0.3	0.0	3.6	55C / 5.5V
GHQZ	9	Output Disable to Output Inactive	ns		17.0	5.2	0.2	19.7	5.2	0.5	0.0	11.8	125C / 4.5V
ELICCH	10	Chip Enable to Power Active	ns	0.0		N/A	N/A	N/A	N/A	N/A	N/A		not tested
EHICCL	11	Chip Disable to Power Standby	ns		35.0	N/A	N/A	N/A	N/A	N/A	N/A		not tested
WRITE CYCLE #1													
AVAV	12	Write Cycle Time	ns	35.0		24.2	0.4	9.0	22.5	0.4	1.7	10.8	125C / 4.5V
WLWH	13	Write Pulse Width	ns	30.0		13.2	0.8	7.0	12.7	0.8	0.5	16.8	125C / 4.5V
ELWH	14	Chip Enable to End of Write	ns	30.0		11.8	0.4	15.2	11.2	0.4	0.6	18.2	125C / 4.5V
DVWH	15	Data Set-up to End of Write	ns	18.0		8.2	0.3	10.5	7.8	0.3	0.6	9.8	125C / 4.5V
WHDX	16	Data Hold after End of Write	ns	0.0		-2.4	0.3	2.7	-2.2	0.3	-0.2	2.4	125C / 4.5V
AVWH	17	Address Set-up to End of Write	ns	30.0		8.0	0.4	18.3	8.6	0.4	-0.6	22.0	125C / 4.5V
AVWL	18	Address Set-up to Start of Write	ns	0.0		-3.4	0.3	3.8	-3.5	0.2	0.1	3.4	55C / 5.5V
WHAX	19	Address Hold after End of Write	ns	0.0		-1.4	0.3	1.8	-1.8	0.2	0.4	1.4	55C / 5.5V
WLQZ	20	Write Enable to Output Disable	ns		17.0	7.4	0.2	16.0	7.6	0.2	-0.2	9.6	125C / 4.5V
WLQV	21	Output valid after end of Write	ns		35.0	27.2	0.6	4.3	26.1	0.5	1.1	7.8	125C / 4.5V
WHQX	21	Output Active after End of Write	ns	5.0		14.2	0.4	7.7	13.5	0.4	0.7	9.2	55C / 5.5V
WRITE CYCLE #2													
AVAV	12	Write Cycle Time	ns	35.0		24.2	0.4	9.0	22.5	0.4	1.7	10.8	125C / 4.5V
WLEH	13	Write Pulse Width	ns	30.0		12.4	0.5	11.7	11.7	0.5	0.7	17.6	125C / 4.5V
ELEH	14	Chip Enable to End of Write	ns	30.0		12.0	0.3	20.0	11.3	0.3	0.7	18.0	125C / 4.5V
DVEH	15	Data Set-up to End of Write	ns	18.0		8.2	0.3	10.5	7.5	0.3	0.7	9.8	125C / 4.5V
EHDX	16	Data Hold after End of Write	ns	0.0		-2.6	0.2	4.3	-2.2	0.2	-0.4	2.6	55C / 5.5V
AVEH	17	Address Set-up to End of Write	ns	30.0		8.0	0.3	24.4	8.4	0.3	-0.4	22.0	125C / 4.5V
AVEL	18	Address Set-up to Start of Write	ns	0.0		-2.5	0.2	4.2	-2.4	0.2	-0.1	2.5	55C / 5.5V
EHAX	19	Address Hold after End of Write	ns	0.0		-1.8	0.2	3.0	-2.0	0.3	0.2	1.8	55C / 5.5V
HARDWARE STORE / RECALL CYCLE													
Recall	22	Recall Cycle Duration	us		25.0	14.0	0.2	18.4	16.4	0.4	-2.5	11.1	125C / 4.5V

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				5962-94599 35ns Spec								
Store	23	Store Cycle Duration	us		12.0	6.9	0.3	5.7	8.2	0.3	-1.3	5.2	125C / 4.5V
PD Store	24	Power Down Store	us		12.0	6.9	0.3	5.7	8.2	0.3	-1.3	5.2	125C / 4.5V
Delay	25	HSB Low to Inhibit On	us	1.0		4.2	0.5	2.1	3.8	0.5	0.4	3.2	125C / 4.5V
Recover	26	HSB High to Inhibit Off	ns		300.0	118.0	8.0	10.1	128.0	8.0	-10.0	182.0	125C / 4.5V
Assert	27	External Store Pulse Width	ns	250.0		N/A	N/A	N/A	N/A	N/A	N/A		not tested
Vswitch	28	Low Voltage Trigger Level	V	4.0		4.2	0.1	1.3	4.1	0.1	0.1	0.2	-55C
HSB_OL	29	HSB Output Low Current	mA	3.0		2.2	0.2	1.3	2.3	0.2	-0.1	3.0	125C / 5.5V
HSB_OH	30	HSB Output High Current	uA		50.0	10.0	0.1	46.7	11.2	0.1	-1.2	7.0	125C / 5.5V
AVAVN	12	Store/Recall Initiation Cycle	ns	35.0		24.2	0.4	9.0	22.9	0.4	1.7	10.8	125C / 4.5V
AVELN	35	Address Set-Up to Chip Enable	ns	0.0		-2.7	0.2	4.5	-2.3	0.2	-0.4	2.7	-55C / 5.5V
ELEHN	36	Chip enable Pulse Width	ns	25.0		3.2	0.4	18.2	3.2	0.4	0.0	21.8	125C / 4.5V
EHAXN	37	Chip Enable to Address Change	ns	0.0		-1.8	0.2	3.0	-1.6	0.3	-0.2	1.8	-55C / 4.5V
DC CHARACTERISTICS													
ICC1		Ave Vcc Current @ AVAV=45ns	mA		85.0	49.0	0.4	30.0	53.8	1.0	-4.8	36.0	125C / 55V
ICC2		Ave Vcc Current During Store	mA		8.0	3.2	0.2	8.0	3.6	0.3	-0.4	4.8	-55C / 5.5V
ICC3		Ave Vcc Current @200ns, 3.3V, 25C	mA		15.0	10.0	0.2	8.3	10.5	0.3	-0.5	5.0	125C / 55V
ICC4		Ave Vcap Current during Autostore	mA		4.0	1.6	0.2	4.0	1.4	0.2	0.2	2.4	-55C / 5.5V
ICC5		Ave Vcc SB current @AVAV = 45ns	mA		35.0	17.8	0.5	11.5	19.1	0.3	-1.3	17.2	-55C / 5.5V
ICC6		Vcc Standby Current	mA		4.0	2.0	0.1	6.7	2.0	0.2	0.0	2.0	-55C / 5.5V
ILKG		Input Leakage Current	uA	-1.0	1.0	N/A	N/A	N/A	N/A	N/A	N/A		not tested
IOLKG		Off-State Output Leakage Current	uA	-5.0	5.0	N/A	N/A	N/A	N/A	N/A	N/A		not tested
VIH		Input Logic "1" Level	V	2.2		1.9	0.1	2.2	1.7	0.1	0.1	0.3	-55C / 5.5V
VIL		Input Logic "0" Level	V		0.8	1.2	0.1	1.7	1.1	0.1	0.0	0.4	-55C / 5.5V
VOH		Output Logic "1" Voltage	V	2.4		2.8	0.0	3.3	3.8	0.0	-0.8	0.4	125C / 4.5V
VOL		Output Logic "0" Voltage	V		0.4	0.2	0.0	1.3	0.3	0.0	0.0	0.2	125C / 4.5V
Cin		Input Capacitance	pF		8.0	7.5	0.1	1.7	7.5	0.1	0.0	0.5	@ 23C
Cout		Output Capacitance	pF		7.0	6.0	0.1	3.3	6.0	0.1	0.0	1.0	@ 23C

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