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# Cypress Semiconductor Product Qualification Report

QTP# 133705 VERSION \*D  
June, 2015

<b>1Mb and 2Mb F-RAM Memory Product Qualification 130nm Technology, TI Fab</b>	
<b>FM25V20A-G</b>	<b>2Mb (256Kx8bits) Serial F-RAM Memory</b>
<b>FM25V20A-GTR</b>	<b>2Mb (256Kx8bits) Serial F-RAM Memory</b>
<b>FM25V20A-DG</b>	<b>2Mb (256Kx8bits) Serial F-RAM Memory</b>
<b>FM25V20A-DGTR</b>	<b>2Mb (256Kx8bits) Serial F-RAM Memory</b>
<b>FM25V20A-DGQ</b>	<b>2Mb (256Kx8bits) Serial F-RAM Memory with Extended Temperature</b>
<b>FM25V20A-DGQTR</b>	<b>2Mb (256Kx8bits) Serial F-RAM Memory with Extended Temperature</b>
<b>FM25V20A-PG</b>	<b>2Mb (256Kx8bits) Serial F-RAM Memory</b>
<b>FM28V202A-TG</b>	<b>2Mb (128Kx16bits) Parallel F-RAM Memory</b>
<b>FM28V202A-TGTR</b>	<b>2Mb (128Kx16bits) Parallel F-RAM Memory</b>
<b>FM28V102A-TG</b>	<b>1Mb (64Kx16bits) Parallel F-RAM Memory</b>
<b>FM28V102A-TGTR</b>	<b>1Mb (64Kx16bits) Parallel F-RAM Memory</b>

**FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT**  
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**PACKAGE/PRODUCT QUALIFICATION HISTORY**

<b>QTP Number</b>	<b>Description of Qualification Purpose</b>	<b>Date</b>
02-60-5112 / 124901	TI Process Qualification 130nm F-RAM Process	Aug 2008 / Dec 2012
130102	Ramtron Quality Integration - Paper Qualification 1Mb and 2Mb F-RAM Memory	Jan 2013
133705	New Product Qualification, 1Mb and 2Mb F-RAM Memory	Aug 2014

<b>PRODUCT DESCRIPTION (for qualification)</b>	
Qualification Purpose: New Product Qualification, 1Mb and 2Mb F-RAM Memory	
Marketing Part #:	FM25V20A-G, FM25V20A-GTR, FM25V20A-DG, FM25V20A-DGTR, FM25V20A-DGQ, FM25V20A-DGQTR, FM25V20A-PG, FM28V202A-TG, FM28V202A-TGTR, FM28V102A-TG, FM28V102A-TGTR
Device Description:	1Mb and 2Mb F-RAM Serial and Parallel Memory
Cypress Division:	Cypress Semiconductor Corporation – Memory Products Division (MPD)

<b>TECHNOLOGY/FAB PROCESS DESCRIPTION</b>			
Number of Metal Layers:	Proprietary*	Metal Composition:	Proprietary*
Passivation Type and Thickness:	Proprietary*		
Generic Process Technology/Design Rule ( $\mu$ -drawn):	CMOS / 130nm		
Gate Oxide Material/Thickness (MOS):	Proprietary*		
Name/Location of Die Fab (prime) Facility:	Texas Instruments / Dallas		
Die Fab Line ID/Wafer Process ID:	DMOS 5 / E035.1		

\*Texas Instruments' proprietary information is available with signed NDA.

## PACKAGE AVAILABILITY

<b>PACKAGE</b>	<b>ASSEMBLY FACILITY SITE</b>
<b>8-pin SOIC</b>	UTAC, Thailand (UT)
<b>8-pin PDIP</b>	UTAC, Thailand (UT)
<b>8-pin TDFN</b>	UTAC, Thailand (UT)
<b>44-pin TSOPII</b>	ASEK, Taiwan (G)

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	SZ820
Package Outline, Type, or Name:	SOIC 8L (208mils)
Mold Compound Name/Manufacturer:	G600 / Sumitomo
Mold Compound Flammability Rating:	UL 94 V=0 pass
Mold Compound Alpha Emission Rate:	<0.1
Oxygen Rating Index: >28%	53%
Lead Frame Designation:	FMP
Lead Frame Material:	Copper
Substrate Material:	N/A
Lead Finish, Composition / Thickness:	Matte Sn
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Henkel
Die Attach Material:	8200T
Bond Diagram Designation	001-86136
Wire Bond Method:	Thermosonic
Wire Material/Size:	CuPd / 0.8 mil
Thermal Resistance Theta JA °C/W:	118 C/W
Package Cross Section Yes/No:	Yes
Assembly Process Flow:	001-85398M
Name/Location of Assembly (prime) facility:	UTAC, Thailand (UT)
MSL LEVEL	3
REFLOW PROFILE	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	UTAC, Thailand / KYEC, Taiwan

**Note:** Please contact a Cypress Representative for other package availability.

## RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.60V, 125 C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.60V, 125 C JESD22-A108	P
Pressure Cooker Test	JESD22-A102: 121 C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30 C°, 60% RH)	P
Data Retention (Plastic)	150 C, non-biased JESD22-A117 and JESD22-A103	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65 C to 150 C Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30 C°, 60% RH)	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level 3 (192 Hrs, 30 C°, 60% RH)	P
Electrostatic Discharge Human Body Model (ESD-HBM): FM25V20A	(1,100V / 1,500V / 2,200V / 3,300V) JEDEC EIA/JESD22-A114-B	P
Electrostatic Discharge Human Body Model (ESD-HBM): FM28V202A	(1,100V / 1,500V / 2,200V) JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM): FM25V20A	(500V / 750V / 1,000V / 1,250V) JESD22-C101	P
Electrostatic Discharge Charge Device Model (ESD-CDM) : FM28V202A	(500V / 750V / 1,000V / 1,250V) JESD22-C101	P
Static Latch up: FM25V20A	85C, ±140mA, 5.4V JESD78	P
Static Latch up: FM28V202A	85C, ±140mA, 5.4V JESD78	P
Static Latch up: FM25V20A / CY15B102Q	105C, ±140mA, 5.4V JESD78	P

## RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF <sup>3</sup>	Failure Rate
High Temperature Operating Life Early Failure Rate	1784 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life <sup>1,2</sup> Long Term Failure Rate	547,000 DHRs* 231,000 DHRs	0	0.7	55	21 FITs

\*Leverage HTOL data from TI 130nm F-RAM Process QTP#124901 (SPEC#001-85093)

<sup>1</sup> Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

<sup>2</sup> Chi-squared 60% estimations used to calculate the failure rate.

<sup>3</sup> Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[ \frac{E_A}{k} \left[ \frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E<sub>A</sub> = The Activation Energy of the defect mechanism.

K = Boltzmann's constant = 8.62x10<sup>-5</sup> eV/Kelvin.

T<sub>1</sub> is the junction temperature of the device under stress and T<sub>2</sub> is the junction temperature of the device at use conditions.



## Reliability Test Data

QTP #: 133705

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
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**STRESS: ACOUSTIC Microscopy, Before and After MSL3 Preconditioning**

FM25V20A-G	4346426	611343226	UTAC - UT	COMP	15	0	
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**STRESS: HIGH TEMPERATURE OPERATING LIFE- EARLY FAILURE RATE (125C, 96 hours, 3.60V)**

FM25V20A-G	4346426	611343226	UTAC - UT	96	1784	0	
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**STRESS: HIGH TEMPERATURE OPERATING LIFE- LATENT FAILURE RATE (125C, 1,000 hours, 3.60V)**

FM25V20-G	060801410	060801410	UTAC - UT	1000	77	0	
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FM25V20-G	057847882	057847882	UTAC - UT	1000	77	0	
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FM25V20-G	15199101	15199101	UTAC - UT	1000	77	0	
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**STRESS: ESD- CHARGED DEVICE MODEL(500V)**

FM25V20A-G	4346426	611343226	UTAC - UT	COMP	12	0	
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FM28V202-TG	4346426	611343224	UTAC - UT	COMP	12	0	
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**STRESS: ESD- CHARGED DEVICE MODEL(750V)**

FM25V20A-G	4346426	611343226	UTAC - UT	COMP	3	0	
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FM28V202-TG	4346426	611343224	UTAC - UT	COMP	3	0	
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**STRESS: ESD- CHARGED DEVICE MODEL(1,000V)**

FM25V20A-G	4346426	611343226	UTAC - UT	COMP	3	0	
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FM28V202-TG	4346426	611343224	UTAC - UT	COMP	3	0	
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**STRESS: ESD- CHARGED DEVICE MODEL(1,250V)**

FM25V20A-G	4346426	611343226	UTAC - UT	COMP	3	0	
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FM28V202-TG	4346426	611343224	UTAC - UT	COMP	3	0	
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**STRESS: ESD-HUMAN BODY CIRCUIT (1,100V)**

FM25V20A-G	4346426	611343226	UTAC - UT	COMP	3	0	
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FM28V202-TG	4346426	611343224	UTAC - UT	COMP	3	0	
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**STRESS: ESD-HUMAN BODY CIRCUIT (1,500V)**

FM25V20A-G	4346426	611343226	UTAC - UT	COMP	5	0	
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FM28V202-TG	4346426	611343224	UTAC - UT	COMP	5	0	
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## Reliability Test Data

### QTP #: 133705

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: ESD-HUMAN BODY CIRCUIT (2,200V)</b>							
FM25V20A-G	4346426	611343226	UTAC - UT	COMP	8	0	
FM28V202-TG	4346426	611343224	UTAC - UT	COMP	8	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT (3,300V)</b>							
FM25V20A-G	4346426	611343226	UTAC - UT	COMP	3	0	
<b>STRESS: PRESSURE COOKER TEST (121C, 100%RH, with MSL3 Preconditioning)</b>							
FM25V20A-G	4346426	611343226	UTAC - UT	168	80	0	
<b>STRESS: DATA RETENTION TEST (150C, unbiased)</b>							
CY15B102Q-SXE	4351641	611410018	UTAC - UT	500	77	0	
CY15B102Q-SXE	4351641	611410018	UTAC - UT	1000	77	0	
CY15B102Q-SXE	4346426	611410540M	UTAC - UT	500	77	0	
CY15B102Q-SXE	4346426	611410540M	UTAC - UT	1000	77	0	
CY15B102Q-SXE	4407065	611415628M	UTAC - UT	500	77	0	
CY15B102Q-SXE	4407065	611415628M	UTAC - UT	1000	77	0	
CY15B102Q-SXE	4407065	611415628M1	UTAC - UT	500	77	0	
CY15B102Q-SXE	4407065	611415628M1	UTAC - UT	1000	77	0	
CY15B102Q-SXE	4407065	611415628M2	UTAC - UT	500	77	0	
CY15B102Q-SXE	4407065	611415628M2	UTAC - UT	1000	77	0	
<b>STRESS: STATIC LATCH-UP TESTING (85C, ±140mA, 5.4V)</b>							
FM25V20A-G	4346426	611343226	UTAC - UT	COMP	6	0	
FM28V202-TG	4346426	611343224	UTAC - UT	COMP	6	0	
<b>STRESS: STATIC LATCH-UP TESTING (105C, ±140mA, 5.4V)</b>							
CY15B102Q-SXE	4407065	611415628M	UTAC - UT	COMP	6	0	
(FM25V20A)							
<b>STRESS: TEMPERATURE CYCLE, CONDITION C (-65C TO 150C), with MSL3 Preconditioning</b>							
FM25V20A-G	4346426	611343226	UTAC - UT	500	80	0	
FM25V20A-G	4346426	611343226	UTAC - UT	1000	80	0	



## Document History Page

Document Title: QTP #133705:1MB AND 2MB F-RAM MEMORY PRODUCT QUALIFICATION  
Document Number: 001-93908

Rev.	ECN No.	Orig. of Change	Description of Change
**	4481201	BECK	Initial Release
*A	4503661	BECK	Replaced SOIJ with SOIC
*B	4773443	BECK	Added FM25V20A-DGQ and FM25V20A-DGQTR to Page 1 and Page 3. Added reference to QTP #130102 on Page 2. Added 150C DRET to Reliability Stress Test Table on Page 5, and 150C DRET results to Page 8. Removed "HR" from the Duration in Pages 7-8.
*C	4788795	BECK	Added Latch-up Test results at 105C on Page 5 and Page 8.
*D	4801346	BECK	Indicated "Proprietary" Items on the "TECHNOLOGY/FAB PROCESS DESCRIPTION" Table, Page 4.

Distribution: WEB

Posting: None