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Cypress Semiconductor
Product Qualification Report

QTP# 131102 VERSION*A
December, 2014

QTP #131102 Parallel F-RAM Family 64Kb and 256Kb Product Qualification 130nm Technology, TI Fab	
FM18W08-SG	256Kb (32Kb x8bits) Wide Voltage Bytewide F-RAM Memory
FM18W08-SGTR	256Kb (32Kb x8bits) Wide Voltage Bytewide F-RAM Memory
FM18W08-PG	256Kb (32Kb x8bits) Wide Voltage Bytewide F-RAM Memory
FM1808B-SG	256Kb (32Kb x8bits) Bytewide F-RAM Memory
FM1808B-SGTR	256Kb (32Kb x8bits) Bytewide F-RAM Memory
FM1808B-PG	256Kb (32Kb x8bits) Bytewide F-RAM Memory
FM16W08-SG	64Kb (8Kb x8bits) Wide Voltage Bytewide F-RAM Memory
FM16W08-SGTR	64Kb (8Kb x8bits) Wide Voltage Bytewide F-RAM Memory
FM16W08-PG	64Kb (8Kb x8bits) Wide Voltage Bytewide F-RAM Memory
FM1608B-SG	64Kb (8Kb x8bits) Bytewide F-RAM Memory
FM1608B-SGTR	64Kb (8Kb x8bits) Bytewide F-RAM Memory
FM1608B-PG	64Kb (8Kb x8bits) Bytewide F-RAM Memory

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
02-60-5112 / 124901		TI Process Qualification 130nm F-RAM Process	Aug 2008 / Dec 2012
131102		QTP #131102 Parallel F-RAM Family 64Kb and 256Kb Product Qualification	Apr 2014
131102		Ramtron quality integration - paper qual	Apr 2014
131102		Standardize SOIC Package from MSL2 to MSL3	Dec 2014

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	Thermal AF[3]	Total Device Hours * AF	# Fails	Activation Energy	Failure Rate
High Temperature Operating Life Early Failure Rate (ELFR)	2400 Devices	N/A	N/A	0	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate (HTOL)	547,000 DHRs*, 125C 231,000 DHRs, 115C	55 34	38,091,403	0	0.7	24 FITs

*Leverage HTOL data from TI 130nm F-RAM Process QTP#124901 (SPEC#001-85093)

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation
[4] Thermal Total device hours is based on HTOL test and post endurance cycles HTOL test

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Qualification Report

FM18W08-SG, and FM18W08-SGTR, FM18W08-PG, FM1808B-SG, FM1808B-SGTR, FM1808B-PG, FM16W08-SG, FM16W08-SGTR, FM16W08-PG, FM1608B-SG, FM1608B-SGTR, FM1608B-PG

64Kb and 256Kb Parallel F-RAM Memory

Revision: AA & AB

Foundry Supplier: Texas Instruments, Dallas, TX; IBM Burlington, VT

28-lead Green SOIC Package Supplier: UTAC, Bangkok, Thailand
28-lead Green PDIP Package Supplier: Lingsen Precision Technologies, Taichung, Taiwan

Issue Date: April 9, 2014

Originated by:

QA/Reliability

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1 SCOPE

1.1.1 Product Qualification testing was completed on the FM18W08-SG product, a 256Kb Parallel F-RAM Memory with wide voltage operation from 2.7V to 5.5V, from the 130 nm process F-RAM fab family, offered in a UTAC 28-lead Green SOIC package. 28-lead Green PDIP Package Qualification testing was performed on this product family, assembled at Lingsen Precision Technologies, in Taichung, Taiwan.

1.1.2 Product testing is designed to assess compliance to the qualification plan, referencing JESD47H.01 standards. Random samples were chosen from three non-consecutive wafer fab and/or assembly lots for qualification tests as applicable.

1.1.3 These devices are fabricated at Texas Instruments in Dallas, Texas and IBM in Burlington, VT. The 28-lead green SOIC packages are assembled at UTAC in Bangkok, Thailand. Qualification stress/testing was performed at Ramtron International Corporation in Colorado Springs, CO, Integra Technologies in Santa Clara, CA, UTAC in Bangkok, Thailand, Lingsen Precision Technologies in Taichung, Taiwan, and at Innovative Circuits Engineering in San Jose, California.

1.1.4 The following report details the environmental stress tests performed, test sample sizes, accept/reject criteria, test results and conclusion of this qualification.

2 APPLICABLE DOCUMENTS

2.1.1 FM18W08 Datasheet

2.1.2 JESD47H.01 Stress-Test-Driven Qualification of Integrated Circuits

3 RELIABILITY STRESS TESTS

3.1 Pre-conditioning of Samples

3.1.1 Inspection method: JEDEC JESD22 A113

3.1.2 Stress Conditions: 28-lead SOIC: Moisture Sensitivity Level 3 soak conditions (30°C, 60%), Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

3.1.3 Purpose: The purpose of the pre-conditioning of samples prior to HAST, Autoclave and Temperature Cycle is to simulate typical solder reflow operation.

3.1.4 Sample size: 77 units per lot per test

3.1.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure from sample. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification.

3.1.6 Pre-conditioning Test Results:

FM18W08-SG: UTAC 28-lead Green SOIC	Lot# 0U9DBG	Lot# 0SQZBG	Lot# 0RUSBG1	Lot# 801202565
Post Pre-Condition Electrical Test	0 fails/231 parts	0 fails/231 parts	0 fails/77parts	0 fails/154 parts

3.2 Preconditioned Autoclave (AC)

3.2.1 Inspection Method: Preconditioning: JEDEC JESD22 Method A113
Autoclave: JEDEC JESD22 Method A102

3.2.1.1 Stress Conditions: 28-lead SOIC Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60%), Relative Humidity for 192 hrs), three cycles of reflow at 260 °C
Autoclave: 121ºC, 29.7 psia 100% Relative Humidity, 96 hrs

3.2.2 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Unbiased autoclave is performed to evaluate the moisture resistance of non hermetic packages. This is a highly accelerated test which employs conditions of pressure, humidity and temperature to accelerate moisture penetration through external protective materials or along the interface between external protective materials and the metallic conductors passing through it.

3.2.3 Sample Size 77 parts, 1 lot

3.2.4 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification after stress.

3.2.5 Pre-Conditioned Autoclave (AC) Test Results:

FM18W08-SG: UTAC 28-lead Green SOIC	Lot# 0U9DBG	Lot# 0RUSBG1	Lot# 801202565
Post Pre-Conditioned AC Electrical Test	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
FM18W08-PG: Lingsen, 28-lead Green PDIP	Lot# 611326615		
Post Pre-Conditioned AC Electrical Test	0 fails/77 parts		

3.3 Preconditioned Temperature Cycling (TC)

3.3.1 Inspection method: Preconditioning: JEDEC Method A113;
Temperature Cycling: JESD22, Method A104 or AEC-Q100-RevG

3.3.1.1 Stress Conditions: 28-lead SOIC Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60%), Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

Temperature Cycling: -50°C to +125°C, 500 cycles (SOIC followed AEC-Q100-RevG)
-65°C to +150°C, 500 cycles (PDIP followed JEDEC-47, Condition C)

3.3.2 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Temperature cycling stress testing is used to subject devices to severe temperature gradients by cycling the parts into hot and cold air. This test evaluates package strength, bond quality, and assembly process consistency. The test will reveal any thermal expansion mismatches in the die or die/package interfaces.

3.3.3 Sample size: 77 parts per lot.

3.3.4 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification after stress.

3.3.5 Pre-Conditioned TC Test Results:

FM18W08-SG: UTAC 28-lead Green SOIC	Lot# 0U9DBG	Lot# 0SQZBG	Lot# 0RUSBG1
Post Pre-Condition TC Electrical Test	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
FM18W08-PG: Lingsen, 28-lead Green PDIP	Lot# 611326615	Lot# 611326616	Lot# 611326617
Post Pre-Condition TC Electrical Test	0 fails/76 parts	0 fails/77 parts	0 fails/77 parts

3.4 Preconditioned Highly Accelerated Test (HAST)

3.4.1 Inspection Method: Preconditioning: JEDEC JESD22 Method A113
HAST- JEDEC Method A110

3.4.1.1 Stress Conditions: Preconditioning, 28-lead SOIC: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

HAST: 130°C, 85% Relative Humidity, P=33.3psia, biased at maximum operating voltage, 96 hours

3.4.2 Test Description: The purpose of the Preconditioned HAST test is to detect defective packaging materials and processes used for the assembly of these parts. Preconditioning simulates a standard multiple solder reflow operation. HAST conditions accelerate the penetration of moisture through the package molding material and die passivation to the active die surface. Die surface moisture, in turn, can initiate corrosion, ionic migration and other processes resulting in functional or parametric part failure.

3.4.3 Sample Size 77 parts, 1 lot

3.4.4 Accept/Reject Criteria: Accept on 0 failures, reject on 1. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification.

3.4.5 Pre-Conditioned Highly Accelerated Stress Test (HAST) Test Results:

FM18W08-SG: UTAC 28-lead Green SOIC	Lot# 0U9DBG	Lot# ORUSBG1	Lot# 801202565
Post Pre-condition HAST Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Lingsen, 28-lead Green PDIP	Lot# 611326615		
Post Pre-Condition HAST Electrical Test @ 25 °C	0 fails/77 parts		

3.5 Data Retention and High Temperature Storage Life (HTSL)

3.5.1 Inspection method: JESD22, Method A103

3.5.2 Stress Conditions: 125C, 1000 hours

3.5.3 Purpose: The purpose of the high temperature storage life test is determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms, including non volatile memory devices.

3.5.4 Sample size: One Lot of 45 samples

3.5.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure for a sample size of 45 parts from 1 lot. A device is considered to fail if it is unable to retain data or operate within the parameters detailed in the Device Specification. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.5.6 High Temperature Storage Life (HTSL) Test Results:

FM18W08-SG	Lot# 0U9DBG	Lot# 0SQZBG	Lot# ORUSBG1
Data Retention Test (Read 0's and Read 1's) at 25C, 500 hours	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Data Retention Test (Read 0's and Read 1's) at 25C, 1000 hours	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTSL Electrical Test 25°C	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts
Post HTSL Electrical Test 85°C	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts

3.6 High Temperature Operating Life (HTOL)

3.6.1 Inspection method: JESD22, Method A108

3.6.2 Stress Conditions: 115°C, maximum operating voltage, operating 1500 hrs

3.6.3 Purpose: The purpose of the high temperature operating life test is to simulate device operation at elevated temperatures and maximum operating voltages. The data obtained from this test is translated to a lower temperature (55^{o}C) by using the Arrhenius temperature acceleration modeling. The acceleration factor and distribution of failures accumulated is then fit to the appropriate failure distribution equation to statistically predict product end of operating life.

3.6.4 Sample size: Three lots of 77 samples each.

3.6.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification.

3.6.6 HTOL Test Results at 115C for 1,500 hours at 5.5V

FM18W08-SG	Lot # OTTNBG	Lot# 0UWPBG	Lot# L3500G15
Post HTOL Electrical Test	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

3.7 Early Life Failure Rate (ELFR)

3.7.1 Inspection method: JESD22, Method A108

3.7.2 Stress Conditions: 115°C, maximum operating voltage, 168 hours.

3.7.3 Test Description: The units are tested per the High Temp Operating Life requirements of JESD22-A108.

3.7.4 Sample size: 800 per lot

3.7.5 Accept/Reject Criteria: Accept on 0, reject on 1. Failed devices are removed from the test and submitted to Failure Analysis for failure mode identification and corrective action.

3.7.6 Early Life Failure Rate (ELFR) Test Results:

FM28V020-SG	Lot # OTTNBG	Lot# 0UWPBG	Lot# L3500G15
Post ELFR Electrical Test	0 fails/ 800 parts	0 fails/800 parts	0 fails/800 parts

3.8 Wire Bond Shear Test (WBS)

3.8.1 Inspection Method: JEDEC Method 22-B117

3.8.2 Stress Conditions: SOIC: 12grams force minimum. PDIP: 9.1grams force minimum average reading and 4.1 grams force minimum.

3.8.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices. Family data is acceptable for this test.

3.8.4 Sample size required: 30 bonds from a minimum of 5 devices. All bonds were tested on all five parts.

3.8.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.8.6 Wire Bond Shear (WBS) Test Results:

	28-lead SOIC: UTAC FM18W08-SG, Lots L3200G1 and L4900G6	28-lead PDIP: Lingsen FM18W08-PG, Lot 611326615
	0 fails/360 bonds	0 fails/100 bonds
Average	23.35g	17.92g
Ppk	1.68	3.58

3.9 Wire Bond Pull Test (WBP)

3.9.1 Inspection Method: MIL-STD883 Method 2011

3.9.2 Stress Conditions: For gold bond wires <1mil diameter, wipe bond pull is performed with the hook over the ball bond, and not mid-wire method.

3.9.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices.

3.9.4 Sample size: 30 bonds from a minimum of 5 devices

3.9.5 Accept/Reject Criteria: 3 grams force minimum for SOIC and 2 grams force minimum for PDIP. Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.9.6 Wire Bond Pull (WBP) Test Results:

	28-lead SOIC: UTAC FM18W08-SG, Lots L3200G1 and L4900G6	28-lead PDIP: Lingsen FM18W08-PG, Lot 611326615
	0 fails/360 wires	0 fails/100 wires
Average	6.20g	5.5g
Ppk	2.16	2.18

3.10 Solderability (SD)

3.10.1 Inspection method: JEDEC Method B102 or AEC-Q100 Rev G

3.10.2 Stress Conditions: 8 hour steam aging prior to solderability test

3.10.3 Purpose: The purpose of this test is to determine the solderability of device package terminal leads intended to be joined to another surface using solder. Family data is acceptable for this test.

3.10.4 Sample size: 1 lot/15 samples (AEC-Q100 Rev G) or 3 lots /22 leads (JEDEC 47H.01)

3.10.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure.

3.10.6 Solderability (SD) Test Results Family Data from UTAC:

	UTAC Solderability (SOIC)
Sample Size	15 parts
Pass/fail	15 passes/0 fails

3.11 Lead Integrity (LI): 28-lead PDIP

3.11.1 Inspection method: JEDEC Method B105

3.11.2 Stress Conditions: Various tension, bending, lead fatigue, and torque stresses

3.11.3 Purpose: to determine the integrity of the lead/package interface and the lead itself, when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly.

3.11.4 Sample size: 3 lots of 5 pieces each.

3.11.5 Accept/Reject Criteria: Under 10x and 20x magnification, reject if there is evidence of cracking, breakage, loosening, or motion between the lead and device body.

3.11.6 Lead Integrity Test Results:

FM18W08-PG	611326615	611326616	611326617
Sample Size	5 parts	5 parts	5 parts
Pass/fail	5 passes/0 fails	5 passes/0 fails	5 passes/0 fails

3.12 Physical Dimensions (PD)

3.12.1 Inspection method: JEDEC Method B100 and MS-024

3.12.2 Stress Conditions: N/A

3.12.3 Purpose: Package outline and leads measured for concurrence with the Device Specification package drawing. Measurements are made with micrometers to determine adherence to specifications (Jedec MS-024).

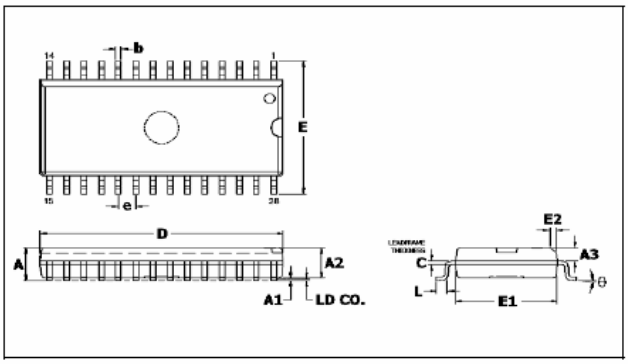
3.12.4 Sample size: 10 units per lot

3.12.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. Cpk > 1.3, ppk > 1.67

3.12.6 Physical Dimension Measurements:

28-lead SOIC:

PRODUCTION PART APPROVAL DIMENSIONAL RESULTS



ORGANIZATION : UTAC Thai Limited
SUPPLIER /VENDOR CODE : UTL
NAME OF INSPECTION FACILITY : UTAC Thai Limited
Part Number # : 28L-SOIC-POD-001
Design Record Change Level : A
Part Name : 28L SOIC Green package
Test date : AUG 28,09
AUG 29,09
AUG 31,09

All dimension are in Inches.

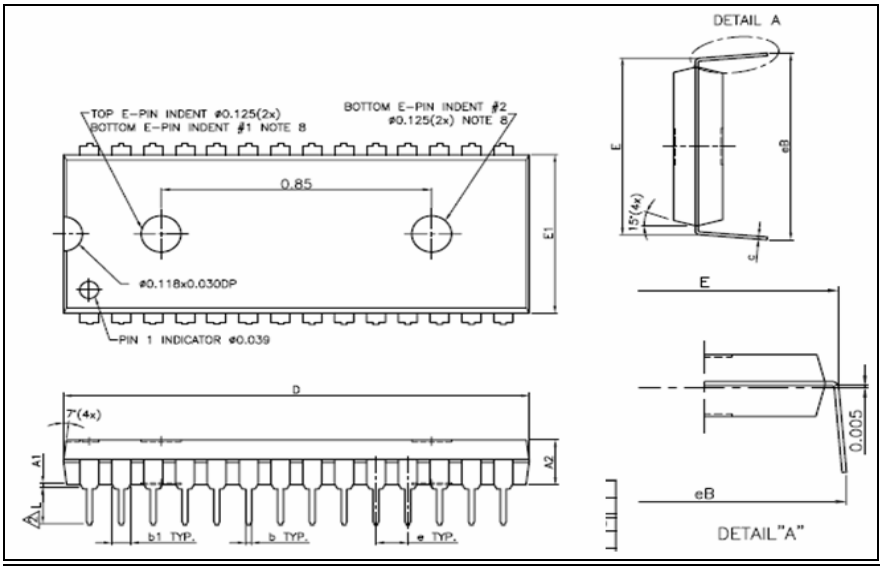
ITEM	Dimension	A	A1	A2	A3	b	C	D	E	E1	E2	e	L PIN 1	L OP. PIN 1	θ PIN 1	θ OP. PIN 1	Ld Co.
Specification	LSL	0.094	0.004	0.088	0.038	0.014	0.009	0.700	0.394	0.291	0.012	0.050	0.024	0.024	0	0	
	USL	0.104	0.012	0.096	0.043	0.018	0.012	0.710	0.419	0.299	0.028	BSC.	0.039	0.039	8	8	0.0039
Lot# 1	1	0.1010	0.0098	0.0917	0.0409	0.0171	0.0113	0.7020	0.4111	0.2967	0.0162	0.0500	0.0379	0.0377	4	4	0.0013
	2	0.1013	0.0097	0.0914	0.0410	0.0176	0.0116	0.7018	0.4117	0.2972	0.0160	0.0500	0.0380	0.0380	4	4	0.0018
	3	0.1011	0.0102	0.0918	0.0415	0.0168	0.0114	0.7016	0.4118	0.2965	0.0165	0.0500	0.0378	0.0374	5	3	0.0017
	4	0.0999	0.0099	0.0914	0.0417	0.0170	0.0115	0.7018	0.4112	0.2964	0.0167	0.0500	0.0377	0.0375	5	5	0.0019
	5	0.1004	0.0101	0.0915	0.0418	0.0172	0.0115	0.7015	0.4113	0.2961	0.0163	0.0500	0.0380	0.0379	4	4	0.0021
	6		0.0104						0.4119								0.0013
	7		0.0095						0.4121								0.0012
	8		0.0098						0.4110								0.0011
	9		0.0095						0.4118								0.0013
	10		0.0091						0.4111								0.0014
	11		0.0098						0.4109								0.0015

ORGANIZATION : UTAC Thai Limited
SUPPLIER /VENDOR CODE : UTL
NAME OF INSPECTION FACILITY : UTAC Thai Limited
Part Number # : 28L-SOIC-POD-001
Design Record Change Level : A
Part Name : 28L SOIC Green package
Test date : AUG 28,09
AUG 29,09
AUG 31,09

All dimension are in Inches.

ITEM	Dimension	A	A1	A2	A3	b	C	D	E	E1	E2	e	L PIN 1	L OP. PIN 1	θ PIN 1	θ OP. PIN 1	Ld Co.
Specification	LSL	0.094	0.004	0.088	0.038	0.014	0.009	0.700	0.394	0.291	0.012	0.050	0.024	0.024	0	0	
	USL	0.104	0.012	0.096	0.043	0.018	0.012	0.710	0.419	0.299	0.028	BSC.	0.039	0.039	8	8	0.0039
Lot# 2	1		0.0100						0.4118								0.0012
	2		0.0098						0.4116								0.0017
	3		0.0096						0.4118								0.0017
	4		0.0087						0.4118								0.0019
	5		0.0090						0.4120								0.0015
	6		0.0097						0.4125								0.0016
	7		0.0101						0.4110								0.0017
	8		0.0098						0.4115								0.0021
	9		0.0101						0.4115								0.0023
	10		0.0094						0.4116								0.0021
	11		0.0094						0.4120								0.0020
Lot# 3	1		0.0102						0.4113								0.0017
	2		0.0097						0.4120								0.0019
	3		0.0095						0.4120								0.0021
	4		0.0089						0.4118								0.0018
	5		0.0090						0.4115								0.0016
	6		0.0100						0.4113								0.0015
	7		0.0101						0.4115								0.0015
	8		0.0100						0.4115								0.0016
	9		0.0096						0.4116								0.0018
	10		0.0098						0.4118								0.0017
	11		0.0102						0.4116								0.0015
	MIN	0.0999	0.0087	0.0914	0.0409	0.0168	0.0113	0.7015	0.4109	0.2961	0.0160	0.0500	0.0377	0.0374	4.00	3.00	0.0011
	MAX	0.1013	0.0104	0.0918	0.0418	0.0176	0.0116	0.7020	0.4125	0.2972	0.0167	0.0500	0.0380	0.0380	5.00	5.00	0.0023
	AVG.	0.1007	0.0097	0.0916	0.0414	0.0171	0.0115	0.7017	0.4116	0.2966	0.0163	0.0500	0.0379	0.0377	4.40	4.00	0.0017
	SD.	0.0006	0.0004	0.0002	0.0004	0.0003	0.0001	0.0002	0.0004	0.0004	0.0003	0.0000	0.0001	0.0003	0.55	0.71	0.0003
	Ppk.	N/A	1.83	N/A	N/A	N/A	N/A	N/A	6.75	N/A	N/A	N/A	N/A	N/A	N/A	N/A	2.48
	WITHIN SPEC.	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	N/A	OK	OK	OK	OK	OK

28-lead PDIP:



LOT# 611326617

Item	spec min	spec max	max read	min read	ave	stdev	cpk
A1	0.38		0.438	0.401	0.417	0.009	
A2	3.71	4.11	3.969	3.941	3.957	0.009	5.67
b	0.36	0.56	0.46	0.441	0.45	0.005	6.00
b1	1.02	1.65	1.49	1.46	1.475	0.009	6.48
c	0.2	0.33	0.28	0.25	0.264	0.01	2.13
D	36.58	37.34	37.294	37.201	37.242	0.03	
E	15.24	15.88	15.619	15.602	15.612	0.005	17.87
E1	13.64	14.15	13.969	13.95	13.958	0.005	12.80
eB	15.88	16.89	16.35	16.251	16.31	0.029	4.94
L	3.18	4.06	3.26	3.223	3.244	0.009	2.37

LOT# 611326616

Item	spec min	spec max	max read	min read	ave	stdev	cpk
A1	0.38		0.436	0.403	0.423	0.01	
A2	3.71	4.11	3.969	3.94	3.956	0.009	5.70
b	0.36	0.56	0.458	0.44	0.45	0.005	6.00
b1	1.02	1.65	1.488	1.46	1.474	0.008	7.33
c	0.2	0.33	0.278	0.25	0.265	0.008	2.71
D	36.58	37.34	37.295	37.209	37.248	0.025	
E	15.24	15.88	15.619	15.6	15.611	0.006	14.94
E1	13.64	14.15	13.968	13.95	13.958	0.006	10.67
eB	15.88	16.89	16.349	16.254	16.306	0.027	5.26
L	3.18	4.06	3.259	3.223	3.24	0.011	1.82

LOT# 611326615

Item	spec min	spec max	max read	min read	ave	stdev	cpk
A1	0.38		0.436	0.4	0.421	0.01	
A2	3.71	4.11	3.968	3.944	3.995	0.007	5.48
b	0.36	0.56	0.459	0.441	0.45	0.005	6.00
b1	1.02	1.65	1.489	1.463	1.477	0.008	7.21
c	0.2	0.33	0.28	0.25	0.264	0.008	2.67
D	36.58	37.34	37.298	37.201	37.249	0.032	
E	15.24	15.88	15.619	15.6	15.61	0.005	18.00
E1	13.64	14.15	13.968	13.95	13.961	0.005	12.60
eB	15.88	16.89	16.347	16.251	16.296	0.028	4.95
L	3.18	4.06	3.259	3.22	3.242	0.012	1.72

3.13 Electrostatic Discharge - Human Body Model (ESD-HBM)

3.13.1 Test Method: JEDEC A114

3.13.2 Stress Conditions: Human Body Model, 100pF discharge through a 1.5K-ohm resistor.

3.13.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Human Body Model as detailed in JEDEC A114-B (100pF discharged through 1.5K ohms). The devices are subjected to voltage ranging from 500V through 4000V for each group of three (3) devices.

3.13.4 Sample size: must pass with at least 3 parts per voltage group tested.

3.13.5 Accept/Reject Criteria: A device passed a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.13.6 FM18W08, FM1608B, FM1808B, and FM16W08 HBM ESD Test Results:

ESD-HBM	FM18W08-SG Lot #00001SG1	FM1608B-PG Lot #00001PG2
500V	0 fails/3	0 fails/3
1000V	0 fails/3	0 fails/3
1500V	0 fails/3	0 fails/3
2000V	0 fails/3	0 fails/3
2500V	0 fails/3	0 fails/3
3000V	0 fails/3	0 fails/3
3500V	0 fails/3	2 fails/3
4000V	0 fails/3	2 fails/3
4500V	1 fail/3	1 fail/3
ESD-HBM	FM1808B-SG Lot #801202565	FM16W08-SG Lot #801202411
1100V	0 fails/3	0 fails/3
2200V	0 fails/8	0 fails/8
3300V	0 fails/3	0 fails/3

Conclusion: FM18W08, FM1608B, FM1808B, and FM16W08 products all pass Human Body ESD immunity >3,000V.

3.14 Electrostatic Discharge – Charged Device Model (CDM)

3.14.1 Test Method: JEDEC22-C101

3.14.2 Stress Conditions: Charged Device Model

3.14.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Charged Device Model as detailed in JEDEC22-C101. The devices are subjected to voltage ranges from 250V to 1250V.

3.14.4 Sample size: must pass with at least 3 parts per voltage group tested.

Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C after ESD stress is applied.

3.14.5 Test Summary: FM18W08, FM1608B, FM1808B, and FM16W08 CDM ESD Results

ESD-CDM	FM18W08 Lot #00001SG1	FM1608B Lot #00001PG2
250V	0 fails/3	0 fails/3
500V	0 fails/3	0 fails/3
750V	0 fails/3	0 fails/3
1000V	0 fails/3	0 fails/3
1250V	0 fails/3	0 fails/3
ESD-CDM	FM1808B-SG Lot #801202565	FM16W08-SG Lot #00001SG
500V	0 fails/9	0 fails/3
1000V	0 fails/3	0 fails/3
1250V	0 fails/3	0 fails/3

3.15 Latch-up Immunity (LU)

3.15.1 Test Method: JEDEC Standard 78

3.15.2 Stress Conditions: Latch-Up: Must pass +/- 100mA current injection, each input pin.
Tested to +/–140mA current injection, each input pin.
Vsupply Over-Voltage Test: 3.65 to 6.4V.

3.15.3 Test Description: The Latch-Up Immunity test assesses the devices susceptibility to latch-up at maximum operating temperatures (85°C). A negative current is applied to each package pin (pin to Vss then pin to Vcc). The current is incremented to +/-200mA, although JEDEC Std 78 only requires –100mA. The device Icc current is measured after each current increment and compared to the maximum value as detailed in the Device Specification. During the Vsupply Over-Voltage Test, the voltage is increased from 3.65 to 6.4V .measuring Icc at each increment after removing the Voltage source.

3.15.4 Sample size: 6 parts from one lot.

3.15.5 Accept/Reject Criteria: Accept on 0 failures and reject on one failure.

3.15.6 FM18W08, FM1608B, FM1808B, and FM16W08 Latch-Up (LU) Test Results:

Part #	Lot Number	Parts Tested	Test Result (85°C)
FM18W08	Lot #00001SG1	6	0 fails up to ±140mA
FM16W08	Lot #00001SG	6	0 fails up to ±140mA
FM1608B	Lot #00001PG2	6	0 fails up to ±140mA
FM1808B	Lot #801202565	6	0 fails up to ±140mA

3.15.7 Conclusion: All devices performed to greater than +/-140mA in Latch up Immunity and passed the Vsupply Over-Voltage Test at 85°C.

4 CONCLUSION

Qualification testing was successfully completed on the FM18W08, FM1608B, FM1808B, and FM16W08 in the 28-lead SOIC package assembled at UTAC, Thailand, and in the 28-lead PDIP package assembled at Lingsen Precision Technologies, Taiwan.

Document History Page

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Rev.	ECN No.	Orig. of Change	Description of Change
**	4338890	BECK	Initial Release
*A	4559940	BECK	Standardized SOIC from MSL2 to MSL3

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