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Cypress Semiconductor
Product Qualification Report
QTP#130804
December 2014

QTP #130804 256Kb Parallel F-RAM Memory Product Qualification 130nm Technology, TI Fab	
FM28V020-SG	256Kb (32Kx8bits) Bytewide F-RAM Memory
FM28V020-SGTR	256Kb (32Kx8bits) Bytewide F-RAM Memory
FM28V020-T28G	256Kb (32Kx8bits) Bytewide F-RAM Memory
FM28V020-T28GTR	256Kb (32Kx8bits) Bytewide F-RAM Memory
FM28V020-TG	256Kb (32Kx8bits) Bytewide F-RAM Memory
FM28V020-TGTR	256Kb (32Kx8bits) Bytewide F-RAM Memory

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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
02-60-5112 / 124901		TI Process Qualification 130nm F-RAM Process	Aug 2008 / Dec 2012
130804		Ramtron quality integration - paper qual	Feb 2013
130401		Reference data from prior ASE TSOP Package Qualification QTP #130401	Feb 2014
130401		Standardize SOIC Package from MSL2 to MSL3	Dec 2014

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate (ELFR)	2400 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate (HTOL)	547,000 DHRs* 231,000 DHRs	0	0.7	55	21 FITs

*Leverage HTOL data from TI 130nm F-RAM Process QTP#124901 (SPEC#001-85093)

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation
[4] Thermal Total device hours is based on HTOL test and post endurance cycles HTOL test

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Qualification Report

FM28V020-SG, FM28V020-SGTR, FM28V020-T28G, FM28V020-T28GTR, FM28V020-TG, FM28V020-TGTR

256Kb Parallel F-RAM Memory

Revision: AD

Foundry Supplier: Texas Instruments, Dallas, TX

28-lead Green SOIC Package Supplier: UTAC, Bangkok, Thailand
32-lead and 28-lead Green TSOP Package Supplier: Advanced Semiconductor Engineering (ASE), Taiwan and Lingsen Precision Technologies, Taiwan

Issue Date: February 14, 2013

Originated by:

QA/Reliability

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1 SCOPE

1.1.1 Product Qualification tests were completed on three non-consecutive wafer lots of FM28V020-SG product, Ramtron's 2.0 to 3.6V, 256Kb Parallel F-RAM Memory, from Ramtron's 130 nm process fab family, offered in a UTAC 28-lead Green SOIC package. Package Qualification testing was completed on three non-consecutive assembly lot splits of the FM28V100-TG product, Ramtron's 2.0 to 3.6V, 1Mb Parallel F-RAM Memory, from Ramtron's 130 nm process fab family in a Lingsen 32-lead Green TSOP package. The 28-lead green TSOP package assembled at Lingsen is qualified by similarity to the larger 32-lead green TSOP package assembled at Lingsen.

1.1.2 The TSOP package at ASE was previously qualified in QTP #130401.

1.1.3 Product testing is designed to assess compliance to Ramtron's qualification plan, referencing JESD47H.01 standards. Random samples were chosen from three non-consecutive wafer fab and/or assembly lots for qualification tests as applicable.

1.1.4 These devices are fabricated at Texas Instruments in Dallas, Texas. The 28-lead green SOIC packages are assembled at UTAC in Bangkok, Thailand. The 32-lead and 28-lead Green TSOP packages are assembled at Lingsen Precision Technologies in Taiwan. Qualification stress/testing was performed at Ramtron International Corporation in Colorado Springs, CO, Integra Technologies in Santa Clara, CA, UTAC in Bangkok, Thailand, Lingsen Precision Technologies in Taichung, Taiwan, and at Innovative Circuits Engineering in San Jose, California.

1.1.5 The following report details the environmental stress tests performed, test sample sizes, accept/reject criteria, test results and conclusions of this qualification. Test and inspection results performed on the selected qualification lots are also summarized in a table at the end of this report.

2 APPLICABLE DOCUMENTS

2.1.1 Ramtron FM28V020 Datasheet Rev 2.1, dated June, 2012

2.1.2 JESD47H.01 Stress-Test-Driven Qualification of Integrated Circuits

2.1.3 Lingsen Assembly data: TS288134—RAM-Q238310.pdf and TS288134—RAM-Q237199.pdf

3 RELIABILITY STRESS TESTS

3.1 Pre-conditioning of Samples

3.1.1 Inspection method: JEDEC JESD22 A113-C

3.1.2 Stress Conditions: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

3.1.3 Purpose: The purpose of the pre-conditioning of samples prior to HAST, Autoclave and Temperature Cycle is to simulate typical solder reflow operation.

3.1.4 Sample size: 77 units per lot per test

3.1.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure from sample. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.1.6 Pre-conditioning Test Results:

FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC	Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
Post Pre-Condition Electrical Test @ 25 °C (prior to HAST/AC)	0 fails/231 parts	0 fails/231 parts	0 fails/231 parts
Post Pre-Condition Electrical Test @ 85 °C (prior to HAST/TC)	0 fails/154 parts	0 fails/154 parts	0 fails/154 parts
FM28V100-TG - Lingsen, 32-lead Green TSOP	Lot # 1700460TG1	Lot # 1700460TG2	Lot # 1700460TG3
Post Pre-Condition Electrical Test @ 25 °C (prior to HAST/TC/AC)	0 fails/231 parts	0 fails/218 parts*	0 fails/231 parts
Post Pre-Condition Electrical Test @ 85 °C (prior to HAST/TC)	0 fails/154 parts	0 fails/141 parts*	0 fails/154 parts
FM22L16-55-TG ASE, 44-lead Green TSOP	Lot # 7630619TG	Lot # 0407488TG1	
Post Pre-Condition Electrical Test @ 25 °C (prior to HAST/TC/AC)	0 fails/160 parts	0 fails/80 parts	
Post Pre-Condition Electrical Test @ 85 °C (prior to HAST/TC)	0 fails/160 parts	0 fails/80 parts	

*13 parts were damaged in handler from FM28V100-TG, 32-lead Green TSOP Lot # 1700460TG2 after stress.

3.1.7 Additional accelerated preconditioning testing was completed on a new sample from 32-lead Green TSOP Lot #1700460TG2 to make up for the 13 pieces that were damaged by the handler. The accelerated preconditioning soak requirements were 40 hours at an accelerated temperature of 60 ºC, at 60% RH, according to JEDEC J-STD-020D.1.

Additional Pre-conditioning Test Results:

FM28V100-TG - Lingsen, 32-lead Green TSOP	Lot # 1700460TG2
Post Pre-Condition Electrical Test @ 25 °C (prior to HAST)	0 fails/77 parts
Post Pre-Condition Electrical Test @ 85 °C (prior to HAST)	0 fails/77 parts

3.2 **Preconditioned Autoclave (AC)**

3.2.1 Inspection Method: Preconditioning: JEDEC JESD22 Method A113-C
Autoclave: JEDEC JESD22 Method A102 Rev. C

3.2.1.1 Stress Conditions: Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

Autoclave: 121ºC, 29.7 psia 100% Relative Humidity, 96 hrs

3.2.2 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Unbiased autoclave is performed to evaluate the moisture resistance of non hermetic packages. This is a highly accelerated test which employs conditions of pressure, humidity and temperature to accelerate moisture penetration through external protective materials or along the interface between external protective materials and the metallic conductors passing through it.

3.2.3 Sample Size 77 parts per lot

3.2.4 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C after stress.

3.2.5 Pre-Conditioned Autoclave (AC) Test Results:

FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC	Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
Post Pre-Conditioned AC Electrical Test @ 25 °C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
FM28V100-TG, Lingsen, 32-lead Green TSOP	Lot # 1700460TG1	Lot # 1700460TG2	Lot # 1700460TG3
Post Pre-Conditioned AC Electrical Test @ 25 °C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
FM22L16-55-TG ASE, 44-lead Green TSOP	Lot# 0407488TG1		
Post Pre-Conditioned AC Electrical Test @ 25 °C	0 fails/77 parts		

3.3 **Preconditioned Temperature Cycling (TC)**

3.3.1 Inspection method: Preconditioning: JEDEC Method A113-C;
Temperature Cycling: JESD22, Method A104, Rev. B

3.3.1.1 Stress Conditions: Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

Temperature Cycling: -50°C to +125°C, 500 cycles

3.3.2 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Temperature cycling stress testing is used to subject devices to severe temperature gradients by cycling the parts into hot and cold air. This test evaluates package strength, bond quality, and assembly process consistency. The test will reveal any thermal expansion mismatches in the die or die/package interfaces. At the conclusion of the temperature cycling test, an electrical functional and parametric test is performed at 85°C.

3.3.3 Sample size: 77 parts per lot.

3.3.4 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C and 85°C after stress.

3.3.5 Pre-Conditioned TC Test Results:

FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC	Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
Post Pre-Condition TC Electrical Test @ 85 °C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
FM28V100-TG, Lingsen, 32-lead Green TSOP	Lot # 1700460TG1	Lot # 1700460TG2	Lot # 1700460TG3
Post Pre-Condition TC Electrical Test @ 85 °C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
FM22L16-55-TG ASE, 44-lead Green TSOP	Lot# 7630619TG		
Post Pre-Conditioned AC Electrical Test @ 25 °C	0 fails/77 parts		

3.4 **Preconditioned Highly Accelerated Test (HAST)**

3.4.1 Inspection Method: Preconditioning: JEDEC JESD22 Method A113-C
HAST- JEDEC Method A110-C

3.4.1.1 Stress Conditions: Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

HAST: 130°C, 85% Relative Humidity, P=33.3psia, biased at 3.6 Vdc, 96 hours

3.4.2 Test Description: The purpose of the Preconditioned HAST test is to detect defective packaging materials and processes used for the assembly of these parts. Preconditioning simulates a standard multiple solder reflow operation. HAST conditions accelerate the penetration of moisture through the package molding material and die passivation to the active die surface. Die surface moisture, in turn, can initiate corrosion, ionic migration and other processes resulting in functional or parametric part failure.

3.4.3 Sample Size 77 parts per lot

3.4.4 Accept/Reject Criteria: Accept on 0 failures, reject on 1. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C.

3.4.5 Pre-Conditioned Highly Accelerated Stress Test (HAST) Test Results:

FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC	Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
Post Pre-condition HAST Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post Pre-condition HAST Electrical Test 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
FM28V100-TG, Lingsen, 32-lead Green TSOP	Lot # 1700460TG1	Lot # 1700460TG2	Lot # 1700460TG3
Post Pre-Condition HAST Electrical Test @ 25 °C	0 fails/77 parts	0 fails/64 parts*	0 fails/77 parts

Post Pre-condition HAST Electrical Test 85°C	0 fails/77 parts	0 fails/64 parts*	0 fails/77 parts
FM22L16-55-TG ASE, 44-lead Green TSOP	Lot# 7630619TG		
Post Pre-Conditioned AC Electrical Test @ 25 °C	0 fails/77 parts		

*13 parts were damaged in handler from FM28V100-TG, 32-lead Green TSOP Lot # 1700460TG2 after stress.

3.4.6 Additional accelerated preconditioning testing was completed on a new sample from 32-lead Green TSOP Lot #1700460TG2 to make up for the 13 pieces that were damaged by the handler. The accelerated preconditioning soak requirements were 40 hours at an accelerated temperature of 60 ºC, at 60% RH, according to JEDEC J-STD-020D.1.

Additional Pre-conditioning Test Results:

FM28V100-TG - Lingsen, 32-lead Green TSOP	Lot # 1700460TG2
Post Pre-Condition HAST Electrical Test @ 25 °C	0 fails/77 parts
Post Pre-condition HAST Electrical Test 85°C	0 fails/77 parts

3.5 **Data Retention and High Temperature Storage Life (HTSL)**

3.5.1 Inspection method: JESD22, Method A103, Rev. B

3.5.2 Stress Conditions: 125C, 1000 hours

3.5.3 Purpose: The purpose of the high temperature storage life test is determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms, including non volatile memory devices.

3.5.4 Sample size: One Lot of 45 samples

3.5.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure for a sample size of 45 parts from 1 lot. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.5.6 High Temperature Storage Life (HTSL) Test Results:

FM28V020-SG	Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
Data Retention Test (Read 0's and Read 1's) at 25C, 1000 hours	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTSL Electrical Test 25°C	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts
Post HTSL Electrical Test 85°C	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts

3.6 High Temperature Operating Life (HTOL)

3.6.1 Inspection method: JESD22, Method A108, Rev. B

3.6.2 Stress Conditions: 125°C, 3.6 Vdc, operating 1000 hrs

3.6.3 Purpose: The purpose of the high temperature operating life test is to simulate device operation at elevated temperatures and higher than nominal operating voltages. The data obtained from this test is translated to a lower temperature (55°C) by using the Arrhenius temperature acceleration modeling. The acceleration factor and distribution of failures accumulated is then fit to the appropriate failure distribution equation to statistically predict product end of operating life.

3.6.4 Sample size: Three lots of 77 samples each.

3.6.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C, 85°C and -40°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode identification and corrective action.

3.6.6 HTOL Test Results:

FM28V020-SG	Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
Post HTOL Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTOL Electrical Test 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTOL Electrical Test -40°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

3.7 Early Life Failure Rate (ELFR)

3.7.1 Inspection method: AEC-Q100-008.

3.7.2 Stress Conditions: 125°C, 3.6Vdc, 48 hours.

3.7.3 Test Description: The units are tested per the High Temp Operating Life requirements of Jedec 22-A108.

3.7.4 Sample size: 800 per lot

3.7.5 Accept/Reject Criteria: Accept on 0, reject on 1. Failed devices are removed from the test and submitted to Failure Analysis for failure mode identification and corrective action.

3.7.6 Early Life Failure Rate (ELFR) Test Results:

FM28V020-SG	Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
Post ELFR Electrical Test 25°C	0 fails/800 parts	0 fails/800 parts	0 fails/800 parts
Post ELFR Electrical Test 85°C	0 fails/800 parts	0 fails/800 parts	0 fails/800 parts

3.8 Wire Bond Shear Test (WBS)

3.8.1 Inspection Method: JEDEC Method 22-B117

3.8.2 Stress Conditions: 5g force minimum for SOIC, and 4.1g force for TSOP

3.8.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices. Family data is acceptable for this test.

3.8.4 Sample size required: 30 bonds from a minimum of 5 devices. All bonds were tested on all five parts.

3.8.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.8.6 Wire Bond Shear (WBS) Test Results:

	UTAC: Minimum Avg Strength Shown, from UTAC SOIC assembly data on four B-Family devices, bonding to the Ramtron 130nm die	Lingsen: Minimum Avg Strength and Ppk, Assembly Qualification Lot # A1607173TG2 (FM28V020-TG device)
	0 fails/30 bonds	0 fails/50 bonds (5pcs)
Average	23.29g	16.38g
Ppk	3.31	5.51

3.9 **Wire Bond Pull Test (WBP)**

3.9.1 Inspection Method: MIL-STD883 Method 2011

3.9.2 Stress Conditions: For gold bond wires <1mil diameter, wipe bond pull is performed with the hook over the ball bond, and not mid-wire method.

3.9.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices.

3.9.4 Sample size: 30 bonds from a minimum of 5 devices

3.9.5 Accept/Reject Criteria: 2 grams force minimum for SOIC and 2 grams force minimum for TSOP. Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.9.6 Wire Bond Pull (WBP) Test Results:

	UTAC: Minimum Avg Strength Shown, from UTAC SOIC assembly data on four B-Family devices, bonding to TI 130nm Die	Lingsen: Minimum Avg Strength and Ppk, Assembly Qualification Lot # A1607173TG2 (FM28V020-TG device)
	0 fails/30 wires	0 fails/50 wires (5pcs)
Average	7.30g	5.07g
Ppk	4.25	1.72

3.10 **Solderability (SD)**

3.10.1 Inspection method: JEDEC Method B102 or AEC-Q100 Rev G

3.10.2 Stress Conditions: 8 hour steam aging prior to solderability test

3.10.3 Purpose: The purpose of this test is to determine the solderability of device package terminal leads intended to be joined to another surface using solder. Family data is acceptable for this test.

3.10.4 Sample size: 1 lot/15 samples (AEC-Q100 Rev G) or 3 lots /22 leads (JEDEC 47H.01)

3.10.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure.

3.10.6 Solderability (SD) Test Results Family Data from UTAC:

	UTAC Solderability on SOIC Leads: Lot #00001G1, FM24W256-G	Lingsen Solderability on TSOP Leads: FM28V020-T28G, Lot A1607173TG, RUN # 237199 and 238310	ASE Solderability on TSOP Leads: FM28V100-TG, Lot 0499856TG2, 0421430TG2, 0527315TG1
Sample Size	15 parts	48 leads	15 parts
Pass/fail	15 passes/0 fails	48 passes/0 fails	15 passes/0 fails

3.11 Electrostatic Discharge - Human Body Model (ESD-HBM)

3.11.1 Test Method: JEDEC A114-B

3.11.2 Stress Conditions: Human Body Model, 100pF discharge through a 1.5K-ohm resistor.

3.11.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Human Body Model as detailed in JEDEC A114-B (100pF discharged through 1.5K ohms). The devices are subjected to voltage ranging from 500V through 4000V for each group of three (3) devices.

3.11.4 Sample size: 3 parts per voltage group tested.

3.11.5 Accept/Reject Criteria: A device passed a voltage level if all devices in the sample group stressed at that voltage and below pass.

NOTE: A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.11.6 FM28V020-SG Rev. AB ESD HBM Test Results:

ESD-HBM	Lot #9702965SG3	
	25°C	85°C
500V	0 fails/3	0 fails/3
1000V	0 fails/3	0 fails/3
1500V	0 fails/3	0 fails/3
2000V	0 fails/3	0 fails/3
2500V	1 fail/3	1 fail/3
3000V	3 fails/3	3 fails/3
3500V	3 fails/3	3 fails/3
4000V	3 fails/3	3 fails/3

3.11.7 The FM28V20 Rev AB passed HBM ESD to 2,000V. This is a Class 2 part by JESD22-A114.

3.12 Electrostatic Discharge – Charged Device Model (CDM)

3.12.1 Test Method: JEDEC22-C101

3.12.2 Stress Conditions: Charged Device Model

3.12.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Charged Device Model as detailed in JEDEC22-C101. The devices are subjected to voltage ranges from 250V to 1250V.

3.12.4 Sample size: 3 parts per voltage group tested.

Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C after ESD stress is applied.

3.12.5 Test Summary: FM28V020-SG Rev. AB ESD – CDM Results

ESD-CDM	Lot #9702965SG3	
	25°C	85°C
250V	0 fails/3	0 fails/3
500V	0 fails/3	0 fails/3
750V	0 fails/3	0 fails/3
1000V	0 fails/3	0 fails/3
1250V	0 fails/3	0 fails/3

3.12.6 Conclusion: The FM28V20 Rev AB devices are categorized as Class 4 for ESD-CDM sensitivity (>1000V) per JESD22-C101.

3.13 Latch-up Immunity (LU)

3.13.1 Test Method: JEDEC Standard 78

3.13.2 Stress Conditions: Latch-Up: Must pass +/- 100mA current injection, each input pin.
Tested to +/–300mA current injection, each input pin.
Vsupply Over-Voltage Test: 3.65 to 6.4V.

3.13.3 Test Description: The Latch-Up Immunity test assesses the devices susceptibility to latch-up at maximum operating temperatures (90°C). A negative current is applied to each package pin (pin to Vss then pin to Vcc). The current is incremented to -300mA, although JEDEC Std 78 only requires –100mA. The device Icc current is measured after each current increment and compared to the maximum value as detailed in the Device Specification. During the Vsupply Over-Voltage Test, the voltage is increased from 3.65 to 6.4V .measuring Icc at each increment after removing the Voltage source.

3.13.4 Sample size: 6 parts from one lot.

3.13.5 Accept/Reject Criteria: Accept on 0 failures and reject on one failure.

3.13.6 FM28V020-SG Rev. AB Latch-Up (LU) Test Results:

Lot Number	Parts Tested	Test Result (85°C)
9702965SG3	6	0 fails up to ±300mA

3.13.7 Conclusion: All devices performed to greater than +/-300mA in Latch up Immunity and passed the Vsupply Over-Voltage Test at 85°C.

4 CONCLUSIONS

Qualification testing was completed, and based on the successful qualification testing; the FM28V020-SG, FM28V020-SGTR, FM28V020-T28G, FM28V020-T28GTR, FM28V020-TG, and FM28V020-TGTR are qualified products.

5 QUALIFICATION SUMMARY TABLE

TEST	ABR	DURATION			
Pre-Conditioning	**PC**	**MSL3**	**FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC**		
			Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
			0 fails/231	0 fails/231	0 fails/231
		MSL3	**FM22L16-55-TG ASE, 44-lead Green TSOP**		
			Lot # 7630619TG	Lot # 0407488TG1	
			0 fails/160	0 fails/80	
		MSL3	**FM28V100-TG - Lingsen, 32-lead Green TSOP**		
			Lot #1700460TG1	Lot #1700460TG2	Lot #1700460TG3
			0 fails/231	0 fails/218 (13 parts damaged in handler)	0 fails/231
				Additional sample: 0 fails/77	
Preconditioned) Autoclave	AC	96-Hr AC/Test Temperature 25C	**FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC**		
			Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
			0 fails/77	0 fails/77	0 fails/77
			FM22L16-55-TG ASE, 44-lead Green TSOP		
			Lot# 0407488TG1		
			0 fails/77		
			FM28V100-TG - Lingsen, 32-lead Green TSOP		
			Lot #1700460TG1	Lot #1700460TG2	Lot #1700460TG3
			0 fails/77	0 fails/77	0 fails/77
(Preconditioned) Temperature Cycle	TC	500 Cycles / Test Temperatures 25C and 85C	**FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC**		
			Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
			0 fails/77	0 fails/77	0 fails/77

			FM22L16-55-TG ASE, 44-lead Green TSOP		
			Lot# 7630619TG		
			0 fails/77 parts		
			FM28V100-TG - Lingsen, 32-lead Green TSOP		
			Lot #1700460TG1	Lot #1700460TG2	Lot #1700460TG3
			0 fails/77	0 fails/77	0 fails/77
(Preconditioned) Highly Accelerated Stress Test	HAST	96-Hr HAST / Test Temperatures 25C and 85C	**FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC**		
			Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
			0 fails/77	0 fails/77	0 fails/77
			FM22L16-55-TG ASE, 44-lead Green TSOP		
			Lot# 7630619TG		
			0 fails/77 parts		
			FM28V100-TG - Lingsen, 32-lead Green TSOP		
			Lot #1700460TG1	Lot #1700460TG2	Lot #1700460TG3
			0 fails/77	0 fails/64 (13 parts damaged in handler) Additional sample: 0 fails/77	0 fails/77
Data Retention and High Temperature Storage Life	EDR/HTSL	125C 1000hrs	**FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC**		
			Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
		Read Zeros	0 fails/77	0 fails/77	0 fails/77
		Read Ones	0 fails/77	0 fails/77	0fails/77
		25°C	0 fails/45	0 fails/45	0 fails/45
		85°C	0 fails/45	0 fails/45	0 fails/45
High Temperature Operating Life	HTOL	125C 1000 hours, 3.6V operating	**FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC**		
			Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG
		25°C	0 fails/77	0 fails/77	0 fails/77
		85°C	0 fails/77	0 fails/77	0 fails/77
		-40°C	0 fails/77	0 fails/77	0 fails/77
Early Life Failure Rate	ELFR	48 hours, 125C, 3.6V operating	**FM28V020-SG, Rev AD UTAC, 28-lead Green SOIC**		
			Lot # 1515052SG1	Lot# 2461754SG	Lot# 2472503SG

		25°C 85°C	0 fails/800 0 fails/800	0 fails/800 0 fails/800	0 fails/800 0 fails/800
Wire Bond Shear Test	WBS			UTAC: Minimum Avg Strength Shown, from UTAC SOIC assembly data on four B-Family devices, bonding to the Ramtron 130nm die	Lingsen: Minimum Avg Strength and Ppk, Assembly Qualification Lot # A1607173TG2 (FM28V020-TG device)
				0 fails/30 bonds	0 fails/50 bonds (5pcs)
			Average	23.29g	16.38g
			Ppk	3.31	5.51
Bond Wire Pull Test	WBP			UTAC: Minimum Avg Strength Shown, from UTAC SOIC assembly data on four B-Family devices, bonding to TI 130nm Die	Lingsen: Minimum Avg Strength and Ppk, Assembly Qualification Lot # A1607173TG2 (FM28V020-TG device)
				0 fails/30 wires	0 fails/50 wires (5pcs)
			Average	7.30g	5.07g
			Ppk	4.25	1.72
Solderability	SD	>95% Lead Coverage	UTAC Solderability on SOIC Leads: Lot #00001G1, FM24W256-G	Lingsen Solderability on TSOP Leads: FM28V020-T28G, Lot A1607173TG, RUN # 237199 and 238310	ASE Solderability on TSOP Leads: FM28V100-TG, Lot 0499856TG2, 0421430TG2, 0527315TG1
		Sample Size	15 parts	48 leads	15 parts
			15 passes/0 fails	48 passes/0 fails	15 passes/0 fails

Electrostatic Discharge- Human Body Model: FM28V020-SG Rev AB Lot #9702965SG3	HBM ESD	500V	0fails/3parts
		1000V	0fails/3parts
		1500V	0fails/3parts
		2000V	0fails/3parts
		2500V	1fail/3parts
		3000V	3fails/3parts
		3500V	3fails/3parts
		4000V	3fails/3parts
		4500V	3fails/3parts
Electro Static Discharge Charged Device Model FM28V020-SG Rev AB Lot #9702965SG3	CDM ESD	250V	0fails/3parts
		500V	0fails/3parts
		750V	0fails/3parts
		1000V	0fails/3parts
		1250V	0fails/3parts
Latch Up Immunity FM28V020-SG Rev AB Lot #9702965SG3	LU	$\pm$ 300 mA	0fails/6parts

Document History Page

Document Title: QTP #130804 256Kb Parallel F-Ram Memory Product Qualification Report
Document Number: 001-86346

Rev.	ECN No.	Orig. of Change	Description of Change
**	3911644	CNOR	Initial spec release.
*A	3954199	BECK	Added Reliability Failure Rate Summary
*B	4275558	BECK	Reference data from prior ASE TSOP Package Qualification QTP #130401
*C	4559895	BECK	Update Page 1 to new template. Standardized SOIC from MSL2 to MSL3

Distribution: WEB

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