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Cypress Semiconductor
Product Qualification Report

QTP#130502
September 2013
Ramtron#: 02-60-5140

QTP #130502 8Mb and 4Mb F-RAM Memory Product Qualification **130nm Technology, TI Fab**	
FM22L16-55-TG	4Mb (256Kx16) F-RAM Memory
FM22L16-55-TGTR	4Mb (256Kx16) F-RAM Memory
FM22LD16-55-BG	4Mb (256Kx16) F-RAM Memory
FM22LD16-55-BGTR	4Mb (256Kx16) F-RAM Memory
FM23MLD16-60-BG	8Mb (512Kx16) F-RAM Memory
FM23MLD16-60-BGTR	8Mb (512Kx16) F-RAM Memory

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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
02-60-5112 / 124901		TI Process Qualification 130nm F-RAM Process	Aug 2008 / Dec 2012
130401		QTP #130401 Documented ASE 44-lead Green TSOP-II Qualification	Jan 2011
02-60-5140		QTP #130502 8Mb and 4Mb F-RAM® Memory Product Qualification	June 2012
130502		Ramtron quality integration - paper qual	Feb 2013

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate (ELFR)	2400 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate (HTOL)	547,000 DHRs* 231,000 DHRs	0	0.7	55	21 FITs

*Leverage HTOL data from TI 130nm F-RAM Process QTP#124901 (SPEC#001-85093)

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation
[4] Thermal Total device hours is based on HTOL test and post endurance cycles HTOL test

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

QUALIFICATION REPORT

(Document #02-60-5140)

FM23MLD16-60-BG and FM22L16-55-TG

8Mb and 4Mb F-RAM Memory

Revision CA

Foundry Supplier: Texas Instruments Inc.

Package Supplier: KY Tech (48-pin BGA); AMKOR Technology Taiwan and ASE Taiwan (44-ld TSOP)

Issue Date: June 27, 2012

Originated by:

QA/Reliability

Distributed to:

Sales & Marketing

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1 SCOPE

1.1.1 Qualification testing was performed on the FM23MLD16-60-BG organized as 512K x 16 bits, F-RAM memory in a 48-pin, “Green”/RoHS BGA package, as well as the FM22L16-55-TG (revision CA) organized as 256K x 16 bits, F-RAM memory in a 44-lead, “Green”/RoHS TSOP-II package.

1.1.2 Product testing is designed to assess overall compliance to the various JEDEC standards. Random samples were chosen from non consecutive FM23MLD16-60-BG and FM22L16C-TG Rev CA manufacturing lots.

1.1.3 These devices were fabricated at Texas Instrument Inc. Dallas, USA. FM23MLD16-60-BG product assembly was performed at KY Technology in Miao-Li, Taiwan. FM22L16-55-TG product assembly was performed at AMKOR Technology in Tao Yuan Hsein,Taiwan and Advanced Semiconductor Engineering, Inc (ASE). Qualification stress/testing was performed at Ramtron International Corporation (RIC), at Innovative Circuits Engineering (ICE) in San Jose, California, at ISE Lab in Fremont, California, at Integra Technologies in Santa Clara, California, at Pikes Peak tech Labs (PPTL) in Colorado Springs, Colorado, and also AMKOR Technology in Tao Yuan Hsein, Taiwan and Advanced Semiconductor Engineering, Inc (ASE).

1.1.4 The following report details the environmental stress tests performed, test sample sizes, accept/reject criteria, test results and conclusions of this qualification. Test and inspection results performed on the selected qualification lots are also summarized in Table I.

Table I: FM23MLD16-60-BG/FM22L16-55-TG Rev. CA Die and Package Qualification Test Summary

* FM22L16-55-TG Qual lots: #8402512(AMKOR), #8432683(AMKOR), #8452803(AMKOR), #7630619TG (ASE), #9667079TG1 (ASE); FM23MLD16-60-BG Qual Lots: 1492363BG3, 1537575BG2, and 1613495BG1

TEST	AEC Q100 Test #	Lots	Fail/ Pass	Conditions
Preconditioning	A1	3 lots each (TSOP BGA)	0/231; 0/102	MSL level 3; bake 24hrs @125°C; soak 30°C /60% RH/192hr; IR-reflow 260°C, 3cycl
(Preconditioned) Highly Accelerated Stress Test	A2	3 lots each (TSOP BGA)	0/77; 0/25	130C, 85% RH, 96 hrs, 33.3psi biased @Vcc max
(Preconditioned) Autoclave	A3	3 lots (TSOP) *Not recommended for BGA.	0/77	121C,100%RH, 29.7psi for 96hrs
(Preconditioned) Temperature Cycle	A4	3 lots each (TSOP BGA)	0/77	Class C: -65C to 150C, 500 cycles
Wire Bond Shear Test	C1	1 lot each (TSOP BGA)	0/5	30 bonds from min 5 devices; Cpk>1.33; Ppk>1.67
Wire Bond Pull Test	C2	1 lot each (TSOP BGA)	0/5	30 bonds from min 5 devices; Cpk>1.33; Ppk>1.67
Solderability	C3	3 lot, 22 leads	0/5	8hrs steam aging; >95% lead coverage
Physical Dimension Averages reported in mils	C4	3 lots (TSOP)	0/30	Cpk>1.33; Ppk>1.67

		*Not required for nonhermetic packages		
Gate Leakage	E8	1 lot (TSOP) *Not required for JEDEC 47H	0/6	+400V, -400V, @155C
High Temperature Storage Life	A5	3 lots	0/77	Included in NVM EDR, B3
High Temperature Operating Life	NA	3 lots	0/316	125C @ 1000hrs, Vcc Max
Early Life Failure Rate	B2	10 lots	0/2400	125C @ 48 hrs (168 hrs)
NVM Endurance Data Retention	B3	3 lots	0/77	Cycling Endurance w/ Focused 5.4E12 cycles; Retention 125C 1000hrs.
Pre & Post Stress Functional/ Parameter	E1	All units	All pass	Functional and Parametric Test at 25C and 85C before and after Stresses.
Electrostatic Discharge-Human Body Model	E2	1 lot	0/15	1.0 1.5 2.0 2.5 KV, 3units/Voltage
Electrostatic Discharge Charged Device Model	E3	1 lot	0/12	250, 500, 750, 800v, 3units/v
Latch Up Immunity	E4	1 lot	0/6	current injection, voltage overstress; sample size = 6units
Electrical Distribution	E5	3 lots	0/30	Data available upon request

2 APPLICABLE DOCUMENTS

Ramtron FM22L16 Datasheet Rev. 1.3 Feb. 2009
Ramtron FM23MLD16 Datasheet Rev.1.3 March, 2012
Stress-Test-Driven Qualification of Integrated Circuits, JESD47H
Process Qualification 130nm F-RAM Process, #02-60-5112

3 RELIABILITY STRESS TESTS

3.1 Preconditioning of Samples

3.1.1 Inspection method: Jedec 22 A113-F

3.1.2 Stress Conditions: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

3.1.3 Purpose: The purpose of the preconditioning of samples prior to HAST, Autoclave (TSOP only), and Temperature Cycle is to simulate typical solder reflow operation.

3.1.4 Sample size: 80 units per lot per tested (total 240 units from each lot on the TSOP and 102 from each lot on the BGA, since Autoclave is not recommended for BGA).

3.1.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure from sample. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC

and DC characteristics at an operating temperature of 25°C and 85 °C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.1.6 FM22L16-55-TG Rev.CA Preconditioning Test Results:

	Lot#8402512TG2	Lot# 8432683TG1	Lot# 8452803TG1	Lot# 7630619TG	Lot# 0407488TG1
Post Precondition Electrical 25 °C	0 fails / 231	0 fails / 231	0 fails / 231	0 fails / 160 parts	0 fails / 80 parts
Post Precondition Electrical 85 °C	0 fails / 231	0 fails / 231	0 fails / 231	0 fails / 160 parts	0 fails / 80 parts

3.1.7 FM23MLD16-60-BG Rev.CA Preconditioning Test Results:

	Lot#1492363BG3	Lot# 1537575BG2	Lot# 1613495BG1
Post Precondition Electrical Test 25 °C	0 fails / 102	0 fails / 102	0 fails / 102
Post Precondition Electrical 85 °C	0 fails / 102	0 fails / 102	0 fails / 102

3.2 Preconditioned Highly Accelerated Stress Test (HAST)

3.2.1 Inspection methods: **Preconditioning**- JEDEC Method A113-F;
HAST- JEDEC Method A110-C

3.2.2 Stress Conditions: **Preconditioning**: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for
192 hrs), three re-flow cycles at 260 °C.
HAST: 130°C, 85% Relative Humidity, P=33.3psia, biased at 3.65 Vdc, 96 hours

3.2.3 Purpose: The purpose of the Preconditioned HAST test is to detect defective packaging materials and processes used for the assembly of these parts. Preconditioning simulates a standard multiple solder reflow operation. HAST conditions accelerate the penetration of moisture through the package molding material and die passivation to the active die surface. Die surface moisture, in turn, can initiate corrosion, ionic migration and other processes resulting in functional or parametric part failure.

3.2.4 Sample size: 77 devices per lot

3.2.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.2.6 FM22L16-55-TG Precondition HAST Test Result

	Lot#8402512TG2	Lot# 8432683TG1	Lot# 8452803TG1	Lot# 7630619TG
Post Precondition HAST Electrical Test 25 °C	0 fails / 77	0 fails / 77	0 fails / 77	0 fails / 77 parts
Post Precondition HAST Electrical Test 85 °C	0 fails / 77	0 fails / 77	0 fails / 77	0 fails / 77 parts

3.2.7 FM23MLD16-60-BG Rev.CA Preconditioned HAST Test Results:

	Lot#1492363BG3	Lot# 1537575BG2	Lot# 1613495BG1
Post Precondition Electrical Test 25 °C	0 fails / 25	0 fails / 25	0 fails / 25
Post Precondition Electrical 85 °C	0 fails / 25	0 fails / 25	0 fails / 25

3.3 Preconditioned Autoclave (AC)

3.3.1 Inspection Method: Preconditioning: JEDEC Method A113-F;
Autoclave JESD 22 Method A102 Rev C

3.3.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 1 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C
Autoclave: 121ºC, 29.7 PSIG 100% Relative Humidity, 96 hrs

3.3.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Unbiased autoclave is performed to evaluate the moisture resistance of non hermetic packages. This is a highly accelerated test which employs conditions of pressure, humidity and temperature to accelerate moisture penetration through external protective materials or along the interface between external protective materials and the metallic conductors passing through it.

3.3.4 Sample Size 77 parts per lot

3.3.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C after stress. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.3.6 FM22L16-55-TG Preconditioned Autoclave (AC) Test Results

	Lot#8402512TG2	Lot# 8432683TG1	Lot# 8452803TG1	Lot# 0407488TG1
Post Precondition Autoclave Electrical Test 25 °C	0 fails / 77	0 fails / 77	0 fails / 77	0 fails / 77 parts

3.4 Preconditioned Temperature Cycling (TC)

3.4.1 Inspection method: Preconditioning: JEDEC Method A113-F;
Temperature Cycling: JESD22, Method A104, Rev. C

3.4.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 1 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C
Temperature Cycling: -65°C to +150°C, 500 cycles (Class C)

3.4.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Temperature Cycle stress testing is used to subject devices to severe temperature gradients by cycling the parts into hot and cold air. This test evaluates package strength, bond quality, and assembly process consistency. The test will reveal any thermal expansion mismatches in the die or die/package interfaces. At the conclusion of the temperature cycling test, an electrical functional and parametric test is performed at 25°C and 85°C. Although it is not required by JEDEC47, 5 units from each TSOP lot were decapped and Wire Pull testing was performed after Temp Cycling. The data is included below.

3.4.4 Sample size: 77 parts per lot.

3.4.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at +25°C and +85°C after stress.

3.4.6 FM22L16-55-TG Preconditioned TC Test Results:

	Lot#8402512TG2	Lot# 8432683TG1	Lot# 8452803TG1	Lot# 7630619TG
Post Precondition Temperature Cycle Electrical Test 25 °C	0 fails / 77	0 fails / 77	0 fails / 77	0 fails / 77 parts
Post Precondition Temperature cycle Electrical Test 85 °C	0 fails / 77	0 fails / 77	0 fails / 77	0 fails / 77 parts

3.4.7 FM23L16-60-BG Preconditioned TC Test Results:

	Lot#1492363BG3	Lot# 1537575BG2	Lot# 1613495BG1
Post Precondition Temperature Cycle Electrical Test 25 °C	0 fails / 77	0 fails / 77	0 fails / 77
Post Precondition Temperature cycle Electrical Test 85 °C	0 fails / 77	0 fails / 77	0 fails / 77

3.5 High Temperature Operating Life (HTOL)

3.5.1 Inspection method: JEDEC Method A108

3.5.2 Stress Conditions: +125°C for 1000hrs, 4.2Vdd, (readpoints at 24, 168, 300, 500, 750 and 1000 hours)

3.5.3 Purpose: The purpose of the high temperature operating life test is to simulate device operation at elevated temperatures and higher than nominal operating voltages. The data obtained from this test is translated to a lower temperature (+55°C) by using the Arrhenius temperature acceleration model. The acceleration factor and distribution of failures accumulated is then fitted into the appropriate failure distribution equation to statistically predict product end of operating life.

3.5.4 Test Description: The HTOL test is conducted under dynamic operating conditions which simulate field operation of the devices. The test conditions of +125°C at 4.2Vdd provide sufficient data to simulate approximately 10 years of operation at an equivalent ambient temperature of +55°C.

3.5.5 Sample size: 77 samples from each of the three lots, 7630619, 7656728 and 7664718, submitted for process qualification.

3.5.6 Accept/Reject Criteria: (Accept on 0 failures for sample size 77 pieces, reject on 1). A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at ambient room temperature. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

4Mb HTOL Results: 125°C @4.2V

	Lot# 7630619TG	Lot# 7656728TG	Lot# 7664718TG
HTOL Electrical Test 25 °C	0 fails / 77	0 fails / 77	0 fails / 77

3.6 Early Life Failure Rate (ELFR)

3.6.1 Inspection method: JEDEC 22-A108A

3.6.2 Stress Conditions: 125°C, 4.2V, 168 hours.

3.6.3 Test Description: The units are tested per the High Temp Operating Life requirements of Jedec 22-A108 C.

3.6.4 Sample size: 2400 units from 10 lots.

3.6.5 Accept/Reject Criteria: Accept on 0, reject on 1.

3.6.6 FM22L16-55-TG Rev CA Early Life Failure Rate (ELFR) Test Results:

Lot #		Post ELFR Electrical Test @ 25°C	Post ELFR Electrical Test @ 85°C
1	#8418791	0 fails/230	0 fails/230
2	#8402512	0 fails/240	0 fails/240
3	#8439158	0 fails/250	0 fails/250
4	#8419208	0 fails/240	0 fails/240
5	#8432683	0 fails/240	0 fails/240
6	#8452803	0 fails/240	0 fails/240
7	#8478399	0 fails/215	0 fails/215
8	#8556953	0 fails/245	0 fails/245
9	#8440557	0 fails/250	0 fails/250
10	#8439157	0 fails/250	0 fails/250
Sum		**0 fails/2400**	**0 fails/2400**

3.7 NVM Endurance, Data Retention and Operational Life (EDR)

3.7.1 Inspection method: JESD 22-A117

3.7.2 Stress Conditions: Preconditioning /Endurance focused 5.4E12 cycles on 128 bits at 3.3V
Data Retention Bake: 125°C, 1000 hrs.

3.7.3 Purpose: Devices are first exercised through the Program/Endurance test followed by Data Retention using the same devices.

3.7.4 Sample size: 77 per lot.

3.7.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C.

3.7.6 FM22L16-55-TG Rev. CA NVM Endurance and Data Retention Test Results

NVM Endurance and Data Retention Test

	Lot#8402512TG2	Lot# 8432683TG1	Lot# 8452803TG1
Endurance Testing per AEC Q100-005 Focused 5.4E 12 Cycles, 3.3V	0 fails / 77	0 fails / 77	0 fails / 77
HTSL Test @ 25 °C, Data Retn for "0", 125°C 1000hrs bake	0 fails / 77	0 fails / 77	0 fails / 77
HTSL Test @ 25 °C, Data Retn for "1", 85°C 30min bake	0 fails / 77	0 fails / 77	0 fails / 77
*Post HTSL Test @ 25 °C	0 fails / 77	0 fails / 77	0 fails / 77
*Post HTSL Test @ 85 °C	0 fails / 77	0 fails / 77	0 fails / 77

** Extended Cycling Endurance Test Results from engineering units up to 5.4E13 are available. Please refer to Appendix at the end of this report.

3.8 Wire Bond Shear Test (WBS)

3.8.1 Inspection Method: JEDS22-B116

3.8.2 Stress Conditions: 7 gf minimum for individual samples, 13 grams on average.

3.8.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices.

3.8.4 Sample size: 30 bonds from a minimum of 5 devices per lot.

3.8.5 Accept/Reject Criteria: Accept the lot on 0 failures.

3.8.6 FM22L16-55-TG Wire Bond Shear (WBS) test Results:

* Sample Size: 30 bonds, Data from AMKOR_BD#ON0003 WB bondability test data.xls.

Lot# 8654958TG1	Max.	Min.	Mean	Stdev	Cpk
Results (g)	18.44	13.04	15.52	1.64	1.74

3.8.7 FM23MLD16-60-BG Wire Bond Shear (WBS) test Results:

* Sample Size: 30 bonds, Data from PPTL "A120771 Ramtron Int.pdf"

Lot# 8654958TG1	Max.	Min.	Mean	Stdev
Results (g)	23	10.0	16.6	2.6

3.9 Wire Bond Pull (WBP)

3.9.1 Inspection Method: Mil Std 883G Method 2011.7

3.9.2 Stress Conditions: Pull to 2.5 gf min.

3.9.3 Purpose: The purpose of this test is to measure tensile bond strength, evaluate strength distributions and determine compliance to the requirements of JEDEC 47.

3.9.4 Sample size: 30 bonds from a minimum of 5 devices per lot.

3.9.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure.

3.9.6 FM22L16-55-TG Wire Bond Pull (WBP) Test Results:

* Sample Size: 30 bonds, Data from AMKOR_BD#ON0003 WB bondability test data.xls.

Lot# 8654958TG1	Max.	Min.	Mean	Stdev	Cpk
Results (g)	9.40	5.81	7.87	0.79	2.26

3.9.7 FM23MLD16-60-BG Wire Bond Pull (WBP) Test Results:

* Sample Size: 30 bonds, Data from PPTL “A120771 Ramtron Int.pdf”

Lot# 8654958TG1	Max.	Min.	Mean	Stdev
Results (g)	6.5	2.0	4.6	1.3

3.10 Solderability (SD) and Solder Ball Shear (SBS)

3.10.1 Inspection method: JEDEC Method B102-E; Jedec Method 22-B117A

3.10.2 Stress Conditions: 8 hour steam aging prior to solderability test.

3.10.3 Purpose: The purpose of solderability test is to determine the solderability of device package terminal leads intended to be joined to another surface using solder. Family data is acceptable for this test. The Solder Ball Shear test specification suggests observations such as statistical outliers in force or failure mode are notable and worthy of attention.

3.10.4 Sample size: Solderability of 3 lots, 22 leads. Solder Ball Shear: 30 balls/5 units. Four devices were tested on 6 points each, and one device was tested for the full 48 locations to provide a more sound statistical basis.

3.10.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. Mean and standard deviation are calculated for the solder ball shear. Using the typical control chart method of establishing limits, upper and lower control limits were set at three standard deviations above and below the mean. No results approached either control limit. Observation of ball shear failure modes found no variation. All balls were sheared in a ductile mode.

3.10.6 FM22L16-55-TG Solderability (SD) Test Results:

	Lot# 8402512TG2	Lot# 8432683TG1	Lot# 8452803TG1	ASE Lot# 0499856TG2	ASE Lot# 0421430TG2	ASE Lot# 0527315TG1
Sample Size	5	5	5	5	5	5
Pass/ Fail	Pass 5/Fail 0	Pass 5/Fail 0	Pass 5/Fail 0	Pass 5/Fail 0	Pass 5/Fail 0	Pass 5/Fail 0

3.10.7 FM23MLD16-60-BG Solder Ball Shear (SBS) Test Results:

Lot# 1492363BG3	Max	Min	Mean	Stdev
Results (g)	548	347	459	50

3.11 Physical Dimensions (PD)

3.11.1 Inspection method: JEDEC Method B100-B* and MS-024
*Not required by JEDEC Standard No. 47H for nonhermetic packages.

3.11.2 Stress Conditions: N/A

3.11.3 Purpose: Package outline and leads measured for concurrence with the Device Specification package drawing. Measurements are made with micrometers to determine adherence to specifications (Jedec MS-024).

3.11.4 Sample size: 10 units per lot

3.11.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. Cpk > 1.3, Ppk > 1.67

3.11.6 FM22L16-55-TG Rev.CA Physical Dimension (PD) Results:

	Lot#8402512TG2	Lot# 8432683TG1	Lot# 8452803TG1	Ppk
Sample Size	10	10	10	
A2 Overall Package Height Lot average Spec: 0.935 -1.05 mm	0.991	0.993	0.986	2.65
b Lead Width Lot average Spec: 0.30-0.45 mm	0.371	0.372	0.369	5.5
D Overall Package Length Lot Average Spec:18.41 min	18.544	18.534	18.528	3.35
E1 Package Width Lot Average Spec: 10.16 min	10.258	10.222	10.271	2.99

3.12 Electrostatic Discharge - Human Body Model (ESD-HBM)

3.12.1 Test Method: JEDEC22-A114

3.12.2 Stress Conditions: Human Body Model, 100pF discharge through a 1.5K-ohm resistor.

3.12.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Human Body Model as detailed in JEDEC A114F (100pF discharged through 1.5K ohms). The devices are subjected to voltage ranging from 500V through 2500V for each group of three (3) devices. ESD testing was done on the FM22L16-55-TG revision CA.

3.12.4 Sample size: 3 parts per voltage group tested.

Accept/Reject Criteria: A device passed a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C after ESD stress is applied.

3.12.5 Human Body Model ESD Results:

ESD-HBM	FM22L16-55-TG Lot #8420512TG2	
	25°C	85°C
500V	0fails/3	0fails/3
1000V	0fails/3	0fails/3
1500V	0fails/3	0fails/3
2000V	0fails/3	0fails/3
2500V	0fails/3	0fails/3

ESD-HBM	FM23MLD16-60-BG Lot #9681818BG1	
	25°C	85°C
1000V	0fails/3	0fails/3
1500V	0fails/3	0fails/3
2000V	2fails/3	2fails/3
2500V	2fails/3	2fails/3

3.12.6 Conclusion: The FM22L16 device is categorized as Class H2 device for, HBM ESD sensitivity > 2000V to <= 4000V, per JEDEC22-A114. The FM22L16-60-BG is classified as a Class H1C device, HBM ESD sensitivity > 1000V to <= 2000V, per JEDEC22-A114

3.13 Electrostatic Discharge – Charged Device Model (CDM)

3.13.1 Test Method: JEDEC 22-C101D

3.13.2 Stress Conditions: Charged Device Model

3.13.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Charged Device Model as detailed in JEDEC 22-C101D . The devices are subjected to voltage ranges from 250V to 800V. ESD testing was done on the FM22L16-55-TG revision CA.

3.13.4 Sample size: 3 parts per voltage group tested.

Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C after ESD stress is applied.

3.13.5 CDM ESD Test Results:

ESD-CDM	FM22L16-55-TG Lot #8420512TG2	
	25°C	85°C
250V	0fails/3	0fails/3
500V	0fails/3	0fails/3
750V	0fails/3	0fails/3
800V	0fails/3	0fails/3

ESD-CDM	FM23ML16-60-TG Lot #9681818BG1	
	25°C	85°C
250V	0fails/3	0fails/3
500V	0fails/3	0fails/3
750V	0fails/3	0fails/3
800V	0fails/3	0fails/3

3.13.6 Conclusion: The FM22L16 device is categorized as Class C3B product for ESD-CDM sensitivity (>500V to <= 750V with corner pin >750V) per JEDEC 22-C101D. The FM22L16-60-BG device is categorized as a Class 4 product for ESD-CDM sensitivity (>1000V) per JEDEC 22-C101D.

3.14 Latch-up Immunity (LU)

3.14.1 Test Method: JEDS Std78

3.14.2 Stress Conditions: Programmed Vdd: 3.65 V
Vdd Current Clamp: 100mA; 50mA
Test Temperature: 85°C
Trigger Source: +/- 50mA to +/-100mA, by +/-25mA step.
Tested to +/–100mA current injection, each input pin.

3.14.3 Test Description: The Latch-Up Immunity test assesses the devices susceptibility to latch up. A negative current is applied to each package pin (pin to Vss, then pin to Vcc). The current is incremented from 50mA to +/-100mA in increments of 25mA per the JEDS 78B requirements. The device Icc current is measured after each current increment and compared to the maximum value as detailed in the Device Specification. During the Vsupply Over-Voltage Test, the voltage is increased from 3.6V to 5.475V measuring Icc at each increment after removing the Voltage source.

3.14.4 Sample size: 6 parts from one lot.

Accept/Reject Criteria: Accept on 0 failures and reject on one failure. Idd fail limit is defined by I(nom) times 1.4 or I (nom) + 10mA, whichever is greater. A device is also considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C after Latch-up stress is applied.

3.14.5 FM22L16-55-TG Rev.CA Latch-Up Test Results:

Lot Number	Parts Tested	Test Result	Remark
Lot #8420512TG2	6	0 fails/6	passed up to ±100mA

3.14.6 FM22L16-60-BG Rev.CA Latch-Up Test Results:

Lot Number	Parts Tested	Test Result	Remark
Lot #9681818BG1	6	0 fails/6	passed up to ±50mA

3.14.7 Conclusion: The FM22L16 device performed to ±100mA in Latch up Immunity and passed the Vsupply Over-Voltage Test to 5.475V. The FM22L16-60-BG device performed to ±50mA in Latch up Immunity and passed the Vsupply Over-Voltage Test to 5.475V.

3.15 Electrically Induced Gate Leakage (GL) AEC Q100 Test# E8

3.15.1 Inspection method: AEC Q100-006 Rev. D

3.15.2 Stress Conditions: ± 400V at 155°C

3.15.3 Test Description: Trapped-charge phenomenon occurs to plastic encapsulated integrated circuits at high temperature when an electric field is present. This test is used to determine surface mount integrated circuit susceptibility to Electro-Thermally induced Parasitic Gate Leakage (GL). Apply electric field (+/-400V/2~3inches) over the sample units at 155°C for the time specified per AEC-Q100-006 and verify parametric and functionality of the devices at 25°C to determine pass or fail. Subject all failing devices to an unbiased bake of 4 hours at 125°C and then submit for complete parametric and functional testing. If the failing devices do not recover following the unbiased bake, then the devices may have been damaged due to handling, ESD, etc. GL testing was done on the FM22L16-55-TG revision CA.

3.15.4 Sample size: 6 units from one lot.

Accept/Reject Criteria: Accept 0, Reject on 1. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C after parasitic gate leakage test.

3.15.5 FM22L16-55-TG Rev.CA Gate Leakage (GL) Test Results:

Lot Number	Parts Tested	400V	Test Results
Lot #8420512TG2	3	+	0 fails/ 3
	3	-	0 fails/ 3

4 FAILURE ANALYSIS

No failing tests were reported. No failure analysis performed.

5 CORRECTIVE ACTION

No Corrective Action required to be implemented.

6 CONCLUSIONS

Based on the completion of the F-RAM product qualification testing, the FM23MLD16-60-BG and FM22L16-55-TG revision CA are qualified to JEDEC standards and the qualification report is issued.

Appendix

Table II: Extended Cycling Endurance Test

Table II shows cycling endurance test results from engineering units, FM22L16-55-TG Rev AE, Lot# 6104423. Endurance cycling up to $5.4x10^{13}$ has been completed on 128 bits (64 2T2C pairs).

Table II. 4Mb Cycling Endurance Results baked at 125°C

No. of Units	Test Mode	No. of Cycles	No. of Bits/Row	No. of Rows	% Failing Test
40	Intrinsic	$2.7x10^{9}$	128	1	0
		$2.7x10^{10}$	128	1	
		$2.7x10^{11}$	128	1	
		$2.7x10^{12}$	128	1	
		$2.7x10^{13}$	128	1	
37	Intrinsic	$5.4x10^{9}$	128	1	0
		$5.4x10^{10}$	128	1	
		$5.4x10^{11}$	128	1	
		$5.4x10^{12}$	128	1	
		$5.4x10^{13}$	128	1	

Document History Page

Document Title: QTP # 130502 8MB AND 4MB F-RAM MEMORY PRODUCT QUALIFICATION
Document Number: 001-85943

Rev.	ECN No.	Orig. of Change	Description of Change
**	3895190	CNOR	Initial spec release.
*A	3954141	BECK	Added Reliability Failure Rate Summary
*B	4133992	BECK	Added ASE TSOP data from QTP #130401

Distribution: WEB

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