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Cypress Semiconductor
Product Qualification Report

QTP#130401
January 2013
Ramtron#: 02-60-5126

QTP #130401 1Mb F-RAM Memory Qualification 130nm Technology, TI Fab	
FM28V100-TG	1Mb (128Kx8bits) 1Mbit Bytewide F-RAM Memory
FM28V100-TGTR	1Mb (128Kx8bits) 1Mbit Bytewide F-RAM Memory

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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
02-60-5112 / 124901		TI Process Qualification 130nm F-RAM Process	Aug 2008 / Dec 2012
02-60-5126		QTP #130401 1Mb F-RAM Memory Qualification	Dec 2010
130401		Ramtron quality integration - paper qual	Jan 2013

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate (ELFR)	2400 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate (HTOL)	547,000 DHRs* 231,000 DHRs	0	0.7	55	21 FITs

*Leverage HTOL data from TI 130nm F-RAM Process QTP#124901 (SPEC#001-85093)

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation
[4] Thermal Total device hours is based on HTOL test and post endurance cycles HTOL test

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

QUALIFICATION REPORT

(Document #02-60-5126)

FM28V100-TG

1Mb F-RAM Memory

Revision AB

Foundry Supplier: Texas Instruments Inc.

Package Supplier: AMKOR Technology Taiwan and ASE Taiwan

Issue Date:

Original Issue Date: December 6, 2010

1st revision: January 11, 2011

Originated by:

QA/Reliability

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1 SCOPE

1.1 Preliminary qualification testing was performed on the FM28V100-TG (revision AB) organized as 128K x 8 bits, F-RAM memory in a 32-lead, “Green”/RoHS TSOP-I package.

1.2 Product testing is designed to assess overall compliance to the various JEDEC standards. Generic family data has been supplied for all testing except as stated in AEC Q100, Rev. G Table 1: Part Qualification/Requalification Lot Requirements. Package test data was provided by AMKOR Technology and Advanced Semiconductor Engineering, Inc (ASE).

1.3 These devices were fabricated at Texas Instrument Inc. Dallas, USA. Product assembly was performed at AMKOR Technology in Tao Yuan Hsein, Taiwan and at Advanced Semiconductor Engineering, Inc. in Kaohsiung, Taiwan. Qualification stress/testing was performed at Ramtron International Corporation (RIC), at Innovative Circuits Engineering (ICE) in San Jose, California, at ISE Lab in Fremont, California, at Integra Technologies in Santa Clara, California, at Pikes Peak tech Labs (PPTL) in Colorado Springs, Colorado, AMKOR Technology in Tao Yuan Hsein, Taiwan, and at Advanced Semiconductor Engineering, Inc. in Kaohsiung, Taiwan.

1.4 The following report details the environmental stress tests performed, test sample sizes, accept/reject criteria, test results and conclusions of this qualification. Test and inspection results performed on the selected qualification lots are also summarized in Table I.

Table I: FM28V100-TG Rev. AB Qualification Test Summary

* Qual lots: # 0499856TG2, #0421430TG2, #0527315TG1, #8536300TG2 (FM28V100-TG)
* Qual lots: #8536300, #8673581, #8709155 (FM25V10-G)
* Qual lots: #8402512, #8432683, #8452803, #7630619TG, #9667079TG1. (FM22L16-TG)

TEST	AEC Q100 Test #	Minimum Lots	Fail/ Pass Per Lot	Conditions	Locations
Preconditioning	A1	3 lots	0/240	MSL level 3; bake 24hrs @125°C; soak 30°C /60% RH/192hr; IR-reflow 260°C, 3cycl	ICE/ISE
(Preconditioned) Highly Accelerated Stress Test	A2	3 lots	0/77	130C, 85% RH, 96 hrs, 33.3psi biased @Vcc max	ISE
(Preconditioned) Autoclave	A3	3 lots	0/77	121C,100%RH, 29.7psi for 96hrs	ICE
(Preconditioned) Temperature Cycle	A4	3 lots	0/77	Class C: -65C to 150C, 500 cycles	ICE
Wire Bond Shear Test	C1	1 lot	0/5	30 bonds from min 5 devices; Cpk>1.33; Ppk>1.67	AMKOR
Wire Bond Pull Test	C2	1 lot	0/5	30 bonds from min 5 devices; Cpk>1.33; Ppk>1.67	AMKOR
Solderbility	C3	3 lot	0/5	8hrs steam aging. >95% lead coverage	PPTL
Physical Dimension Averages reported in mils	C4	3 lots	0/30	Cpk>1.33; Ppk>1.67	RIC
Gate Leakage	E8	1 lot	0/6	+400V, -400V, @155C	PPTL
High Temperature Storage Life	A5	3 lots	0/77	Included in NVM EDR, B3	TI/RIC
High Temperature Operating Life	NA	3 lots	0/316	125C @ 1000hrs, Vcc Max	TI/ RIC
Early Life Failure Rate	B2	10 lots	0/2400	125C @ 48 hrs (168 hrs)	TI/ RIC
NVM Endurance Data Retention	B3	3 lots	0/77	Cycling Endurance w/ Focused 5.4E12 cycles; Retention 125C 1000hrs.	TI/ RIC
Pre & Post Stress Functional/ Parameter	E1	All units	All pass	Functional and Parametric Test at 25C and 90C before and after Stresses.	RIC
Electrostatic Discharge-Human Body Model	E2	1 lot	0/15	0.5 1.0 1.5 2.0 2.5 kv, 3units/v	ISE
Electrostatic Discharge Charged Device Model	E3	1 lot	0/12	250, 500, 750, 800v, 3units/v	ISE
Latch Up Immunity	E4	1 lot	0/6	injection, voltage overstress; ss = 6units	ISE
Electrical Distribution	E5	3 lots	0/30	Data available upon request	RIC

2 APPLICABLE DOCUMENTS

2.1 Ramtron V100 Datasheet. Rev. 1.1 Mar. 2009

2.2 Stress-Test-Driven Qualification of Integrated Circuits, JESD47F

2.3 AMKOR_BD#ON0003 WB bondability test data.

2.4 AMKOR Ramtron-TSOP44 Engineering Report, #02-02-6755

3 RELIABILITY STRESS TESTS

3.1 Preconditioning of Samples

3.1.1 Inspection method: Jedec 22 A113-F

3.1.2 Stress Conditions: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs),
three cycles of reflow at 260 °C

3.1.3 Purpose: The purpose of the preconditioning of samples prior to HAST, Autoclave and Temperature Cycle is to simulate typical solder reflow operation.

3.1.4 Sample size: 80 units per lot per test (total 240 units from each lot)

3.1.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure from sample. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85 °C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.1.6 FM22L16-TG Rev.CA Preconditioning Test Results:

	Amkor Lot#8402512TG2	Amkor Lot# 8432683TG1	Amkor Lot# 8452803TG1	ASE Lot# 7630619TG	ASE Lot# 0407488TG1
Post Precondition Electrical Test 25 °C	0 fails / 240 parts	0 fails / 240 parts	0 fails / 239* parts	0 fails / 160 parts	0 fails / 80 parts
Post Precondition Electrical 90 °C	0 fails / 240 parts	0 fails / 240 parts	0 fails / 239 parts	0 fails / 160 parts	0 fails / 80 parts

* One unit lost due to hander malfunction.

3.2 Highly Accelerated Stress Test (HAST)

3.2.1 Inspection methods: Preconditioning- JEDEC Method A113-F;
HAST- JEDEC Method A110-C

3.2.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for
192 hrs), three re-flow cycles at 260 °C.
HAST: 130°C, 85% Relative Humidity, P=33.3psia, biased at 3.65 vdc, 96 hours

3.2.3 Purpose: The purpose of the Preconditioned HAST test is to detect defective packaging materials and processes used for the assembly of these parts. Preconditioning simulates a standard multiple solder reflow operation. HAST conditions accelerate the penetration of moisture through the package molding material and die passivation to the active die surface. Die surface moisture, in turn, can initiate corrosion, ionic migration and other processes resulting in functional or parametric part failure.

3.2.4 Sample size: 77 devices per lot

3.2.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 90°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.2.6 FM FM22L16-TG Precondition HAST Test Result

	Amkor Lot#8402512TG2	Amkor Lot# 8432683TG1	Amkor Lot# 8452803TG1	ASE Lot# 7630619TG
Post Precondition HAST Electrical Test 25 °C	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts
Post Precondition HAST Electrical Test 90 °C	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts

3.3 Preconditioned Autoclave (AC)

3.3.1 Inspection Method: Preconditioning: JEDEC Method A113-F;
Autoclave JESD 22 Method A102 Rev C

3.3.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 1 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C
Autoclave: 121ºC, 29.7 PSIG 100% Relative Humidity, 96 hrs

3.3.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Unbiased autoclave is performed to evaluate the moisture resistance of non hermetic packages. This is a highly accelerated test which employs conditions of pressure, humidity and temperature to accelerate moisture penetration through external protective materials or along the interface between external protective materials and the metallic conductors passing through it.

3.3.4 Sample Size 77 parts per lot

3.3.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at +25°C after stress. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.3.6 FM22L16-TG Preconditioned Autoclave (AC) Test Results

	Amkor Lot#8402512TG2	Amkor Lot# 8432683TG1	Amkor Lot# 8452803TG1	ASE Lot# 0407488TG1
Post Precondition Autoclave Electrical Test 25 °C	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts

3.4 Preconditioned Temperature Cycling (TC)

3.4.1 Inspection method: Preconditioning: JEDEC Method A113-F;
Temperature Cycling: JESD22, Method A104, Rev. C

3.4.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 1 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C
Temperature Cycling: -65°C to +150°C, 500 cycles (Class C)

3.4.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Temperature Cycling stress testing is used to subject devices to severe temperature gradients by cycling the parts into hot and cold air. This test evaluates package strength, bond quality, and assembly process consistency. The test will reveal any thermal expansion mismatches in the die or die/package interfaces. At the conclusion of the temperature cycling test, an electrical functional and parametric test is performed at 25°C and 90°C. The 5 units from each lot are decapped and Wire Pull testing performed.

3.4.4 Sample size: 77 parts per lot.

3.4.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at +25°C and +90°C after stress.

3.4.6 FM22L16-TG Preconditioned TC Test Results:

	Amkor Lot#8402512TG2	Amkor Lot# 8432683TG1	Amkor Lot# 8452803TG1	ASE Lot# 7630619TG
Post Precondition Temperature Cycle Electrical Test 25 °C	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts
Post Precondition Temperature cycle Electrical Test 90 °C	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts	0 fails / 77 parts
Wire Bond Pull Test Min 2.1 grams minimum	0 fails Min. 4.0	0 fails Min. 4.8	0 fails Min. 4.5	

3.5 High Temperature Operating Life (HTOL), AEC-Q100 Test #B1

3.5.1 Inspection method: JESD22, Method A108, Rev. B

3.5.2 Stress Conditions: 125°C, 3.65 Vdc, operating 1000 hrs

3.5.3 Purpose: The purpose of the high temperature operating life test is to simulate device operation at elevated temperatures and higher than nominal operating voltages. The data obtained from this test is translated to a lower temperature (55°C) by using the Arhennius temperature acceleration modeling. The acceleration factor and distribution of failures accumulated is then fit to the appropriate failure distribution equation to statistically predict product end of operating life.

3.5.4 Sample size: Three lots of 77 samples each.

3.5.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality

and AC and DC characteristics at an operating temperature of 25°C, 90°C and -45°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.5.6 FM 25V10-G Rev. AB HTOL Test Results:

FM25V10-G Lots	Lot# 8536300	Lot# 8673581	Lot# 8709155
Post HTOL Electrical Test 25 °C	0 fails / 77	0 fails / 77	0 fails / 77
Post HTOL Electrical Test 90 °C	0 fails / 77	0 fails / 77	0 fails / 77
Post HTOL Electrical Test -45 °C	0 fails / 77	0 fails / 77	0 fails / 77

3.6 Early Life Failure Rate (ELFR), AEC-Q100 Test #B2

3.6.1 Inspection method: AEC-Q100-008.

3.6.2 Stress Conditions: 125°C, 3.65Vdc, 48 hours.

3.6.3 Test Description: The units are tested per the High Temp Operating Life requirements of Jedec 22-A108.

3.6.4 Sample size: 800 per lot

3.6.5 Accept/Reject Criteria: Accept on 0 fails, reject on 1 fail.

3.6.6 FM25V10-G Rev AB Early Life Failure Rate (ELFR) Test Results:

FM25V10-G Lots	Lot# 8536300	Lot# 8673581	Lot# 8709155
Post ELFR Electrical Test 25 °C	0 fails /800	0 fails /800	0 fails /800
Post ELFR Electrical Test 90 °C	0 fails/800	0 fails/800	0 fails/800

3.7 NVM Endurance, Data Retention and Operational Life (EDR), AEC-Q100 Test #B3

3.7.1 Inspection method: AEC-Q100-005

3.7.2 Stress Conditions: Program/Endurance: 1 E5 Cycles at 3.65V
HTOL: 125 °C, 1000 hrs.

3.7.3 Purpose: Devices are first exercised through the Program/Endurance test, then HTOL.

3.7.4 Sample size: 77 per lot.

3.7.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 90°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.7.6 FM25V10-G Rev. AB NVM Endurance (EDR) Test Results:

NVM Endurance and HTSL

FM25V10-G Lot #	Lot# 8536300	Lot# 8673581	Lot# 8709155
Endurance Testing per AEC Q100-005 1E 5 Cycles, 3.65V	0 fails / 77	0 fails / 77	0 fails / 77
Read Zeros	0 fails / 77	0 fails / 77	0 fails / 77
Read Ones	0 fails / 77	0 fails / 77	0 fails / 77
Post RET Electrical Test 25 °C	0 fails / 77	0 fails / 77	0 fails / 77
Post RET Electrical Test 90 °C	0 fails / 77	0 fails / 77	0 fails / 77

3.8 Wire Bond Shear Test (WBS), AEC Q100 Test#C1

3.8.1 Inspection Method: AEC Q100-001 Rev. C

3.8.2 Stress Conditions: 7 gf minimum for individual samples.

3.8.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices.

3.8.4 Sample size: 30 bonds from a minimum of 5 devices per lot.

3.8.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33. Ppk>1.67

3.8.6 FM22L16-TG Wire Bond Shear (WBS) test Results:

* Sample Size: 30 bonds, Data from AMKOR_BD#ON0003 WB bondability test data.xls.

Lot# 8654958TG1	Max.	Min.	Mean	Stdev	Cpk
Results (g)	18.44	13.04	15.52	1.64	1.74

3.9 Wire Bond Pull (WBP), AEC Q100 Test# C2

3.9.1 Inspection Method: Mil Std 883G Method 2011.7

3.9.2 Stress Conditions: Pull to 2.5 gf min.

3.9.3 Purpose: The purpose of this test is to measure tensile bond strength, evaluate strength distributions and determine compliance to the requirements of JEDEC 47.

3.9.4 Sample size: 30 bonds from a minimum of 5 devices per lot.

3.9.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33.

3.9.6 Wire Bond Pull (WBP) Test Results:

* Sample Size: 30 bonds, Data from AMKOR_BD#ON0003 WB bondability test data.xls.

Lot# 8654958TG1	Max.	Min.	Mean	Stdev	Cpk
Results (g)	9.40	5.81	7.87	0.79	2.26

3.10 Solderability (SD)

3.10.1 Inspection method: JEDEC Method B102-E

3.10.2 Stress Conditions: 8 hour steam aging prior to solderability test

3.10.3 Purpose: The purpose of this test is to determine the solderability of device package terminal leads intended to be joined to another surface using solder. Family data is acceptable for this test.

3.10.4 Sample size: 5 samples from 3 lot.

3.10.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure.

3.10.6 FM28V100-TG Solderability (SD) Test Results:

	ASE Lot# 0499856TG2	ASE Lot# 0421430TG2	ASE Lot# 0527315TG1
Sample Size	5	5	5
Pass/ Fail	Pass 5/Fail 0	Pass 5/Fail 0	Pass 5/Fail 0

3.11 Physical Dimensions (PD)

3.11.1 Inspection method: JEDEC Method B100-B and MS-024.

3.11.2 Stress Conditions: N/A

3.11.3 Purpose: Package outline and leads measured for concurrence with the Device Specification package drawing. Measurements are made with micrometers to determine adherence to specifications (Jedec MS-024).

3.11.4 Sample size: 10 units per lot

3.11.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. Cpk > 1.3, ppk > 1.67

3.11.6 FM28V100-TG Rev.CA Physical Dimension (PD) Results:

	ASE Lot# 0499856TG2	ASE Lot# 0421430TG2	ASE Lot# 0527315TG1	Cpk
Sample Size	10	10	10	
A2 Overall Package Height Lot average Spec: 0.90 -1.05 mm	1.019	1.024	1.021	1.84
b Lead Width Lot average Spec: 0.17-0.27 mm	0.204	2.06	2.17	2.59
D Overall Package Length Lot Average Spec:11.80 bsc	11.76	11.711	11.768	bsc
E1 Package Width Lot Average Spec: 8 bsc	7.94	7.82	7.95	bsc

3.12 Electrostatic Discharge - Human Body Model (ESD-HBM) AEC-Q100 Test #E2

3.12.1 Test Method: AEC-Q100-002 Rev. D.

3.12.2 Stress Conditions: Human Body Model, 100pF discharge through a 1.5K-ohm resistor.

3.12.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Human Body Model as detailed in JEDEC A114-B (100pF discharged through 1.5K ohms). The devices are subjected to voltage ranging from 500V through 4000V for each group of three (3) devices. ESD testing was done on the FM28V100-G revision AB.

3.12.4 Sample size: 3 parts per voltage group tested.

3.12.5 Accept/Reject Criteria: A device passed a voltage level if all devices in the sample group stressed at that voltage and below pass.

NOTE: A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.12.6 FM28V100-G Rev. AB ESD HBM Test Results:

	Lot #8536300TG2	
	25°C	90°C
500V	0 fails/3	0 fails/3
1000V	0 fails/3	0 fails/3
1500V	0 fails/3	0 fails/3
2000V	0 fails/3	0 fails/3

3.12.7 Conclusion: Devices categorized as Class H1C devices for HBM ESD sensitivity (pass 2000V) per AEC Q100-002.

3.13 Electrostatic Discharge – Charged Device Model (CDM) AEC-Q100 Test #E3

3.13.1 Test Method: AEC-Q100-011 Rev. B

3.13.2 Stress Conditions: Transferring of electrostatic charge between bodies at different electrostatic potentials, with circuitry as described in section 2.1 of AEC–Q100-011 Rev. B, Direct Charge or Field Induced Charge.

3.13.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Charged Device Model as detailed in AEC Q100-011. The devices are subjected to voltage ranges from 250V to 1250V. ESD testing was done on the FM28V100-G revision AB.

3.13.4 Sample size: 3 parts per voltage group tested.

3.13.5 Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.13.6 Test Summary: FM28V100-G Rev. AB ESD – CDM Results

	Lot #8536300TG2	
	25°C	90°C
250V	0 fails/3	0 fails/3
500V	0 fails/3	0 fails/3
750V	0 fails/3	0 fails/3
1000V	0 fails/3	0 fails/3
1250V	0 fails/3	0 fails/3

3.13.7 Conclusion: Devices categorized as Class C5 for ESD-CDM sensitivity (pass 1250V) per AEC Q100-011.

3.14 Latch-up Immunity (LU) AEC-Q100 Test #E4

3.14.1 Test Method: AEC-Q100-004

3.14.2 Stress Conditions: Latch-Up: Must pass - 100mA current injection, each input pin.
Tested to –300mA current injection, each input pin.
Vsupply Over-Voltage Test: 3.65 to 6.4V.

3.14.3 Test Description: The Latch-Up Immunity test assesses the devices susceptibility to latch-up at maximum operating temperatures (90°C). A negative current is applied to each package pin (pin to Vss then pin to Vcc). The current is incremented to -300mA, although AEC Q100-011 only requires –100mA. The device Icc current is measured after each current increment and compared to the maximum value as detailed in the Device Specification. During the Vsupply Over-Voltage Test, the voltage is increased from 3.65 to 6.4V .measuring Icc at each increment after removing the Voltage source. ESD/LU testing was done on FM28V100-G revision AB parts.

3.14.4 Sample size: 6 parts from one lot.

3.14.5 Accept/Reject Criteria: Accept on 0 failures and reject on one failure.

3.14.6 FM28V100-G Rev. AB Latch-Up (LU) Test Results:

Lot Number	Parts Tested	Test Result (90°C)

#8536300TG2	6	0 fails up to ±300mA

3.14.7 Conclusion: All devices performed to greater than -300mA in Latch up Immunity and passed the Vsupply Over-Voltage Test at 90°C.

3.15 Electrical Distributions (ED) AEC-Q100-009 Test #E5

3.15.1 Test Description: Selected parameters from the Characterization test program are tested and data logged at 3 temperatures, 25C, 90C, and -45C. The data is stored in an excel spreadsheet that then has pivot tables created from it to generate Ppks.

3.15.2 Sample size: 30 parts from each of the 3 lots

3.15.3 Accept/Reject Criteria: Accept Ppk>1.67

Electrical Distribution	**Ppks**	**Ppks**	**Ppks**
Lots/Temperatures	**Lot #8536300**	**Lot #8673581**	**Lot #8709155**
+25 Degrees C	Average Ppk = 37.01	Average Ppk = 34.27	Average Ppk = 36.76
+90 Degrees C	Average Ppk = 29.79	Average Ppk = 30.75	Average Ppk = 32.74
-45 Degrees C	Average Ppk = 34.38	Average Ppk = 37.68	Average Ppk = 35.54

3.15.4 Results: Average Ppks > 1.67 for all lots at all temperatures.

3.16 Electrically Induced Gate Leakage (GL) AEC-Q100 Test #E8

3.16.1 Inspection method: AEC-Q100-006 Rev. D.

3.16.2 Stress Conditions: 155°C, ± 20kVDC.

3.16.3 Test Description: This test is used to determine surface mount integrated circuit susceptibility to Electro-Thermally induced Parasitic Gate Leakage.

3.16.4 Sample size: 6 units from one lot.

3.16.5 Accept/Reject Criteria: Accept 0, Reject on 1.

3.16.6 FM25V10-G Rev. AB Gate Leakage (GL) Test Results:

Lot Number	+20kVDC	-20kVDC
8536300	0fails/3parts	0fails/3parts

4 CONCLUSIONS

4.1 Based on the completion of the F-RAM product qualification testing, the FM28V100-TG revision AB is qualified to JEDEC standards and the qualification report is issued.

Document History Page

Document Title: QTP# 130401: 1MB F-RAM MEMORY QUALIFICATION REPORT
Document Number: 001-85810

Rev.	ECN No.	Orig. of Change	Description of Change
**	3883374	CNOR	Initial spec release.
*A	3954246	BECK	Added Reliability Failure Rate Summary

Distribution: WEB

Posting: None