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Cypress Semiconductor
Product Qualification Report

QTP#130105
December 2014
Ramtron#: 02-60-5134

QTP #130105 AEC-Q100 Grade 1 Qual Report, B-W Serial F-RAM Family 4Kb to 64Kb Product Qualification **130nm Technology, TI Fab**	
FM24CL64B-GA	64Kb (8192Kx8bits) I2C 3V Serial F-RAM Memory
FM24CL64B-GATR	64Kb (8192Kx8bits) I2C 3V Serial F-RAM Memory
FM25040B-GA	4Kb (512Kx8bits) I2C 5V Serial F-RAM Memory
FM25040B-GATR	4Kb (512Kx8bits) I2C 5V Serial F-RAM Memory
FM25640B-GA	64Kb (8192Kx8bits) SPI 5V Serial F-RAM Memory
FM25640B-GATR	64Kb (8192Kx8bits) SPI 5V Serial F-RAM Memory
FM25C160B-GA	16Kb (2048Kx8bits) SPI 5V Serial F-RAM Memory
FM25C160B-GATR	16Kb (2048Kx8bits) SPI 5V Serial F-RAM Memory
FM25CL64B-GA	64Kb (8192Kx8bits) SPI 3V Serial F-RAM Memory
FM25CL64B-GATR	64Kb (8192Kx8bits) SPI 3V Serial F-RAM Memory
FM25L04B-GA	4Kb (512Kx8bits) I2C 3V Serial F-RAM Memory
FM25L04B-GATR	4Kb (512Kx8bits) I2C 3V Serial F-RAM Memory

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
02-60-5112 / 124901		TI Process Qualification 130nm F-RAM Process	Aug 2008 / Dec 2012
02-60-5134		QTP #130105 AEC Q-100 Grade 1 Qual Report, B-W Serial F-RAM Family 4Kb to 64Kb Product Qualification	Aug 2011
130105		Ramtron quality integration - paper qual	Jan 2013
130105		Standardize from MSL1 to MSL3	Dec 2014

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate (ELFR)	4800 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate (HTOL)	547,000 DHRs* 616,000 DHRs	0	0.7	55	14 FITs

*****Leverage HTOL data from TI 130nm F-RAM Process QTP#124901 (SPEC#001-85093)

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation
[4] Thermal Total device hours is based on HTOL test and post endurance cycles HTOL test

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

AEC-Q100 Grade 1 Product Qualification Report

(Document #02-60-5134)

PRODUCTS: FM25040B-GA; FM25L04B-GA; FM25C160B-GA; FM25L16B-GA; FM25CL64B-GA; FM25640B-GA; FM24CL64-GA

4Kbit to 64Kbit Memory, SPI and I2C, 3V and 5V

Revision: AA & AB

Foundry Supplier: Texas Instruments & IBM

Package Suppliers: UTL & HANA, Bangkok, Thailand

Issue Date: August 8, 2011

Updated: December 21, 2012

Originated by:

QA/Reliability

TABLE OF CONTENTS

1 SCOPE

1.1 AEC-Q100 Grade 1 Product Family Qualification testing is successfully performed on the Ramtron 130 nm process fab family, initially based on 1Mb TI memory products, with supplementary B/W-Family testing. Package Qualification testing was successfully completed on the 8-lead SOIC Green package assembled at HANA and UTAC. This Qualification Report includes family data for the following products:

FM24CL64B-GA: 64Kb I2C Serial 3V F-RAM Memory, organized as 8,192 x 8 bits
FM25040B-GA: 4Kb I2C Serial 5V F-RAM Memory, organized as 512 x 8 bits
FM25L04B-GA: 4Kb I2C Serial 3V F-RAM Memory, organized as 512 x 8 bits
FM25C160B-GA: 16Kb SPI Serial 5V F-RAM Memory, organized as 2,048 x 8 bits
FM25L16B-GA: 16Kb SPI Serial 3V F-RAM Memory, organized as 2,048 x 8 bits
FM25CL64B-GA: 64Kb SPI Serial 3V F-RAM Memory, organized as 8,192 x 8 bits
FM25640B-GA: 64Kb SPI Serial 5V F-RAM Memory, organized as 8,192 x 8 bits

AEC-Q100 package-related testing is successfully completed on three assembly lots of product from this family, the largest memory size produced at each vendor was selected for testing:

8-lead Green SOIC package at HANA
8-lead Green SOIC package at UTL

1.2 Product testing is designed to assess overall compliance to the AEC-Q100 Rev. G Standard. Random samples were chosen from three lots for each test.

1.3 These products were fabricated at Texas Instruments in Dallas, Texas and IBM in Burlington, VT. Product qualified was assembled at UTL and HANA in Bangkok, Thailand. Qualification stress/testing was performed at Ramtron International Corporation in Colorado Springs, CO, Integra Technologies in Santa Clara, CA and at Innovative Circuits Engineering in San Jose, California.

1.4 The following report details the environmental stress tests performed, test sample sizes, accept/reject criteria, test results and conclusions of this qualification. Test and inspection results performed on the selected qualification lots are also summarized in Table I.

2 APPLICABLE DOCUMENTS

2.1 Ramtron FM24CL64B-GA; FM25040B-GA; FM25L04B-GA; FM25C160B-GA; FM25L16B-GA; FM25CL64B-GA; FM25640B-GA Datasheets, Rev 1.0

2.2 “Failure Mechanism Based Stress Test Qualification for Integrated Circuits” AEC-Q100 Rev. G.

2.3 Ramtron FM25V10-G Qualification Report, Document #02-60-5119, dated November 23, 2009.

3 RELIABILITY STRESS TESTS

3.1 Pre-conditioning of Samples, AEC-Q100 Test #A1

3.1.1 Inspection method: JEDEC JESD22 A113-C

3.1.2 Stress Conditions: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C

3.1.3 Purpose: The purpose of the pre-conditioning of samples prior to HAST, Autoclave and Temperature Cycle is to simulate typical solder reflow operation.

3.1.4 Sample size: 80 units per lot per test (240 units from each lot)

3.1.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure from sample. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.1.6 Pre-conditioning Test Results:

TI 130nm Fabricated 1Mbit Monolithic F-RAM AEC-Q100 Grade 1	FM25V10-G Fab Lot# 8536300	FM25V10-G Fab Lot# 8673581	FM25V10-G Fab Lot# 8709155
Post Pre-Condition Electrical Test @ 25 ºC	0fails/240parts	0fails/240parts	0fails/240parts

W/B-Family Product AEC-Q100 Grade 1	FM25W256-G (256Kbit) UTL Assembly Lot 00001G	FM24W256-G (256Kbit) UTL Assembly Lot 00001G	FM24C64B-G (64Kbit) HANA Assembly Lot 00001G8
Post Pre-Condition Electrical Test @ 25 ºC	0fails/240parts	0fails/240parts	0fails/240parts

3.2 Highly Accelerated Stress Test (HAST), AEC-Q100 Test #A2

3.2.1 Inspection methods: **Preconditioning**- JEDEC JESD22 Method A113-C;
HAST- JEDEC JESD22 Method A110-B

3.2.2 Stress Conditions: **Preconditioning**: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C
HAST: 130°C, 85% Relative Humidity, P=33.3psia, biased at Vddmax, 96 hours

3.2.3 Purpose: The purpose of the Pre-conditioned HAST test is to detect defective packaging materials and processes used for the assembly of these parts. Preconditioning simulates a standard multiple solder reflow operation. HAST conditions accelerate the penetration of moisture through the package molding material and die passivation to the active die surface. Die surface moisture, in turn, can initiate corrosion, ionic migration and other processes resulting in functional or parametric part failure.

3.2.4 Sample size: 77 devices per lot

3.2.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 125°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.2.6 Pre-Conditioned HAST Test Result:

W/B-Family Product AEC-Q100 Grade 1	FM25W256-G (256Kbit) UTL Assembly Lot 00001G	FM24W256-G (256Kbit) UTL Assembly Lot 00001G	FM24C64B-G (64Kbit) HANA Assembly Lot 00001G8
Post Pre-Conditioned HAST Electrical Test @ 25 ºC	0fails/77parts	0fails/77parts	0fails/77parts
Post Pre-Conditioned HAST Electrical Test @ 125ºC	0fails/77parts	0fails/77parts	0fails/77parts

3.3 Preconditioned Autoclave (AC), AEC-Q100 Test #A3

3.3.1 Inspection Method: Preconditioning: JEDEC JESD22 Method A113-C
Autoclave: JEDEC JESD22 Method A102 Rev. C

3.3.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C
Autoclave: 121ºC, 29.7 psia 100% Relative Humidity, 96 hrs

3.3.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Unbiased autoclave is performed to evaluate the moisture resistance of non hermetic packages. This is a highly accelerated test which employs conditions of pressure, humidity and temperature to accelerate moisture penetration through external protective materials or along the interface between external protective materials and the metallic conductors passing through it.

3.3.4 Sample Size 77 parts per lot

3.3.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C after stress. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.3.6 Pre-Conditioned Autoclave (AC) Test Results:

TI 130nm Fabricated 1Mbit Monolithic F-RAM AEC-Q100 Grade 1	FM25V10-G Fab Lot# 8536300	FM25V10-G Fab Lot# 8673581	FM25V10-G Fab Lot# 8709155
Post Pre-Conditioned AC Electrical Test @ 25 ºC	0fails/77parts	0fails/77parts	0fails/77parts

W/B-Family Product AEC-Q100 Grade 1	FM25W256-G (256Kbit) UTL Assembly Lot 00001G	FM24W256-G (256Kbit) UTL Assembly Lot 00001G	FM24C64B-G (64Kbit) HANA Assembly Lot 00001G8
Post Pre-Conditioned AC Electrical Test @ 25 ºC	0fails/77parts	0fails/77parts	0fails/77parts

3.4 Preconditioned Temperature Cycling (TC), AEC-Q100 Test #A4

3.4.1 Inspection method: Preconditioning: JEDEC Method A113-C;
Temperature Cycling: JESD22, Method A104, Rev. B

3.4.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 3 soak conditions (30°C, 60% Relative Humidity for 192 hrs), three cycles of reflow at 260 °C
Temperature Cycling: -65°C to +150°C, 500 cycles
Wire Pull on decapped units – 3 grams min

3.4.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Temperature cycling stress testing is used to subject devices to severe temperature gradients by cycling the parts into hot and cold air. This test evaluates package strength, bond quality, and assembly process consistency. The test will reveal any thermal expansion mismatches in the die or die/package interfaces. At the conclusion of the temperature cycling test, an

electrical functional and parametric test is performed at 25°C and 125°C. The 5 units from each lot are decapped and Wire Pull testing performed.

3.4.4 Sample size: 77 parts per lot.

3.4.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C and 125°C after stress. 5 decapped units for wire bond pull testing must meet 3 gram minimum. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.4.6 Pre-Conditioned TC Test Results:

W/B-Family Product AEC-Q100 Grade 1	FM25W256-G (256Kbit) UTL Assembly Lot 00001G	FM24W256-G (256Kbit) UTL Assembly Lot 00001G	FM24C64B-G (64Kbit) HANA Assembly Lot 00001G8
Post Pre-Conditioned TC Electrical Test @ 25 °C (500cycles -65°C to +150°C)	0fails/77parts	0fails/77parts	0fails/77parts
Post Pre-Conditioned TC Electrical Test @ 125°C (500cycles -65°C to +150°C)	0fails/77parts	0fails/77parts	0fails/77parts
Post Pre-Conditioned TC Wire Pull Test	0fails/5 units	0fails/5 units	0fails/5 units

3.5 High Temperature Storage Life (HTSL), AEC-Q100 Test #A6

3.5.1 Inspection method: JESD22, Method A103, Rev. B

3.5.2 Stress Conditions: 150°C, 500 hrs.

3.5.3 Purpose: The purpose of the high temperature storage life test is determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms, including non volatile memory devices.

3.5.4 Sample size: One Lot of 45 samples

3.5.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure for a sample size of 45 parts from 1 lot. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 125 °C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.5.6 High Temperature Storage Life (HTSL) Test Results:

W/B-Family Product AEC-Q100 Grade 1	FM24C64B-G (64Kbit) Fab Lot L3804G8	FM25640B-G (64Kbit) Fab Lot L3807G5	FM25C160B-G (16Kbit) Fab Lot AM1300G1 (Rev AB)	FM24CL64B (64Kbit) Fab Lot L3803G4
Post HTSL (1,000 hour, 150°C Bake) Electrical Test 25°C	0fails/45parts	0fails/45parts	0fails/45parts	0fails/45parts
Post HTSL (1,000 hour, 150°C Bake) Electrical Test 125°C	0fails/45parts	0fails/45parts	0fails/45parts	0fails/45parts

3.6 High Temperature Operating Life (HTOL), AEC-Q100 Test #B1

3.6.1 Inspection method: JESD22, Method A108, Rev. B

3.6.2 Stress Conditions: 125°C, Vddmax, Operating 1000 hrs

3.6.3 Purpose: The purpose of the high temperature operating life test is to simulate device operation at elevated temperatures and higher than nominal operating voltages. The data obtained from this test is translated to a lower temperature (55°C) by using the Arhennius temperature acceleration modeling. The acceleration factor and distribution of failures accumulated is then fit to the appropriate failure distribution equation to statistically predict product end of operating life.

3.6.4 Sample size: Three lots of 77 samples each.

3.6.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C, 125°C and -40°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.6.6 HTOL Test Results:

TI 130nm Fabricated 1Mbit Monolithic F-RAM AEC-Q100 Grade 1	FM25V10-G Fab Lot# 8536300	FM25V10-G Fab Lot# 8673581	FM25V10-G Fab Lot# 8709155
Endurance: 1 E5 Cycles at 3.65V	0fails/77parts	0fails/77parts	0fails/77parts
Post Pre-Conditioned HTOL Electrical Test @ 25 ºC	0fails/77parts	0fails/77parts	0fails/77parts
Post Pre-Conditioned HTOL Electrical Test @ 125ºC	0fails/77parts	0fails/77parts	0fails/77parts
Post Pre-Conditioned HTOL Electrical Test @ -40 ºC	0fails/77parts	0fails/77parts	0fails/77parts

W/B-Family Product AEC-Q100 Grade 1	FM24W256-G (256Kbit) Fab Lot 00001G	FM5640B-G (64Kbit) Fab Lot L3807G5	FM24C64B-G (64Kbit) Fab Lot L3804G8	FM25C160B-G (16Kbit) Fab Lot AM1300G1 (Rev AB)	FM24CL64B-G (64Kbit) Lot L3803G4
Post Pre-Conditioned HTOL Electrical Test @ 25 ºC	0fails/77parts	0fails/77parts	0fails/77parts	0fails/77parts	0fails/77parts
Post Pre-Conditioned HTOL Electrical Test @ 125ºC	0fails/77parts	0fails/77parts	0fails/77parts	0fails/77parts	0fails/77parts
Post Pre-Conditioned HTOL Electrical Test @ -40 ºC	16fails/77parts* (**not** pre-tested at -40C)	0fails/77parts(pre & post tested at -40C)	0fails/77parts(pre & post tested at -40C)	0fails/77parts(pre & post tested at -40C)	0fails/77parts(pre & post tested at -40C)

*Cold Temperature Failures resulted in TPU specification change (look-ahead lot not pre-tested at -40C). Test escape, not related to HTOL stress.

3.7 Early Life Failure Rate (ELFR), AEC-Q100 Test #B2

3.7.1 Inspection method: AEC-Q100-008.

3.7.2 Stress Conditions: 125°C, Vddmax, 48 hours.

3.7.3 Test Description: The units are tested per the High Temp Operating Life requirements of Jedec 22-A108.

3.7.4 Sample size: 800 per lot

3.7.5 Accept/Reject Criteria: Accept on 0, reject on 1.

3.7.6 Early Life Failure Rate (ELFR) Test Results:

TI 130nm Fabricated 1Mbit Monolithic F-RAM AEC-Q100 Grade 1	FM25V10-G Fab Lot# 8536300	FM25V10-G Fab Lot# 8673581	FM25V10-G Fab Lot# 8709155
Post Pre-Conditioned ELFR Electrical Test @ 25 ºC	0fails/800parts	0fails/800parts	0fails/800parts
Post Pre-Conditioned ELFR Electrical Test @ 125ºC	0fails/800parts	0fails/800parts	0fails/800parts

W/B-Family Product AEC-Q100 Grade 1	FM25640B-G (64Kbit) Fab Lot L3807G5	FM24C64B-G (64Kbit) Fab Lot L3804G8	FM25C160B-G (64Kbit) Fab Lot AM1300G1 (Rev AB)
Post Pre-Conditioned ELFR Electrical Test @ 25 ºC	0fails/800parts	0fails/800parts	0fails/800parts
Post Pre-Conditioned ELFR Electrical Test @ 125ºC	0fails/800parts	0fails/800parts	0fails/800parts

3.8 NVM Endurance, Data Retention and Operational Life (EDR), AEC-Q100 Test #B3

3.8.1 Inspection method: AEC-Q100-005

3.8.2 Stress Conditions: Program/Endurance: 1E5 Cycles at 3.65V
High Temperature Storage: 150°C, 1000 hrs.

3.8.3 Purpose: Devices are first exercised through the Program/Endurance test, then HTSL.

3.8.4 Sample size: 77 per lot.

3.8.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 125°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.8.6 NVM Endurance, Data Retention, and HTSL:

TI 130nm Fabricated 1Mbit Monolithic F-RAM AEC-Q100 Grade 1	FM25V10-G Fab Lot# 8536300
Endurance Testing per AEC Q100-005 1E 5 Cycles, 3.65V prior to 150C bake	0 fails/77 parts
Read Zeros	0 fails/77 parts

Read Ones	0 fails/77 parts

W/B-Family Product AEC-Q100 Grade 1	FM25640B-G (64Kbit) Fab Lot #L3807G5	FM24C64B-G (64Kbit) Fab Lot #L3804G8	FM25C160B-G (64Kbit) Fab Lot AM1300G1 (Rev AB)	FM24CL64B-G (64Kbit) Fab Lot #L3803G4	F25W256-G Fab Lot #00001G	FM24W256-G Fab Lot #00001G
Read Zeros	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts	0 fails/69 parts	0 fails/76 parts
Read Ones	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts	0 fails/69 parts	0 fails/76 parts
Post RETN Electrical Test 25°C (HTSL)	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts	0 fails/69 parts	0 fails/76 parts
Post RETN Electrical Test 125°C (HTSL)	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts	0 fails/45 parts		

3.9 Wire Bond Shear Test (WBS), AEC-Q100 Test #C1

3.9.1 Inspection Method: AEC-Q100-001

3.9.2 Stress Conditions: 12.4 grams minimum.

3.9.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices. Family data is acceptable for this test.

3.9.4 Sample size: 30 bonds from a minimum of 5 devices

3.9.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.9.6 Wire Bond Shear (WBS) Test Results: (Family Data)

W/B-Family Product Assembled at HANA	Min	Avg	CPK
FM24C04B-GA	15.01	22.88	1.73
FM24C16B-G	13.74	22.43	1.62
FM24C64B-GA	15.10	21.47	1.71
FM24CL04B-GA	15.05	19.22	1.51

W/B-Family Product Assembled at UTAC	Min	Avg	PPK
FM25040B-G	20.65	22.46	3.45
FM25L04B-G	20.50	24.17	2.20
FM25640B-G	20.79	23.62	2.42
FM25CL64B-G	20.15	23.29	2.44

3.10 Wire Bond Pull Test (WBP), AEC-Q100 Test #C2

3.10.1 Inspection Method: MIL-STD883 Method 2011

3.10.2 Stress Conditions: For gold bond wires <1mil diameter, wipe bond pull is performed with the hook over the ball bond, and not mid-wire method; 2.4g min.

3.10.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices. Family data is acceptable for this test.

3.10.4 Sample size: 30 bonds from a minimum of 5 devices

3.10.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.10.6 Wire Bond Shear (WBS) Test Results: (Family Data)

W/B-Family Product Assembled at HANA	Min	Avg	CPK
FM24C04B-GA	5.01	6.57	3.73
FM24C16B-G	5.04	6.53	3.66
FM24C64B-GA	5.31	6.32	4.10
FM24CL04B-GA	5.16	6.50	4.05

W/B-Family Product Assembled at UTAC	Min	Avg	PPK
FM25040B-G	6.66	7.25	7.10
FM25L04B-G	6.32	7.14	4.25
FM25640B-G	6.86	7.41	4.62
FM25CL64B-G	6.69	7.29	4.53

3.11 **Solderability (SD), AEC-Q100 Test #C3**

3.11.1 Inspection method: JEDEC Method B102-C

3.11.2 Stress Conditions: 8 hour steam aging prior to solderability test

3.11.3 Purpose: The purpose of this test is to determine the solderability of device package terminal leads intended to be joined to another surface using solder. Family data is acceptable for this test.

3.11.4 Sample size: 15 samples from 1 lot.

3.11.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure.

3.11.6 Solderability (SD) Test Results: (Family Data)

	8-Lead Green SOIC Assembled at UTL Lot #00001G1, FM24W256-G	8-Lead Green SOIC Family Data from HANA
Sample Size	15	15
Pass/fail	15 passes/0 fails	15 passes/0 fails

3.12 **Physical Dimensions (PD), AEC-Q100 Test #C4**

3.12.1 Inspection method: JEDEC Method B100

3.12.2 Stress Conditions: N/A

3.12.3 Purpose: Package outline and leads measured for concurrence with the Device Specification package drawing. Measurements are made with micrometers to determine adherence to specifications (Jedec MS-012). Family data is acceptable for this test.

3.12.4 Sample size: 10 units per lot

3.12.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. Cpk > 1.3, ppk > 1.67

3.12.6 Family Data Physical Dimension (PD) Results:

HANA 8-lead Green SOIC (02-60-5120)	Lot# 94078052	Lot# 94725581	Lot# 95378251	Ppk
Sample Size	10	10	10	
A Overall Package Height Lot average Spec: 1.35-1.75mm	1.513	1.544	1.54	5.28
b Lead Width Lot average Spec: .33-.51 mm	0.453	0.447	0.438	3.46
D Overall Package Length Lot Average Spec:4.80-5.00mm	4.925	4.954	4.961	3.14
E Overall Package Width Lot Average Spec: 5.80-6.20mm	5.941	5.92	5.948	7.4

UTL Green 8-lead SOIC (02-60-5113)				
Sample Size	10	10	10	Ppk
A Overall Package Height Lot average Spec: 1.35-1.75mm	1.6	1.596	1.599	7.46
b Lead Width Lot average Spec: .33-.51 mm	0.431	0.435	0.448	2.34
D Overall Package Length Lot Average Spec:4.80-5.00mm	4.931	4.925	4.919	2.26
E Overall Package Width Lot Average Spec: 5.80-6.20mm	6.028	6.035	6.037	6.67

3.13 **Electrostatic Discharge - Human Body Model (ESD-HBM) AEC-Q100 Test #E2**

3.13.1 Test Method: AEC-Q100-002

3.13.2 Stress Conditions: Human Body Model, 100pF discharge through a 1.5K-ohm resistor.

3.13.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Human Body Model as detailed in JEDEC A114-B (100pF discharged through 1.5K ohms). The devices are subjected to voltage ranging from 500V through 4500V for each group of three (3) devices.

3.13.4 Sample size: 3 parts per voltage group tested.

3.13.5 Accept/Reject Criteria: A device passed a voltage level if all devices in the sample group stressed at that voltage and below pass.

NOTE: A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.13.6 ESD HBM Test Results:

Voltage	FM24CL64B Lot # 00001G9	FM25040B Lot # 00001G	FM25L04B Lot # 00001G1	FM25C160B Lot # L4103G3	FM25L16B Lot # L3807G11	FM25640B Lot# L3807G5	25CL64B Lot # 00001G3
HBM 500V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
HBM 1000V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
HBM 1500V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
HBM 2000V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
HBM 2500V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
HBM 3000V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
HBM 3500V	Pass	**Pass**	Pass	Pass	Pass	Pass	Pass
HBM 4000V	Pass	Fail	Pass	Pass	Pass	Pass	Pass
HBM 4500V	**Pass**	Fail	**Pass**	**Pass**	**Pass**	**Pass**	**Pass**

3.14 Electrostatic Discharge – Charged Device Model (CDM) AEC-Q100 Test #E3

3.14.1 Test Method: AEC-Q100-011

3.14.2 Stress Conditions: Transferring of electrostatic charge between bodies at different electrostatic potentials, with circuitry as described in section 2.1 of AEC–Q100-011 Rev. B, Direct Charge or Field Induced Charge.

3.14.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Charged Device Model as detailed in AEC Q100-011. The devices are subjected to voltage ranges from 250V to 1250V.

3.14.4 Sample size: 3 parts per voltage group tested.

3.14.5 Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

3.14.6 Test Summary: ESD CDM Results

Voltage	FM24CL64B Lot # 00001G9	FM25040B Lot # 00001G	FM25L04B Lot # 00001G1	FM25C160B Lot # L4103G3	FM25L16B Lot # L3807G11	FM25640B Lot# L3807G5	25CL64B Lot # 00001G3
CDM 250V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
CDM 500V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
CDM 750V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
CDM 1000V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
CDM 1250V	**Pass**	**Pass**	**Pass**	**Pass**	**Pass**	**Pass**	**Pass**

3.15 **Latch-up Immunity (LU) AEC-Q100 Test #E4**

3.15.1 Test Method: AEC-Q100-004

3.15.2 Stress Conditions: Latch-Up: Must pass - 100mA current injection, each input pin.
Tested to –300mA current injection, each input pin.
Vsupply Over-Voltage Test

3.15.3 Test Description: The Latch-Up Immunity test assesses the devices susceptibility to latch-up at maximum operating temperatures (125°C). A negative current is applied to each package pin (pin to Vss then pin to Vcc). The current is incremented to -300mA, although AEC Q100-011 only requires –100mA. The device Icc current is measured after each current increment and compared to the maximum value as detailed in the Device Specification.

3.15.4 Sample size: 6 parts from one lot.

3.15.5 Accept/Reject Criteria: Accept on 0 failures and reject on one failure.

3.15.6 Latch-Up (LU) Test Results:

Stress	FM24CL64B Lot # 00001G9	FM25040B Lot # 00001G	FM25L04B Lot # 00001G1	FM25C160B Lot # L4103G3	FM25L16B Lot # L3807G11	FM25640B Lot# L3807G5	25CL64B Lot # 00001G3
LU +300mA at 125C	Pass	Pass	Pass	Pass	Pass	Pass	Pass

3.16 **Electrical Distributions (ED) AEC-Q100-009 Test #E5**

3.16.1 Test Description: Selected parameters from the Characterization test program are tested and datalogged at 3 temperatures, 25C, 125C, and -45C. The data is stored in an excel spreadsheet that then has pivot tables created from it to generate Ppks.

3.16.2 Sample size: 30 parts from each of the 3 lots

3.16.3 Accept/Reject Criteria: Accept Ppk>1.67

Electrical Distribution	FM25CL64B-G	FM25L04B-G	FM25040B-G
Lots/Temperatures	**Lot: A00001G3** (30 pcs)	**Lot:A00001G1** (30 pcs)	**Lot:A00001G** (30 pcs)
+25 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67
+90 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67
-45 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67

3.15.4 Results: Pass – All average Ppks > 1.67 for all lots at all temperatures.

3.17 Electrically Induced Gate Leakage (GL) AEC-Q100 Test #E8

3.17.1 Inspection method: AEC-Q100-006 Rev. D.

3.17.2 Stress Conditions: 155°C, ± 20kVDC.

3.17.3 Test Description: This test is used to determine surface mount integrated circuit susceptibility to Electro-Thermally induced Parasitic Gate Leakage.

3.17.4 Sample size: 6 units from one lot.

3.17.5 Accept/Reject Criteria: Accept 0, Reject on 1.

3.17.6 Gate Leakage (GL) Test Results:

Part Number	Lot Number	+20kVDC	-20kVDC
FM25V10-G	Lot 8536300	0fails/3parts	0fails/3parts
FM24W256-G	Lot 00001G	0fails/3parts	0fails/3parts
FM25CL64B	Lot #L3802G7	0fails/3parts	0fails/3parts

4 CONCLUSIONS

4.1 Based on this successful completion of the FRAM Product Qualification testing, the FM25040B-GA; FM25L04B-GA; FM25C160B-GA; FM25L16B-GA; FM25CL64B-GA; FM25640B-GA; FM24CL64-GA, Revisions AA and AB, are AEC-Q100 Grade 1 qualified products.

5 ADDITIONAL REPORTS and DATA

5.1 Electrostatic Discharge – Machine Model (MM)

5.1.1 Test Method: JEDEC 22-A115

5.1.2 Stress Conditions: Machine Model, 200pF discharge through no resistance.

5.1.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Machine Model test method.

5.1.4 Sample size: 3 parts per voltage group tested.

5.1.5 Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

5.1.6 Test Summary: ESD MM Results

Voltage	FM24CL64B Lot # 00001G9	FM25040B Lot # 00001G	FM25L04B Lot # 00001G1	FM25C160B Lot # L4103G3	FM25L16B Lot # L3807G11	FM25640B Lot# L3807G5	25CL64B Lot # 00001G3
100V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
200V	Pass	Pass	Pass	Pass	Pass	Pass	Pass
250V	Pass	**Pass**	Pass	Pass	Pass	Pass	Pass
300V	**Pass**	Fail	**Pass**	**Pass**	**Pass**	**Pass**	**Pass**
400V	Fail	Fail	Fail	Fail	Fail	Fail	Fail

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Rev.	ECN No.	Orig. of Change	Description of Change
**	3868901	CNOR	Initial spec release.
*A	3913713	BECK	Added Reliability Failure Rate Summary
*B	3953951	BECK	Correct font and typo of " 14 ITs" to "14 FITs"
*C	4559805	BECK	Update Page 1 to new template. Standardized from MSL1 to MSL3

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