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# Cypress Semiconductor Product Qualification Report

**QTP#125003**  
**January 2013**  
**Ramtron#: 02-60-5127**

<b>QTP #125003 128Kb and 256Kb F-RAM AEC-Q100 Memory Product Qualification</b>	
<b>130nm Technology, TI Fab</b>	
FM25V01-G	128Kb (16,384Kx8bits) Serial 3V F-RAM Memory
FM25V01-GTR	128Kb (16,384Kx8bits) Serial 3V F-RAM Memory
FM25V02-G	256Kb (32,768Kx8bits) Serial 3V F-RAM Memory
FM25V02-GTR	256Kb (32,768Kx8bits) Serial 3V F-RAM Memory
FM24V01-G	128Kb (16,384Kx8bits) Serial 3V F-RAM Memory
FM24V01-GTR	128Kb (16,384Kx8bits) Serial 3V F-RAM Memory
FM24V02-G	256Kb (32,768Kx8bits) Serial 3V F-RAM Memory
FM24V02-GTR	256Kb (32,768Kx8bits) Serial 3V F-RAM Memory
FM25V02-DG	256Kb (32,768Kx8bits) Serial 3V F-RAM Memory
FM25V02-DGTR	256Kb (32,768Kx8bits) Serial 3V F-RAM Memory

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**QUALIFICATION HISTORY**

<b>Qual Report</b>		<b>Description of Qualification Purpose</b>	<b>Date Comp</b>
02-60-5112 / 124901		TI Process Qualification 130nm F-RAM Process	Aug 2008 / Dec 2012
02-60-5127		QTP #125003 128Kb and 256Kb F-RAM AEC-Q100 Memory Product Qualification	Dec 2010
125003		Ramtron quality integration - paper qual	Jan 2013

### RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF <sup>3</sup>	Failure Rate
High Temperature Operating Life Early Failure Rate (ELFR)	2400 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life <sup>1,2</sup> , Long Term Failure Rate (HTOL)	547,000 DHRs* 231,000 DHRs	0	0.7	55	21 FITs

\*Leverage HTOL data from TI 130nm F-RAM Process QTP#124901 (SPEC#001-85093)

<sup>1</sup> Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

<sup>2</sup> Chi-squared 60% estimations used to calculate the failure rate.

<sup>3</sup> Thermal Acceleration Factor is calculated from the Arrhenius equation

<sup>4</sup> Thermal Total device hours is based on HTOL test and post endurance cycles HTOL test

$$AF = \exp \left[ \frac{E_A}{k} \left[ \frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

$E_A$  = The Activation Energy of the defect mechanism.

$k$  = Boltzmann's constant =  $8.62 \times 10^{-5}$  eV/Kelvin.

$T_1$  is the junction temperature of the device under stress and  $T_2$  is the junction temperature of the device at use conditions.

# **AEC-Q100 Grade 3 Product Qualification Report**

(Document #02-60-5127)

## **FM25V01-G, FM25V02-G, FM24V01-G and FM24V02-G**

### **128Kb & 256Kb F-RAM® SPI and I2C Serial Memory Parts**

**Revision: AB**

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**Foundry Supplier: Texas Instruments**

**Package Suppliers: UTL & HANA, Bangkok, Thailand; Lingsen  
Precision Industries, Taichung, Taiwan**

**Issue Date:**

**December 10, 2010**

**Originated by:**

**QA/Reliability**

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## 1 SCOPE

- 1.1 AEC-Q100 Qualification die-related testing is successfully performed on the Ramtron 130 nm process fab family with memory size up to 1Mb, offered in an 8-lead SOIC Green package. This Qualification Report includes family data for the following products:

FM25V02-G: 256Kb SPI Serial 3V F-RAM Memory, organized as 32,768 x 8 bits

FM25V01-G: 128Kb SPI Serial 3V F-RAM memory, organized as 16,384 x 8 bits

FM24V02-G: 256Kb I2C Serial 3V F-RAM Memory, organized as 32,768 x 8 bits

FM24V01-G: 128Kb I2C Serial 3V F-RAM memory, organized as 16,384 x 8 bits

AEC-Q100 package-related testing is successfully completed on three assembly lots of product from this wafer fab family, the largest memory size produced at each vendor was selected for testing:

8-lead Green SOIC package, containing a die with memory size up to 1Mb at HANA

8-lead Green SOIC package, containing a die with memory size up to 256Kb at UTL

8-lead Green SOIC package, containing a die with memory size up to 128Kb at Lingsen

- 1.2 Product testing is designed to assess overall compliance to the AEC-Q100 Rev. G Standard. Random samples were chosen from three lots for each test.
- 1.3 These devices were fabricated at Texas Instruments in Dallas, Texas. Product qualified was assembled at UTL and Hana in Bangkok, Thailand and at Lingsen Precision Industries in Taichung, Taiwan. Qualification stress/testing was performed at Ramtron International Corporation in Colorado Springs, CO, Integra Technologies in Santa Clara, CA and at Innovative Circuits Engineering in San Jose, California.
- 1.4 The following report details the environmental stress tests performed, test sample sizes, accept/reject criteria, test results and conclusions of this qualification. Test and inspection results performed on the selected qualification lots are also summarized in Table I.

## 2 APPLICABLE DOCUMENTS

- 2.1 Ramtron FM25V02-G Datasheet dated June, 2010, Rev. 2.0
- 2.2 Ramtron FM25V01-G Datasheet, dated May, 2010, Rev. 1.0
- 2.3 Ramtron FM24V02-G Datasheet dated May, 2010, Rev. 2.0
- 2.4 Ramtron FM24V01-G Datasheet, dated October, 2010, Rev. 1.0
- 2.5 "Failure Mechanism Based Stress Test Qualification for Integrated Circuits" AEC-Q100 Rev. G.
- 2.6 Ramtron FM25V10-G Qualification Report, Document #02-60-5119, dated November 23, 2009.

## 3 RELIABILITY STRESS TESTS

### 3.1 Pre-conditioning of Samples, AEC-Q100 Test #A1

- 3.1.1 Inspection method: JEDEC JESD22 A113-C
- 3.1.2 Stress Conditions: Moisture Sensitivity Level 1 soak conditions (85°C, 85% Relative Humidity for 168 hrs), three cycles of reflow at 260 °C
- 3.1.3 Purpose: The purpose of the pre-conditioning of samples prior to HAST, Autoclave and Temperature Cycle is to simulate typical solder reflow operation.
- 3.1.4 Sample size: 80 units per lot per test (240 units from each lot)

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3.1.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure from sample. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.1.6 Pre-conditioning Test Results: (Family Data)

Device/Lot Number	Lingsen 8-lead SOIC Green Lot # 4537874 (FM24V01-G)	UTL 8-lead SOIC Green Lot# 04838552 (FM25V02-G)	HANA 8-lead SOIC Green Lot# 04505521 (FM25V10-G)
Post Pre-Condition Electrical Test @ 25 °C	0 fails/240 parts	0 fails/240 parts	0 fails/240 parts
Post Pre-Condition Electrical Test @ 85 °C – for HAST and Temp. Cycle	0 fails/160 parts	0 fails/160 parts	0 fails/160 parts

### 3.2 Highly Accelerated Stress Test (HAST), AEC-Q100 Test #A2

3.2.1 Inspection methods: **Preconditioning-** JEDEC JESD22 Method A113-C;

**HAST-** JEDEC JESD22 Method A110-B

3.2.2 Stress Conditions: **Preconditioning:** Moisture Sensitivity Level 1 soak conditions (85°C, 85% Relative Humidity for 168 hrs), three re-flow cycles at 260 °C.

**HAST:** 130°C, 85% Relative Humidity, P=33.3psia, biased at 3.65 vdc, 96 hours

3.2.3 Purpose: The purpose of the Pre-conditioned HAST test is to detect defective packaging materials and processes used for the assembly of these parts. Preconditioning simulates a standard multiple solder reflow operation. HAST conditions accelerate the penetration of moisture through the package molding material and die passivation to the active die surface. Die surface moisture, in turn, can initiate corrosion, ionic migration and other processes resulting in functional or parametric part failure.

3.2.4 Sample size: 77 devices per lot

3.2.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.2.6 Pre-Conditioned HAST Test Result: (Some Family Data)

Device/Lot Number	Lingsen 8-lead SOIC Green Lot # 4537874 (FM24V01-G)	UTL 8-lead SOIC Green Lot# 04838552 (FM25V02-G)	HANA 8-lead SOIC Green Lot# 04505521 (FM25V10-G)
Post Pre-condition HAST Electrical Test @ 25°C	0 fails /77 parts	0 fails /77 parts	0 fails /77 parts
Post Pre-condition HAST Electrical Test @ 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

### 3.3 Preconditioned Autoclave (AC), AEC-Q100 Test #A3

3.3.1 Inspection Method: **Preconditioning:** JEDEC JESD22 Method A113-C

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#### Autoclave: JEDEC JESD22 Method A102 Rev. C

- 3.3.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 1 soak conditions (85°C, 85% Relative Humidity for 168 hrs), three cycles of reflow at 260 °C  
Autoclave: 121°C, 29.7 psia 100% Relative Humidity, 96 hrs
- 3.3.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Unbiased autoclave is performed to evaluate the moisture resistance of non hermetic packages. This is a highly accelerated test which employs conditions of pressure, humidity and temperature to accelerate moisture penetration through external protective materials or along the interface between external protective materials and the metallic conductors passing through it.
- 3.3.4 Sample Size 77 parts per lot
- 3.3.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C after stress. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.
- 3.3.6 Pre-Conditioned Autoclave (AC) Test Results: (Some Family Data)

Device/Lot Number	Lingsen 8-lead SOIC Green Lot # 4537874 (FM24V01-G)	UTL 8-lead SOIC Green Lot# 04838552 (FM25V02-G)	HANA 8-lead SOIC Green Lot# 04505521 (FM25V10-G)
Post Pre-condition Autoclave Electrical Test 25 °C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

#### 3.4 Preconditioned Temperature Cycling (TC), AEC-Q100 Test #A4

- 3.4.1 Inspection method: Preconditioning: JEDEC Method A113-C;  
Temperature Cycling: JESD22, Method A104, Rev. B
- 3.4.2 Stress Conditions: Preconditioning: Moisture Sensitivity Level 1 soak conditions (85°C, 85% Relative Humidity for 168 hrs), three cycles of reflow at 260 °C  
Temperature Cycling: -50°C to +125°C, 500 cycles  
Wire Pull on decapped units – 3 grams min
- 3.4.3 Test Description: Preconditioning conditions simulate a standard multiple solder reflow operation. Temperature cycling stress testing is used to subject devices to severe temperature gradients by cycling the parts into hot and cold air. This test evaluates package strength, bond quality, and assembly process consistency. The test will reveal any thermal expansion mismatches in the die or die/package interfaces. At the conclusion of the temperature cycling test, an electrical functional and parametric test is performed at 25°C and 85°C. The 5 units from each lot are decapped and Wire Pull testing performed.
- 3.4.4 Sample size: 77 parts per lot.
- 3.4.5 Accept/Reject Criteria: Accept on 0 failures, Reject on 1 failure. A device is considered a failure if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at 25°C and 85°C after stress. 5 decapped units for wire bond pull testing must meet 3 gram minimum. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.
- 3.4.6 Pre-Conditioned TC Test Results: (Some Family Data)

Device/Lot Number	Lingsen 8-lead SOIC Green Lot # 4537874 (FM24V01-G)	UTL 8-lead SOIC Green Lot# 04838552 (FM25V02-G)	HANA 8-lead SOIC Green Lot# 04505521 (FM25V10-G)
Post Pre-condition Autoclave Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post Pre-condition Autoclave Electrical Test 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Wire Bond Pull Test 3 grams minimum		0 fails Min. 6.27g	0 fails Min. 3.38g

### 3.5 High Temperature Storage Life (HTSL), AEC-Q100 Test #A6

3.5.1 Inspection method: JESD22, Method A103, Rev. B

3.5.2 Stress Conditions: 150°C, 500 hrs.

3.5.3 Purpose: The purpose of the high temperature storage life test is determine the effects of time and temperature, under storage conditions, for thermally activated failure mechanisms, including non volatile memory devices.

3.5.4 Sample size: One Lot of 45 samples

3.5.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure for a sample size of 45 parts from 1 lot. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

3.5.6 FM 25V05-G Rev. AB High Temperature Storage Life (HTSL) Test Results: (Family Data)

FM25V10-G Lot	Lot# 8709155
Post HTSL Electrical Test 25°C	0 fails/45 parts
Post HTSL Electrical Test 85°C	0 fails/45 parts

### 3.6 High Temperature Operating Life (HTOL), AEC-Q100 Test #B1

3.6.1 Inspection method: JESD22, Method A108, Rev. B

3.6.2 Stress Conditions: 125°C, 3.65 Vdc, operating 1000 hrs

3.6.3 Purpose: The purpose of the high temperature operating life test is to simulate device operation at elevated temperatures and higher than nominal operating voltages. The data obtained from this test is translated to a lower temperature (55°C) by using the Arrhenius temperature acceleration modeling. The acceleration factor and distribution of failures accumulated is then fit to the appropriate failure distribution equation to statistically predict product end of operating life.

3.6.4 Sample size: Three lots of 77 samples each.

3.6.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC

characteristics at an operating temperature of 25°C, 85°C and -40°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

### 3.6.6 FM 25V10-G Rev. AB HTOL Test Results: (Family Data)

FM25V10-G Lots	Lot# 8536300	Lot# 8673581	Lot# 8709155
Post HTOL Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTOL Electrical Test 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post HTOL Electrical Test -40°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

## 3.7 Early Life Failure Rate (ELFR), AEC-Q100 Test #B2

3.7.1 Inspection method: AEC-Q100-008.

3.7.2 Stress Conditions: 125°C, 3.65Vdc, 48 hours.

3.7.3 Test Description: The units are tested per the High Temp Operating Life requirements of Jedec 22-A108.

3.7.4 Sample size: 800 per lot

3.7.5 Accept/Reject Criteria: Accept on 0, reject on 1.

### 3.7.6 FM25V10-G Rev AB Early Life Failure Rate (ELFR) Test Results: (Family Data)

FM25V10-G Lots	Lot# 8536300	Lot# 8673581	Lot# 8709155
Post ELFR Electrical Test 25°C	0 fails/800 parts	0 fails/800 parts	0 fails/800 parts
Post ELFR Electrical Test 85°C	0 fails/800 parts	0 fails/800 parts	0 fails/800 parts

## 3.8 NVM Endurance, Data Retention and Operational Life (EDR), AEC-Q100 Test #B3

3.8.1 Inspection method: AEC-Q100-005

3.8.2 Stress Conditions: Program/Endurance: 1E5 Cycles at 3.65V  
High Temperature Storage: 125°C, 1000 hrs.

3.8.3 Purpose: Devices are first exercised through the Program/Endurance test, then HTSL.

3.8.4 Sample size: 77 per lot.

3.8.5 Accept/Reject Criteria: Accept on 0 failures, reject on 1 failure. A device is considered to fail if it is unable to electrically operate within the parameters detailed in the Device Specification for functionality and AC and DC characteristics at an operating temperature of 25°C and 85°C. Failed devices are removed from the test and submitted to Failure Analysis for failure mode and mechanism identification.

### 3.8.6 FM25V10-G Rev. AB NVM Endurance (EDR) Test Results: (Family Data)

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### NVM Endurance and HTSL

FM25V10-G Lot #	Lot# 8536300	Lot# 8673581	Lot# 8709155
Endurance Testing per AEC Q100-005 1E 5 Cycles, 3.65V	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Read Zeros	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Read Ones	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post RET Electrical Test 25°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts
Post RET Electrical Test 85°C	0 fails/77 parts	0 fails/77 parts	0 fails/77 parts

### 3.9 Wire Bond Shear Test (WBS), AEC-Q100 Test #C1

3.9.1 Inspection Method: AEC-Q100-001 Rev. C

3.9.2 Stress Conditions: 6.31g minimum for individual measurements and average 11.43grams minimum.

3.9.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices. Family data is acceptable for this test.

3.9.4 Sample size: 30 bonds from a minimum of 5 devices

3.9.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.9.6 Wire Bond Shear (WBS) Test Results: (Family Data)

	Run #0B0259, FM24V01-G Lingsen	Run #0B0260, FM25V01-G Lingsen	Family Data from UTL	Family Data from HANA
Sample Size	30 bonds, 5 pcs	30 bonds, 5 pcs	30 bonds, 5 pcs	30 bonds, 5 pcs
Minimum Value (gf)	18.12	19.00	9.68	15.58
Average Lot Value (gf)	20.27	21.57	13.43	22.27
CPK	3.60	3.55	1.34	1.92

### 3.10 Wire Bond Pull Test (WBP), AEC-Q100 Test #C2

3.10.1 Inspection Method: MIL-STD883 Method 2011

3.10.2 Stress Conditions: For gold bond wires <1mil diameter, wipe bond pull is performed with the hook over the ball bond, and not mid-wire method.

3.10.3 Purpose: This test establishes a procedure for determining the strength of the interface between the gold ball bond and a package bonding surface on either pre-encapsulated or post encapsulated devices. Family data is acceptable for this test.

3.10.4 Sample size: 30 bonds from a minimum of 5 devices

3.10.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure, and Cpk >1.33or Ppk>1.67

3.10.6 Wire Bond Shear (WBS) Test Results: (Family Data)

	Run #0B0259, FM24V01-G Lingsen	Run #0B0260, FM25V01-G Lingsen	Family Data from UTL	Family Data from HANA
Sample Size	30 bonds, 5 pcs	30 bonds, 5 pcs	30 bonds, 5 pcs	30 bonds, 5 pcs
Minimum Value (gf)	6.20	6.15	5.74	7.04
Average Lot Value (gf)	6.92	6.91	6.32	8.09
CPK	3.02	2.56	2.70	3.38

\*Lingsen preliminary 1mil gold bond wire data shown will be replaced with data 0.8mil gold bond wire.

### 3.11 Solderability (SD), AEC-Q100 Test #C3

3.11.1 Inspection method: JEDEC Method B102-C

3.11.2 Stress Conditions: 8 hour steam aging prior to solderability test

3.11.3 Purpose: The purpose of this test is to determine the solderability of device package terminal leads intended to be joined to another surface using solder. Family data is acceptable for this test.

3.11.4 Sample size: 15 samples from 1 lot.

3.11.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure.

3.11.6 Solderability (SD) Test Results: (Family Data)

	8-Lead SOIC Family Data from Lingsen	8-Lead SOIC Family Data from UTL	8-Lead SOIC Family Data from Hana
Sample Size	15	15	15
Pass/fail	15 passes/0 fails	15 passes/0 fails	15 passes/0 fails

### 3.12 Physical Dimensions (PD), AEC-Q100 Test #C4

3.12.1 Inspection method: JEDEC Method B100-A

3.12.2 Stress Conditions: N/A

3.12.3 Purpose: Package outline and leads measured for concurrence with the Device Specification package drawing. Measurements are made with micrometers to determine adherence to specifications (Jedec MS-012). Family data is acceptable for this test.

3.12.4 Sample size: 10 units per lot

3.12.5 Accept/Reject Criteria: Accept the lot on 0 failures, reject on 1 failure. Cpk > 1.3, ppk > 1.67

## 3.12.6 Family Data Physical Dimension (PD) Results:

HANA 8-lead Green SOIC (02-60-5120)	Lot# 94078052	Lot# 94725581	Lot# 95378251	Ppk
Sample Size	10	10	10	
A Overall Package Height Lot average Spec: 1.35-1.75mm	1.513	1.544	1.54	5.28
b Lead Width Lot average Spec: .33-.51 mm	0.453	0.447	0.438	3.46
D Overall Package Length Lot Average Spec:4.80-5.00mm	4.925	4.954	4.961	3.14
E Overall Package Width Lot Average Spec: 5.80-6.20mm	5.941	5.92	5.948	7.4

UTL Green 8-lead SOIC (02-60-5113)				
Sample Size	10	10	10	Ppk
A Overall Package Height Lot average Spec: 1.35-1.75mm	1.6	1.596	1.599	7.46
b Lead Width Lot average Spec: .33-.51 mm	0.431	0.435	0.448	2.34
D Overall Package Length Lot Average Spec:4.80-5.00mm	4.931	4.925	4.919	2.26
E Overall Package Width Lot Average Spec: 5.80-6.20mm	6.028	6.035	6.037	6.67

Lingsen 8-lead Green SOIC	Lot# 04537874	CPK
Sample Size	10	
A Overall Package Height Lot average Spec: 1.35-1.75mm	1.503	12.2
b Lead Width Lot average Spec: .33-.51 mm	.4264	2.9
D Overall Package Length Lot Average Spec:4.80-5.00mm	4.817	1.3
E Overall Package Width Lot Average Spec: 5.80-6.20mm	5.999	3.9

### 3.13 Electrostatic Discharge - Human Body Model (ESD-HBM) AEC-Q100 Test #E2

- 3.13.1 Test Method: AEC-Q100-002 Rev. D.
- 3.13.2 Stress Conditions: Human Body Model, 100pF discharge through a 1.5K-ohm resistor.
- 3.13.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Human Body Model as detailed in JEDEC A114-B (100pF discharged through 1.5K ohms). The devices are subjected to voltage ranging from 500V through 4500V for each group of three (3) devices.
- 3.13.4 Sample size: 3 parts per voltage group tested.
- 3.13.5 Accept/Reject Criteria: A device passed a voltage level if all devices in the sample group stressed at that voltage and below pass.

NOTE: A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.

#### 3.13.6 FM25V02-G Rev. AA ESD HBM Test Results:

ESD-HBM	FM25V02-G Lot# 94784181		ESD-HBM	FM24V02-G Lot# 94784181	
	25°C	85°C		25°C	85°C
500V	0 fails/3parts	0 fails/3parts	500V	0 fails/3parts	0 fails/3parts
1000V	0 fails/3parts	0 fails/3parts	1000V	0 fails/3parts	0 fails/3parts
1500V	3 fails/3parts	3 fails/3parts	1500V	0 fails/3parts	0 fails/3parts
2000V	2 fails/3parts	2 fails/3parts	2000V	0 fails/3parts	0 fails/3parts
2500V	0 fails/3parts	0 fails/3parts	2500V	0 fails/3parts	0 fails/3parts
3000V	0 fails/3parts	0 fails/3parts	3000V	0 fails/3parts	0 fails/3parts
3500V	0 fails/3parts	0 fails/3parts	3500V	0 fails/3parts	0 fails/3parts
4000V	1 fails/3parts	1 fails/3parts	4000V	2 fails/3parts	2 fails/3parts
4500V	2 fails/3parts	2 fails/3parts	4500V	2 fails/3parts	2 fails/3parts

- 3.13.7 Conclusion: Device categorized as Class H1C devices for HBM ESD sensitivity (>1000V to ≤2000V) per AEC Q100-002.

### 3.14 Electrostatic Discharge – Charged Device Model (CDM) AEC-Q100 Test #E3

- 3.14.1 Test Method: AEC-Q100-011 Rev. B
- 3.14.2 Stress Conditions: Transferring of electrostatic charge between bodies at different electrostatic potentials, with circuitry as described in section 2.1 of AEC-Q100-011 Rev. B, Direct Charge or Field Induced Charge.
- 3.14.3 Test Description: The purpose of the electrostatic discharge test is to classify the components as to their sensitivity to static electricity by using the Charged Device Model as detailed in AEC Q100-011. The devices are subjected to voltage ranges from 250V to 1250V.
- 3.14.4 Sample size: 3 parts per voltage group tested.
- 3.14.5 Accept/Reject Criteria: A device passes a voltage level if all devices in the sample group stressed at that voltage and below pass. A device is considered a failure if it is unable to operate electrically within the device parameters detailed in the Device Specification after ESD stress is applied.
- 3.14.6 Test Summary: FM25V02-G Rev. AA ESD CDM Results

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ESD-CDM	FM25V02-G Lot# 94784181			ESD-CDM	FM24V02-G Lot# 94784181	
	25°C	85°C			25°C	85°C
250V	0 fails/3parts	0 fails/3parts		250V	0 fails/3parts	0 fails/3parts
500V	0 fails/3parts	0 fails/3parts		500V	0 fails/3parts	0 fails/3parts
750V	0 fails/3parts	0 fails/3parts		750V	0 fails/3parts	0 fails/3parts
1000V	0 fails/3parts	0 fails/3parts		1000V	0 fails/3parts	0 fails/3parts
1250V	0 fails/3parts	0 fails/3parts		1250V	0 fails/3parts	0 fails/3parts

3.14.7 Conclusion: Devices categorized as Class C5 for ESD-CDM sensitivity (>1000V) per AEC Q100-011.

### 3.15 Latch-up Immunity (LU) AEC-Q100 Test #E4

3.15.1 Test Method: AEC-Q100-004

3.15.2 Stress Conditions: Latch-Up: Must pass - 100mA current injection, each input pin.  
Tested to -300mA current injection, each input pin.  
Vsupply Over-Voltage Test: 3.65 to 6.4V.

3.15.3 Test Description: The Latch-Up Immunity test assesses the devices susceptibility to latch-up at maximum operating temperatures (90°C). A negative current is applied to each package pin (pin to Vss then pin to Vcc). The current is incremented to -300mA, although AEC Q100-011 only requires -100mA. The device Icc current is measured after each current increment and compared to the maximum value as detailed in the Device Specification. During the Vsupply Over-Voltage Test, the voltage is increased from 3.65 to 6.4V .measuring Icc at each increment after removing the Voltage source.

3.15.4 Sample size: 6 parts from one lot.

3.15.5 Accept/Reject Criteria: Accept on 0 failures and reject on one failure.

3.15.6 FM25V02-G and FM24V02-G Rev. AA Latch-Up (LU) Test Results:

<u>Lot Number</u>	<u>Parts Tested</u>	<u>Test Result (90°C)</u>
94784181 (Both Devices)	6	0 fails up to $\pm 300$ mA

3.15.7 Conclusion: All devices performed to greater than -300mA in Latch up Immunity and passed the Vsupply Over-Voltage Test at 90°C.

### 3.16 Electrical Distributions (ED) AEC-Q100-009 Test #E5

3.16.1 Test Description: Selected parameters from the Characterization test program are tested and datalogged at 3 temperatures, 25C, 90C, and -45C. The data is stored in an excel spreadsheet that then has pivot tables created from it to generate Ppks.

3.16.2 Sample size: 20 parts from each of the 3 lots

3.16.3 Accept/Reject Criteria: Accept Ppk>1.67



Electrical Distribution – FM25V02-G	Ppks	Ppks	Ppks
Lots/Temperatures	Lot# 9482299	Lot# 9646447	Lot# 96750871
+25 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67
+90 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67
-45 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67

Electrical Distribution – FM24V02-G	Ppks	Ppks	Ppks
Lots/Temperatures	Lot# 96671901	Lot# 96750873	Lot# 97029652
+25 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67
+90 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67
-45 Degrees C	Average Ppk >1.67	Average Ppk >1.67	Average Ppk >1.67

3.15.4 Results: Pass – All average Ppks > 1.67 for all lots at all temperatures.

### 3.17 Electrically Induced Gate Leakage (GL) AEC-Q100 Test #E8

3.17.1 Inspection method: AEC-Q100-006 Rev. D.

3.17.2 Stress Conditions: 155°C,  $\pm$  20kVDC.

3.17.3 Test Description: This test is used to determine surface mount integrated circuit susceptibility to Electro-Thermally induced Parasitic Gate Leakage.

3.17.4 Sample size: 6 units from one lot.

3.17.5 Accept/Reject Criteria: Accept 0, Reject on 1.

3.17.6 FM25V02-G Gate Leakage (GL) Test Results:

<u>Lot Number</u>	<u>+20kVDC</u>	<u>-20kVDC</u>
04838552	0fails/3parts	0fails/3parts

## 4 CONCLUSIONS

4.1 Based on this successful completion of the FRAM Product Qualification testing, the FM25V01-G, FM25V02-G, FM24V01-G, and FM24V02-G, Rev. AB, meet the requirements of AEC-Q100 Rev. G and are now AEC-Q100 Grade 3 qualified products.

## 5 REPORTS AND DATA

5.1 Table I: Overall AEC-Q100 Qualification Test Summary

TEST	AEC Q100 Test #	ABR	DURATION	Lot# 8536300	Lot# 04838552	Lot# 04505521
Pre-Conditioning	A1	PC		0fails/240parts	0fails/240parts	0fails/240parts
(Preconditioned) Highly Accelerated Stress Test	A2	HAST	96-Hr HAST			
			25°C	0/77	0/77	0/77
			85°C	0/77	0/77	0/77
(Preconditioned) Autoclave	A3	AC	96-Hr AC			
			25°C	0/77	0/77	0/77
			85°C	0/77	0/77	0/77
(Preconditioned) Temperature Cycle	A4	TC	500 Cycles			
			25°C	0/77	0/77	0/77
			85°C	0/77	0/77	0/77
		WP	g- min			
High Temperature Storage Life 150°C	A5	HTSL	500 hrs	Lot# 8701955		
			25°C	0/45		
			85°C	0/45		
High Temperature Operating Life	B1	HTOL		Lot# 8536300	Lot# 8673581	Lot# 8709155
			25°C	0/77	0/77	0/77
			85°C	0/77	0/77	0/77
			-40°C	0/77	0/77	0/77
Early Life Failure Rate	B2	ELFR	48 hours			
			25°C	0/800	0/800	0/800
			85°C	0/800	0/800	0/800
NVM Endurance Data Retention 125C 1000hrs	B3	EDR	Endurance	0/77	0/77	0/77
			Read Zeros	0/77	0/77	0/77
			Read Ones	0/77	0/77	0/77
			25°C	0/77	0/77	0/77
			85°C	0/77	0/77	0/77
Wire Bond Shear Test ( 8-lead Green SOIC)	WBS	C1	Min	Lingsen 33.53	UTL 9.68	HANA 15.58
			Avg.	33.03	13.43	22.27
			Cpk	1.99	1.34	1.92
Bond Wire Pull Test ( 8-lead Green SOIC)	BPS	C2	Min	Lingsen 8.40	UTL 5.74	HANA 7.04
			Avg.	10.18	6.32	8.09
			Cpk	1.93	2.70	3.38
Solderability ( Family data)	SD	C3	>95% Lead Coverage	Lingsen 0 fails/15 parts	UTL 0 fails/15 parts	Hana 0 fails/15 parts

Physical Dimension ( 8-lead Green SOIC)	PD	C4	Ppk>1.67 Height Lead Length Width	Lot# 94078052 1.513mm 0.453mm 4.925mm 5.941mm	Lot# 94725581 1.544mm 0.447mm 4.954mm 5.92mm	Lot# 95378251 1.54mm 0.438mm 4.961mm 5.948mm
Pre & Post Stress	Test	E1		All units tested	All units tested	All units tested
<b>TEST</b>	<b>AEC</b>	<b>ABR</b>	<b>Voltage/Current</b>		<b>FM25V02-G</b> <b>Lot# 94784181</b>	<b>FM24V02-G</b> <b>Lot# 94784181</b>
	<b>Q100</b>					
	<b>Test #</b>					
Electrostatic Discharge- Human Body Model	ESD- HBM	E2	500V 1000V 1500V 2000V 2500V 3000V 3500V 4000V 4500V		0fails/3parts 0fails/3parts 3fails/3parts 2fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 1fails/3parts 2fails/3parts	0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 2fails/3parts 2fails/3parts
Electro Static Discharge Charged Device Model	ESD- CDM	E3	250V 500V 750V 1000V 1250V		0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts	0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts 0fails/3parts
Latch Up Immunity	LU	E4	± 300 mA		0fails/6parts	0fails/6parts
Electrical Distributions – <b>FM25V02-G</b>	ED	E5	Ppk > 1.67	Lot #9482299 Pass @ 25C, 90C & -45C	Lot #9646447 Pass @ 25C, 90C & -45C	Lot #96750871 Pass @ 25C, 90C & -45C
Electrical Distributions – <b>FM24V02-G</b>	ED	E5	Ppk > 1.67	Lot #96671901 Pass @ 25C, 90C & -45C	Lot #96750873 Pass @ 25C, 90C & -45C	Lot #97029652 Pass @ 25C, 90C & -45C
Gate Leakage	GL	E8	155C, + 20kV -20kV		0/3 0/3	



## Document History Page

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Rev.	ECN No.	Orig. of Change	Description of Change
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*A	3954178	BECK	Added Reliability Failure Rate Summary

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