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Cypress Semiconductor
Product Qualification Report

QTP# 112604 VERSION*A
March 2015

72 Meg / 36Meg QDR II+ Extreme Synchronous SRAM Family 65nm (LL6XP-18R) Technology, UMC Fab 12A	
CY7C1562XV18 CY7C1564XV18	72-Mbit QDR(R) II+ Xtreme SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1563XV18 CY7C1565XV18	72-Mbit QDR(R) II+ Xtreme SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1568XV18 CY7C1570XV18	72-Mbit DDR II+ Xtreme SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C2562XV18 CY7C2564XV18	72-Mbit QDR(R) II+ Xtreme SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) With ODT
CY7C2563XV18 CY7C2565XV18	72-Mbit QDR(R) II+ Xtreme SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency) With ODT
CY7C2568XV18 CY7C2570XV18	72-Mbit DDR II+ Xtreme SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) With ODT
CY7C1262XV18 CY7C1264XV18	36-Mbit QDR(R) II+ Xtreme SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1263XV18 CY7C1265XV18	36-Mbit QDR(R) II+ Xtreme SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1268XV18 CY7C1270XV18	36-Mbit DDR II+ Xtreme SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C2262XV18 CY7C2264XV18	36-Mbit QDR(R) II+ Xtreme SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) With ODT
CY7C2263XV18 CY7C2265XV18	36-Mbit QDR(R) II+ Xtreme SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency) With ODT
CY7C2268XV18 CY7C2270XV18	36-Mbit DDR II+ Xtreme SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) With ODT

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose	Date Comp
091706		Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device CY7C1553K Base Die Product Family	Aug 2009
093202		Qualification of UMC 65nm Process Improvement	Nov 2009
112604		Qualification of UMC LL65XP-18R 72M/36M QDR2+ Extreme 7C2565QX Product	Feb 2012

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose:	Qualify UMC LL65XP-18R 72M/36M QDR2+ Extreme 7C2565QX Base Die
Marketing Part #:	CY7C15xxXV18, CY7C25xxXV18, CY7C12xxXV18, CY7C22xxXV18
Device Description:	1.8V Commercial and Industrial available in 165-Ball FBGA (13 x 15 x 1.4 mm)
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division
What ID markings on Die:	7C1553QXO

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65P-18R			
Number of Metal Layers:	5+RDL	Metal Composition:	Metal 1: Cu 0.18um Metal 2: Cu 0.22um Metal 3: Cu 0.22um Metal 4: Cu 0.36um Metal 5: Cu 1.25um Metal 6 (RDL): Al 1.2um
Passivation Type and Materials:			0.4um Oxide / 0.5um Nitride
Number of Transistors in Device			~600M
Number of Logic Gates in Device			~300M
Generic Process Technology/Design Rule (µ-drawn):			CMOS, 65nm
Gate Oxide Material/Thickness (MOS):			19.5A MOS
Name/Location of Die Fab (prime) Facility:			UMC Fab 12
Die Fab Line ID/Wafer Process ID:			LL65XP-18R

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-Ball FBGA	**CML Autoline**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BW165R
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	CK7000-LA
Mold Compound Flammability Rating:	UL94, V-0
Oxygen Rating Index:	N/A
Substrate Material:	BT resin
Lead Finish, Composition / Thickness:	SnAgCu
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Sawing 100%
Die Attach Supplier:	Henkel
Die Attach Material:	QMI-506
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-55180
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	13.7
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-09031
Name/Location of Assembly (prime) facility:	CML-RA

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-RA

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125C Dynamic Operating Condition, 125C, 1.95V Vcc Max	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125C/150C Dynamic Operating Condition, 125C, 1.95V Vcc Max	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at LFR 80hrs, 500hrs & 1000hrs	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V/1.95V, 150C	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.25V, -30C	P
High Accelerated Saturation Test (HAST)	130C, 2.25V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, **260C**+0, -5C	P
Temperature Humidity Bias Test (THB)	85C, 2.25V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, **260C**+0, -5C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30□C/60%RH+3IR-Reflow, **260C**+0, -5C	P
Pressure Cooker	121C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30□C/60%RH+3IR-Reflow**, 260C**+0, -5C	P
Precondition	JESD22 Moisture Sensitivity	P
High Temperature Storage	150C ± 5C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V, JESD22-A114E	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101C	P
Electrostatic Discharge Machine Model (ESD-MM)	200V, JESD22-A115-A	P
Soft Error (Alpha Particle)	JESD89A	P
Soft Error (Neutron/Proton)	JESD89A	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020	P
Static Latchup	JESD78B , 125C, ± 140mA	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	9,981 Devices	1	N/A	N/A	100 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate (150C)	89,000 DHRs	0	0.7	170	21 FIT
High Temperature Operating Life[1,2] Long Term Failure Rate (125C)	508,816 DHRs	0	0.7	55	

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	500	178	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA							
CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	
STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE, 3-TEPM, 3-VOLTAGE, @ 85C, Vcc Nom							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
STRESS: X-SECTION/STEM XY AUDIT							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		

Reliability Test Data

QTP #: 093202

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	COMP	8	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	1000	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	96	596	0	
CY7C15631KV18 (7C1553K)	8910015	610921676	TAIWN-G	96	711	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	96	1795	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	168	190	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	500	184	0	

Reliability Test Data

QTP #: 112604

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML_RA	COMP	15	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML_RA	COMP	6	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML_RA	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML_RA	COMP	5	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 1.95V Vcc Max							
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML-RA	96	4164	1	3-bit failure, CAR# 201209003
CY7C2565XV18 (7C2565QX)	8142002	611201854	CML-RA	96	5817	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 1.95V Vcc Max							
CY7C2565XV18 (7C2565QX)	8127016	611147742	CML-RA	168	172	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 1.95, Vcc Max							
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML_RA	336	77	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 2.85V, +/-140mA							
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML_RA	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML_RA	500	77	0	
CY7C1570XV18 (7C1570QX)	8127016	611144584	CML_RA	1000	77	0	

Document History Page

Document Title: QTP 112604: 72 MEG / 36MEG QDR EXTREME SYNCHRONOUS SRAM FAMILY, 65NM (LL6XP-18R) TECHNOLOGY, UMC FAB 12A
Document Number: 001-76403

Rev.	ECN No.	Orig. of Change	Description of Change
**	3538076	NSR	Initial spec release.
*A	4678942	HSTO	Align qualification report based on the new template in the front page Updated Reliability Test Performed Table: • Deleted reference Cypress spec for ESD-CDM, ESD-MM, Soft Error, Current Density, Acoustic Microscopy and Static Latchup. • Replaced it with reference industry standards

Distribution: WEB

Posting: None