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Cypress Semiconductor
Product Qualification Report

QTP# 111503 VERSION*C
December 2014

4 Meg MoBL SRAM Family R95LD-3R, FAB 4	
CY621472ELL MOBL® CY621472E18LL MOBL® CY621472E30LL MOBL®	4-Mbit (256K x 16) Static RAM with 2 Chip Enable

FOR ANY QUESTIONS ON THIS REPORT, PLEAE CONTACT
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PRODUCT QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date
054302	R95LD-3R, Fab 4 and New Device CY7C62xxx (4Meg) MoBL Product Family	Dec 05
111503	Qualification of 4M 2 CE NSO Parts, R95LD-3R Technology in CMI	Nov 11

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify 4M 2 CE NSO Parts MoBL product family in qualified technology R95LD-3R, Fab 4	
Marketing Part #:	CY621472Exxx
Device Description:	1.8V, 3V, 5V 4Meg 2 CE NSO MoBL SRAM
Cypress Division:	Cypress Semiconductor Corporation –Memory Products Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 100Å Ti / 3200Å Al / 300Å TiW Metal 2: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Thickness:			1000Å Oxide TEOS / 9000Å Nitride
Generic Process Technology/Design Rule (µ-drawn):			CMOS, Double Metal, 0.09µm
Gate Oxide Material/Thickness (MOS):			28Å
Name/Location of Die Fab (prime) Facility:			Cypress Semiconductor -- Bloomington, MN
Die Fab Line ID/Wafer Process ID:			Fab4/R95LD-3RP

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
44-Lead TSOP II	CML-R

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZW44
Package Outline, Type, or Name:	44-Pin Thin Small Outlined Packages (Type II)
Mold Compound Name/Manufacturer:	Hitachi CEL9200
Mold Compound Flammability Rating:	V-O per UL94
Mold Compound Alpha Emission Rate:	0.0015c/cm2-h
Oxygen Rating Index:	N/A
Substrate Material:	Copper
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	100% Saw Through
Die Attach Supplier:	Dexter
Die Attach Material:	QMI-509
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-68155
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au. 0.9mil
Thermal Resistance Theta JA °C/W:	37° C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	Cypress Philppines (CML-R)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CML-R), KYEC, Chipmos

Note: Please contact a Cypress Representative for other package availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	JESD22-A108: Dynamic Operating Condition, Vcc Max = 1.85V, 125°C	P
High Temperature Operating Life Latent Failure Rate	JESD22-A108: Dynamic Operating Condition, Vcc Max = 1.85V, 150°C	P
Long Life Verification	JESD22-A108: Dynamic Operating Condition, Vcc = 1.85V, 150°C	P
High Temperature Steady State Life	JESD22-A108: Static Operating Condition, Vcc Max = 1.75V, 125°C	P
Low Temperature Operating Life	JESD22-A108: Dynamic Operating Condition, Vcc = 2.0V, -30°C	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, **260°C**+0, -5°C	P
Pressure Cooker	JESD22-A102:121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow**, 260°C**+0, -5°C	P
High Temperature Storage	JESD22-A103: 150°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020	P
Dynamic Latchup	JESD78	P
Static Latchup	125C, ± 140/200/300mA JESD78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	7,338 Devices	1	N/A	N/A	136 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	600,000 DHRs	1	0.7	170	10 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data
*QTP #:*054302

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ACOUSTIC-MSL3							
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	COMP	15	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	COMP	15	0	
CY62147EV30LL (7C62147F)	4447261	*610506302N*	CML-R	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY62147EV30LL (7C62147F)	4514985	*610527600*	CML-R	COMP	10	0	
CY62136EV30LL (7C62136F)	4516742	*610537839*	CML-R	COMP	10	0	
CY62147EV30LL (7C62147F)	4516646	*610527599*	CML-R	COMP	10	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 1.85V, Vcc Max (Core)							
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	96	679	0	
CY62147EV30LL (7C62147F)	4527847	*610558767*	CML-R	96	4031	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	96	1711	0	
CY62147EV30LL (7C62147F)	4447261	*610506302N*	CML-R	96	917	1	Single Bit (Non-visual)
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 1.85V, Vcc Max (Core)							
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	80	400	0	
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	500	400	1	Blocked contact at Poly
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	80	400	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	500	400	0	
CY62147EV30LL (7C62147F)	4447261	*610506302N*	CML-R	80	400	0	
CY62147EV30LL (7C62147F)	4447261	*610506302N*	CML-R	500	400	0	
STRESS: LONG LIFE VERIFICATION, 150C, 1.85V, Vcc Max (Core)							
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	1000	393	0	
STRESS: HIGH TEMPERATURE STEADY STATE LIFE, 125C, 1.75V, Vcc Max							
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	168	76	0	
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	336	75	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.0V, Vcc							
CY62147EV30LL (7C62147F)	4447261	*610506302N*	CML-R	500	45	0	
STRESS: HIGH TEMPERATURE STORAGE							
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	500	45	0	
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	1000	45	0	

Reliability Test Data
*QTP #:*054302

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62147EV30LL (7C62147F)	4527847	*610548767*	CML-R	COMP	9	0	
CY62148EV30LL (7C62148F)	4527847	*610548491*	TAIWN-G	COMP	9	0	
CY62148EV30LL (7C62148F)	4527847	*610550592*	CML-RA	COMP	9	0	
CY62147EV30LL (7C62147F)	4516646	*610527599*	CML-R	COMP	9	0	
CY62147EV30LL (7C62147F)	4514985	*610527600*	CML-R	COMP	9	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY62147EV30LL (7C62147F)	4527847	*610548767*	CML-R	COMP	9	0	
CY62148EV30LL (7C62148F)	4527847	*610548491*	TAIWN-G	COMP	9	0	
CY62148EV30LL (7C62148F)	4527847	*610551587*	CML-R	COMP	9	0	
CY62148EV30LL (7C62148F)	4527847	*610550592*	CML-RA	COMP	9	0	
CY62147EV30LL (7C62147F)	4516646	*610527599*	CML-R	COMP	9	0	
CY62147EV30LL (7C62147F)	4514985	*610527600*	CML-R	COMP	9	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62147EV30LL (7C62147F)	4527847	*610548767*	CML-R	COMP	3	0	
CY62148EV30LL (7C62148F)	4527847	*610548491*	TAIWN-G	COMP	3	0	
CY62148EV30LL (7C62148F)	4527847	*610551587*	CML-R	COMP	3	0	
CY62148EV30LL (7C62148F)	4527847	*610550592*	CML-RA	COMP	3	0	
CY62147EV30LL (7C62147F)	4516646	*610527599*	CML-R	COMP	3	0	
CY62147EV30LL (7C62147F)	4514985	*610527600*	CML-R	COMP	3	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY62137EV30LL (7C62137F)	4516742	*610539321*	CML-R	128	45	0	
CY62137EV30LL (7C62137F)	4516742	*610539321*	CML-R	256	45	0	
CY62137EV30LL (7C62137F)	4516742	*610539321*	CML-R	128	54	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 5.5V, PRE COND 192 HR 30C/60%RH, MSL3							
CY62147EV30LL (7C62147F)	4527847	*610558767*	CML-R	128	45	0	
CY62147EV30LL (7C62147F)	4527847	*610558767*	CML-R	264	45	0	

Reliability Test Data
*QTP #:*054302

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: DYNAMIC LATCH-UP TESTING, 9.0V							
CY62147EV30LL (7C62147F)	4438656	*610461414*	TAIWN-G	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-300mA							
CY62147EV30LL (7C62147F)	4514985	*610527600*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, +/-300mA							
CY62147EV30LL (7C62147F)	4527847	*610548767*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 9.5V, +/-300mA							
CY62147EV30LL (7C62147F)	4516646	*610527599*	CML-R	COMP	3	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.5V, +/-200mA							
CY62148EV30LL (7C62148F)	4527847	*610548491*	TAIWN-G	COMP	3	0	
CY62148EV30LL (7C62148F)	4527847	*610551587*	CML-R	COMP	3	0	
CY62148EV30LL (7C62148F)	4527847	*610550592*	CML-RA	COMP	3	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY62147EV30LL (7C62147F)	4516742	*610537714*	CML-R	168	50	0	
CY62147EV30LL (7C62147F)	4516742	*610537714*	CML-R	288	50	0	
CY62147EV30LL (7C62147F)	4516646	*610537739*	CML-R	168	50	0	
CY62147EV30LL (7C62147F)	4516646	*610537739*	CML-R	288	50	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	168	50	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY62147EV30LL (7C62147F)	4438656	*610461414*	CML-RA	300	42	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	300	49	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	500	48	0	
CY62147EV30LL (7C62147F)	4519690	*610533058*	CML-RA	1000	46	0	
CY62147EV30LL (7C62147F)	4447261	*610506302N*	CML-R	300	45	0	
CY62147EV30LL (7C62147F)	4447261	*610506302N*	CML-R	500	44	0	
CY62147EV30LL (7C62147F)	4447261	*610506302N*	CML-R	1000	44	0	

Reliability Test Data
*QTP #:*111503

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY621472EV30LL (7C621473F)	4112687	*611137280*	CML-R	COMP	8	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.6V, +/-140mA							
CY621472EV30LL (7C621473F)	4112687	*611137280*	CML-R	COMP	6	0	
STRESS: CLASS YIELD							
CY621472EV30LL (7C621473F)	4112687	*611137280*	CML-R	COMP	COMPARABLE		
STRESS: E-TEST							
CY621472EV30LL (7C621473F)	4112687	*611137280*	CML-R	COMP	COMPARABLE		
STRESS: SORT YIELD							
CY621472EV30LL (7C621473F)	4112687	*611137280*	CML-R	COMP	COMPARABLE		

Document History Page

Document Title:QTP 111503: 4 MEG MOBL SRAM FAMILY (2 CE NSO PARTS), R95LD-3R TECHNOLOGY IN CMI
Document Number: 001-73951

Rev.	ECN No.	Orig. of Change	Description of Change
**	3432406	NSR	New Spec Release
*A	3809205	NSR	Removed the reference Cypress specs in reliability tests performed table and replace with reference Industry standards. Added **'4'** MEG in the spec title. Removed Assembly process flow Cypress spec11-20047.
*B	4194550	HSTO	Added KYEC & Chipmos Test Location in "ELECTRICAL TEST" table at page 4.
*C	4596444	HSTO	Align qualification report based on the new template in the front page

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