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Cypress Semiconductor
Product Qualification Report

QTP# 103405 VERSION*C
January, 2015

144 Meg QDR/DDR Synchronous SRAM Family 65nm (LL65P-18R) Technology, UMC Fab 12A	
CY7C1612KV18	144-Mbit QDR II SRAM 2-Word Burst Architecture
CY7C1613KV18	144-Mbit QDR II SRAM 4-Word Burst Architecture
CY7C1614KV18	144-Mbit QDR® II SRAM 2-Word Burst Architecture
CY7C1615KV18	144-Mbit QDR® II SRAM 4-Word Burst Architecture
CY7C1618KV18	144-Mbit DDR® II SRAM 2-Word Burst Architecture
CY7C1620KV18	144-Mbit DDR® II SRAM 2-Word Burst Architecture
CY7C1623KV18	144-Mbit DDR®-SIO SRAM 2-Word Burst Architecture
CY7C1625KV18	144-Mbit QDR® II SRAM 2-Word Burst Architecture
CY7C1626KV18	144-Mbit QDR® II SRAM 4-Word Burst Architecture
CY7C1643KV18	144-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1645KV18	144-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1648KV18	144-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1650KV18	144-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1663KV18	144-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1665KV18	144-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1668KV18	144-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1670KV18	144-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C2644KV18	144-Mbit QDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency) with ODT
CY7C2663KV18	144-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2665KV18	144-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2668KV18	144-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2670KV18	144-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) with ODT
CY7C2642KV18	144-Mbit QDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycles Read Latency) with ODT

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT

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QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date Comp
091706	Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device CY7C1553K Base Die 72M QDR Product Family	Aug 2009
093202	Qualification of UMC 65nm Process Improvement	Nov 2009
103405	LL65 144M QDR Product Family Qualification	Dec 2010

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose:	Qualify LL65 144M QDR Product Family at UMC Fab 12A	
Marketing Part #:	CY7C1612KV18, etc.	
Device Description:	1.8V Commercial and Industrial available in 165-Ball FBGA (15 x 17 x 1.4 mm)	
Cypress Division:	Cypress Semiconductor Corporation –Memory & Image Division	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. K
What ID markings on Die:	7C1653K	

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65P-18R			
Number of Metal Layers:	5+RDL	Metal Composition:	Metal 1: Cu 0.18um Metal 2: Cu 0.22um Metal 3: Cu 0.22um Metal 4: Cu 0.36um Metal 5: Cu 1.25um Metal 6 (RDL): Al 1.2um
Passivation Type and Materials:			0.4um Oxide / 0.5um Nitride
Free Phosphorus contents in top glass layer(%):			0 %
Number of Transistors in Device			~600M
Number of Logic Gates in Device			~300M
Generic Process Technology/Design Rule (µ-drawn):			CMOS, 65nm
Gate Oxide Material/Thickness (MOS):			19.5A
Name/Location of Die Fab (prime) Facility:			UMC Fab 12
Die Fab Line ID/Wafer Process ID:			L65LL

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-Ball FBGA	**CML Autoline**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	GR9810/Hysol
Mold Compound Flammability Rating:	UL94, V-0
Substrate Material:	SUBBBW165RF/ SUBBBW165RG
Lead Finish, Composition / Thickness:	SAC405
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Saw
Die Attach Supplier:	Henkel
Die Attach Material:	QMI-506
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-57409, 001-57411
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	12.55 ^{0}C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	11-21099
Name/Location of Assembly (prime) facility:	CML-Philippines

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-RA

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C /150°C JESD22-A108	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at LFR 80hrs, 500hrs & 1000hrs	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V, 150°C Static Operating Condition, Vcc Max= 2.05V, 125°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.25V, -30°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 85%RH, 2.25V Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C +0, -5°C	P
Temperature Humidity Bias Test (THB)	JESD22-A101: 85°C, 85%RH, 2.25V Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C +0, -5°C	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C MIL-STD-883, Method 1010, Condition B, -55°C to 125°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C +0, -5°C	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C +0, -5°C	P
High Temperature Storage	JESD22-A103: 150°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101	P
Electrostatic Discharge Machine Model (ESD-MM)	200V, JESD22-A115	P
Soft Error (Alpha Particle)	JESD89	P
Soft Error (Neutron/Proton)	JESD89	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C +0, -5°C	P
Dynamic Latch up	JESD78	P
Static Latch up	125C, ± 140mA JESD78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	3,033 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate (150°C)	89,000 DHRs	0	0.7	170	15 FIT
High Temperature Operating Life[1,2] Long Term Failure Rate (125°C)	805,008 DHRs	0	0.7	55	

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	500	178	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA							
CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	
STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE, 3-TEPM, 3-VOLTAGE, @ 85C, Vcc Nom							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
STRESS: X-SECTION/STEM XY AUDIT							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		

Reliability Test Data

QTP #: 093202

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	COMP	8	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	1000	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	96	596	0	
CY7C15631KV18 (7C1553K)	8910015	610921676	TAIWN-G	96	711	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	96	1795	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	168	190	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	500	184	0	

Reliability Test Data

QTP #: 103405

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	COMP	15	0	
CY7C1612K (7C1612K)	8845001	611032555	CML-RA	COMP	15	0	
CY7C1612K (7C1612K)	8845001	611032554	CML-RA	COMP	15	0	
CY7C1612K (7C1612K)	8908003	611024882	CML-RA	COMP	230	0	
CY7C1612K (7C1612K)	8845001	611024890	CML-RA	COMP	15	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C16539K (7C16539K)	8845004	610933466	G-Taiwan	COMP	8	0	
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C16539K (7C16539K)	8845004	610933466	G-Taiwan	COMP	9	0	
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C16539K (7C16539K)	8845004	610933466	G-Taiwan	COMP	5	0	
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 2.05V), PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	264	76	0	
CY7C1612K (7C1612K)	8908003	611024882	CML-RA	264	72	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.05V, REG ON							
CY7C16538K (7C16538K)	8937000	610945141	G-Taiwan	96	48	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C16538K (7C16538K)	8937000	610944083	G-Taiwan	96	1809	0	
CY7C1614K (7C1614K)	8927001	610946060	G-Taiwan	96	1224	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C16538K (7C16538K)	8937000	610944083	G-Taiwan	168	178	0	
CY7C16538K (7C16538K)	8937000	610944083	G-Taiwan	1000	178	0	
CY7C1614K (7C1614K)	8927001	610946060	G-Taiwan	168	178	0	
CY7C1614K (7C1614K)	8927001	610946060	G-Taiwan	1000	178	0	

Reliability Test Data

QTP #: 103405

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP STORAGE 150C							
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	500	76	0	
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	1000	74	0	
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	1500	66	0	
CY7C1612K (7C1612K)	8908003	611024882	CML-RA	500	77	0	
CY7C1612K (7C1612K)	8908003	611024882	CML-RA	1000	76	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.05V, Vcc Max							
CY7C16539K (7C16539K)	8845004	610933941	CML-RA	168	77	0	
CY7C16539K (7C16539K)	8845004	610933941	CML-RA	336	77	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	168	75	0	
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	288	72	0	
CY7C1612K (7C1612K)	8845001	611032555	CML-RA	168	73	0	
CY7C1612K (7C1612K)	8845001	611032555	CML-RA	288	73	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C16538K (7C16538K)	8937000	610944083	G-Taiwan	COMP	10	0	
CY7C1614K (7C1614K)	8927001	610946060	G-Taiwan	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-180mA							
CY7C16539K (7C16539K)	8845004	610933466	TAIWN-G	COMP	9	0	
CY7C1612K (7C1612K)	8845001	611032553	CML-RA	COMP	9	0	
STRESS: TC COND. B -55C TO 125C, PRE COND192 HRS 30C/60%RH, MSL3							
CY7C1614KV (7C1614K)	8945028	611036123	CML-RA	500	74	0	
CY7C1614KV (7C1614K)	8945028	611036123	CML-RA	1000	74	0	
CY7C1614KV (7C1614K)	8945028	611036123	CML-RA	1300	74	0	
CY7C1618KV (7C1618K)	8945028	611036125	CML-RA	500	76	0	
CY7C1618KV (7C1618K)	8945028	611036125	CML-RA	1000	75	0	
CY7C1618KV (7C1618K)	8945028	611036125	CML-RA	1300	75	0	
CY7C1613KV (7C1613K)	8015005	611041460	CML-RA	500	77	0	
CY7C1613KV (7C1613K)	8015005	611041460	CML-RA	1000	77	0	
CY7C1613KV (7C1613K)	8015005	611041460	CML-RA	1300	77	0	

Document History Page

Document Title: QTP 103405: LL65 144 MEG QDR/DDR SYNCHRONOUS PRODUCT QUALIFICATION REPORT
Document Number: 001-66060

Rev.	ECN No.	Orig. of Change	Description of Change
**	3112570	NSR	Initial spec release.
*A	4020395	NSR	Removed VERSION 1.0 in the title page. Added device CY7C2642KV18 in page 1. Removed ® and ™ in the device description in page 1. Fixed page alignment. Removed obsolete specs 001-57677 and 001-57674. Removed reference Cypress specs in Reliability Tests performed table and replaced with/retain the reference Industry standards.
*B	4231183	JYF	Updated title of QA Engineering Director to Reliability Director in QTP title page; Complete re-write of Reliability Tests Performed table for template alignment.
*C	4614526	JYF	Sunset review: Updated QTP title page for template alignment.

Distribution: WEB

Posting: None