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Cypress Semiconductor
Product Qualification Report

QTP# 100901 VERSION*F
December, 2014

18 Meg QDR/DDR Synchronous SRAM Family 65nm (LL65P-18R) Technology, UMC Fab 12A	
CY7C1311KV18	**18-Mbit QDR® II SRAM 4-Word Burst x8 Architecture**
CY7C1312KV18	**18-Mbit QDR® II SRAM 2-Word Burst x18 Architecture**
CY7C1313KV18	**18-Mbit QDR® II SRAM 4-Word Burst x18 Architecture**
CY7C1314KV18	**18-Mbit QDR® II SRAM 2-Word Burst x36 Architecture**
CY7C1315KV18	**18-Mbit QDR® II SRAM 4-Word Burst x36 Architecture**
CY7C1318KV18	**18-Mbit DDR® II SRAM 2-Word Burst x18 Architecture**
CY7C1319KV18	**18-Mbit DDR® II SRAM 4-Word Burst x18 Architecture**
CY7C1320KV18	**18-Mbit DDR® II SRAM 2-Word Burst x36 Architecture**
CY7C1321KV18	**18-Mbit DDR® II SRAM 4-Word Burst x36 Architecture**
CY7C1393KV18	**18-Mbit DDR®-II SIO SRAM 2-Word Burst x18 Architecture**
CY7C1911KV18	**18-Mbit QDR® II SRAM 4-Word Burst x9 Architecture**
CY7C1143KV18	**18-Mbit QDR®-II+ SRAM 4-Word Burst x18 Architecture (2.0 Cycle Read Latency)**
CY7C1145KV18	**18-Mbit QDR®-II+ SRAM 4-Word Burst x36 Architecture (2.0 Cycle Read Latency)**
CY7C1148KV18	**18-Mbit DDR®-II+ SRAM 2-Word Burst x18 Architecture (2.0 Cycle Read Latency)**
CY7C1150KV18	**18-Mbit DDR®-II+ SRAM 2-Word Burst x36 Architecture (2.0 Cycle Read Latency)**
CY7C1163KV18	**18-Mbit QDR®-II+ SRAM 4-Word Burst x18 Architecture (2.5 Cycle Read Latency)**
CY7C1165KV18	**18-Mbit QDR®-II+ SRAM 4-Word Burst x36 Architecture (2.5 Cycle Read Latency)**
CY7C1168KV18	**18-Mbit DDR®-II+ SRAM 2-Word Burst x18 Architecture (2.5 Cycle Read Latency)**
CY7C1170KV18	**18-Mbit DDR®-II+ SRAM 2-Word Burst x36 Architecture (2.5 Cycle Read Latency)**
CY7C2163KV18	**18-Mbit QDR®-II+ SRAM 4-Word Burst x18 Architecture (2.5 Cycle Read Latency) with ODT**
CY7C2165KV18	**18-Mbit QDR®-II+ SRAM 4-Word Burst x36 Architecture (2.5 Cycle Read Latency) with ODT**
CY7C2168KV18	**18-Mbit DDR®-II+ SRAM 2-Word Burst x18 Architecture (2.5 Cycle Read Latency) with ODT**
CY7C2170KV18	**18-Mbit DDR®-II+ SRAM 2-Word Burst x36 Architecture (2.5 Cycle Read Latency) with ODT**
CY7C1392KV18	**18-Mbit 1.8V DDRII SIO SRAM Two-Word Burst x8 Architecture**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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QUALIFICATION HISTORY

QTP Number	Description of Qualification Purpose	Date Comp
091706	Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device 72M QDR CY7C1553K Base Die Product Family	Aug 2009
093202	Qualification of UMC 65nm Process Improvement	Nov 2009
100901	LL65 18M QDR 7C1173K Base Die Product Family Qualification	Nov 2010

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose:	Qualify 18M QDR 7C1173K Base Die Product Family, LL65P-18R Technology at UMC Fab 12A 65nm	
Marketing Part #:	CY7C1313KV18, etc.	
Device Description:	1.8V Commercial and Industrial available in 165-Ball FBGA (13 x 15 x 1.4 mm)	
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. A/B
What ID markings on Die:	7C1173K	

TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65P-18R			
Number of Metal Layers:	5+RDL	Metal Composition:	Metal 1: Cu 0.18um Metal 2: Cu 0.22um Metal 3: Cu 0.22um Metal 4: Cu 0.36um Metal 5: Cu 1.25um Metal 6 (RDL): Al 1.2um
Passivation Type and Materials:			0.4um Oxide / 0.5um Nitride
Free Phosphorus contents in top glass layer(%):			0 %
Number of Transistors in Device			~600M
Number of Logic Gates in Device			~300M
Generic Process Technology/Design Rule (µ-drawn):			CMOS, 65nm
Gate Oxide Material/Thickness (MOS):			19.5A
Name/Location of Die Fab (prime) Facility:			UMC Fab 12
Die Fab Line ID/Wafer Process ID:			L65LL

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
165-Ball FBGA	**CML Autoline**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	CK7000 / Plascon
Mold Compound Flammability Rating:	UL94, V-0
Oxygen Rating Index:	45%
Substrate Material:	BT resin
Lead Finish, Composition / Thickness:	Sn63Pb37
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Saw
Die Attach Supplier:	Hysol
Die Attach Material:	QMI 506
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-60847, 001-60848, 001-60849
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	13.7 °C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-09031
Name/Location of Assembly (prime) facility:	CML-Philippine

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Chipmos

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C JESD22-A-108	P
High Temperature Operating Life Early Failure Rate Regulator On	Dynamic Operating Condition, Vcc Max=2.05V, 150°C JESD22-A-108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C /150°C JESD22-A-108	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at LFR 80hrs, 500hrs & 1000hrs	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.05V/2.25V, 150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.25V, -30°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 85%RH, 2.25V Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+ Reflow, 260°C+0, -5°C	P
Temperature Humidity Bias Test (THB)	JESD22-A101: 85°C, 85%RH, 2.25V Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+ Reflow, 260°C+0, -5°C	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65 °C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+ Reflow, 260°C+0, -5°C	P
Pressure Cooker	JESD22-A102:121°C /100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+ Reflow, 260°C+0, -5°C	P
High Temperature Storage	JESD22-A103: 150 C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V, JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101	P
Electrostatic Discharge Machine Model (ESD-MM)	200V, JESD22-A115	P
Soft Error (Alpha Particle)	JESD89	P
Soft Error (Neutron/Proton)	JESD89	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+ Reflow, 260°C+0, -5°C	P
Dynamic Latchup	JESD78	P
Static Latchup	125C, ± 200mA / ± 140mA JESD78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	3,041 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate (150°C)	89,000 DHRs	0	0.7	170	18 FIT
High Temperature Operating Life[1,2] Long Term Failure Rate (125°C)	661,588 DHRs	0	0.7	55	

[1] Assuming an ambient temperature of 55□C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	500	178	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA							
CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	
STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	

Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: SER – ALPHA PARTICLE, 3-TEMP, 3-VOLTAGE, @ 85C, Vcc Nom							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
STRESS: X-SECTION/STEM XY AUDIT							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		

Reliability Test Data

QTP #: 093202

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	COMP	8	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	1000	80	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	96	596	0	
CY7C15631KV18 (7C1553K)	8910015	610921676	TAIWN-G	96	711	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	96	1795	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	168	190	0	
CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	500	184	0	

Reliability Test Data

QTP #: 100901

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C11739KV18 (7C11739K)	8014006	611039246	CML-RA	COMP	8	0	
CY7C1313KV18 (7C1313K)	8018004	611051407	CML-RA	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C11739KV18 (7C11739K)	8014006	611039246	CML-RA	COMP	9	0	
CY7C1313KV18 (7C1313K)	8018004	611051407	CML-RA	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY7C11739KV18 (7C11739K)	8014006	611039246	CML-RA	COMP	5	0	
CY7C1313KV18 (7C1313K)	8018004	611051407	CML-RA	COMP	5	0	
STRESS: ELECTRICAL PARAMETER ASSESSMENT, Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	COMP	12	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE REGULATOR ON (125C, 2.05V)							
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	96	45	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	96	1526	0	
CY7C1313KV18 (7C1313K)	8012001	611023529RN	CML-RA	96	1515	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V							
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	168	183	0	
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	500	182	0	
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	1000	181	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.05V							
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	168	77	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	96	79	0	
CY7C11739KV18 (7C11739K)	8014006	611039246	CML-RA	96	77	0	
CY7C11739KV18 (7C11739K)	8014006	611039246	CML-RA	168	77	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 2.85V, +/140mA							
CY7C11739KV18 (7C11739K)	8012001	611023530	CML-RA	COMP	6	0	
CY7C11738KV18 (7C11738K)	8012001	611023528	CML-RA	COMP	6	0	

Reliability Test Data

QTP #: 100901

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	500	76	0	
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	1000	76	0	
STRESS: SER – ALPHA PARTICLE, 3-TEMP @ 88C, Vcc Nom							
CY7C1313KV18 (7C1313K)	8012001	611023529	CML-RA	COMP	3	0	

Document History Page

Document Title: 100901: LL65 18 MEG QDR/DDR SYNCHRONOUS PRODUCT QUALIFICATION REPORT
Document Number: 001-65263

Rev.	ECN No.	Orig. of Change	Description of Change
**	3086614	NSR	Initial spec release.
*A	3182786	CS	Added LL65nm 18M QDR device/bond option 7C1319K, Memo CS-478.
*B	3387797	CS NSR	Sunset Review - Added LL65nm 18M QDR device/bond option 7C1311K, Memo CS-519. Remove the QTP version on the Title page. Changed Spec Category from 'Customer Specific Notification Report' to 'Qualification Report'.
*C	3498743	NSR	CY7C1392KV18 with reference to Memo GRW-376.
*D	3815658	NSR	Removed reference Cypress spec in reliability tests performed table.
*E	4202436	JYF	Sunset review: Updated title of QA Engineering Director to Reliability Director; Updated device division from MID to MPD; Complete re-write of Reliability Tests Performed table for template alignment;
*F	4583766	JYF	Sunset review: Updated QTP title page for template alignment.

Distribution: WEB

Posting: None