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Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Cypress Semiconductor
Technology Qualification Plan

QTP# 092508 VERSION *A
July 2014

Simtek 256K nvSAM Product Family 0.8µ SONOS Technology	
STK11C88 **STK14C88** **STK15C88** **STK16C88**	**5V 256K Non-Volatile SRAM**

FOR ANY QUESTIONS ON THIS REPORT, PLEAE CONTACT
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QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
092508		Qualification of Simtek 256K 5V nvSRAM Products using 0.8umTechnology, Chartered Semiconductor (CSM2, Fab2). It is a acquisition product qual by extension.		August 2009

PRODUCT DESCRIPTION (for qualification)	
Purpose: Qualification of Simtek 256K nvSRAM Products on 0.8µ Technology fabricated at Chartered Semiconductor	
Marketing Part #:	STK11C88, STK14C88, STK15C88, STK16C88
Device Description:	5V Commercial and Industrial available in 28/32-Lead SOIC (300mils) Package
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION	
Metal Composition Passivation Type and Materials:	8000A Al-Si-Cu, 1000A TI/TIN 7000A Silicon Nitride, 3000A Silicon Dioxide
Generic Process Technology/Design Rule (-drawn):	0.8um 8F2 DT Technology
Gate Oxide Material/Thickness (MOS):	SiO2 Thickness
Name/Location of Die Fab (prime) Facility:	Chartered Semiconductor, Singapore
Die Fab Line ID/Wafer Process ID:	2N822-734-00A, 2N822-700-00A

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
28/32-Lead SOIC	**AMKOR-PHILS**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	SZ32
Package Outline, Type, or Name:	32-Lead SOIC (300mils)
Mold Compound Name/Manufacturer:	G600 Sumitomo
Mold Compound Flammability Rating:	UL94-V0
Oxygen Rating Index:	None
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	100% Matte Sn
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Sawing
Die Attach Supplier:	Ablestik
Die Attach Material:	8290
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.2 mil
Thermal Resistance Theta JA °C/W:	44.3°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	PHIL-M
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	KYEC-Taiwan

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life [HTOL]	MIL-STD-883, Method 1005 Dynamic Operating Condition, Full SRAM Array, Vcc Nom, 125°C	P
Data Retention	MIL-STD-883, Method 1008 Unbiased, 150°C, Store nv array at 0 hour read stored data	P
Endurance	Per datasheet Store/Recall cycles of full nv array functional check at read points	P
Electrostatic Discharge Human Body Model (ESD-HBM)	JESD22-A114-B 1,800V	P
Static Latch-up	JEDEC 78 70C, ± 100mA	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life[1,2] Long Term Failure Rate	467,000 DHRs	0	0.7	55	35 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Qualification Summary

CSM2 0.8µ CMOS/SNOS Process, Simtek 256K 5V nvSRAM

Test	Method	Conditions	Readpoint	Start Qty	# of Failures	Failure Detail
High Temperature Operating Life [HTOL]	Mil-Std-883, M1005	Dynamic Full SRAM Array 125C Vcc nom	0 hrs	467	0	
			168 hrs	467	0	
			500 hrs	467	0	
			1000 hrs	467	0	4 Fab Lots, Zero fails @ 1K hours
Retention	Mil-Std-883, M1008	Unbiased Bake 150C Store nv array at 0 hr Read stored data at read points 4 Fab Lots	0 hrs	400	0	
			48 hrs	400	0	
			168 hrs	400	1	1 fail at 10yr/70C equivalent & 1 fail at 10yr/85C equivalent. Corrective
			500 hrs	399	1	Adjust retention screen limit. Corrective actions complete & verified
			1000 hrs	398	0	4 Fab Lots
Endurance	Per Datasheet	Store/Recall cycles of nv array Recall and Functional check at read points	0 cycles	269	0	
			100K cycles	269	0	
			500K cycles	269	0	
			1M cycles	269	0	3 lots. Zero fails @ 1M cycles.
ESD	JEDEC 22-B A114	Human Body Model		6	0	Pass 1.8KV
Latch-Up Integrity	JEDEC 78	± 100mA, 70C		6	0	Pass ±100mA, 70C

Note 1: 2 failures recorded in retention testing [store NV array followed by unbiased bake with interim readpoints to verify stored data pattern is no corrupted and all cells read correct data state]. Wafer level retention screening limits adjusted to provide greater margin against Data Sheet Retention specification.

Reference Simtek Qualification Report: STK-05-51-029 03

Document History Page

Document Title: QTP# 092508: SIMTEK 256K NVSAM PRODUCT FAMILY "STK11C88 /14C88/15C88/16C88" 0.8 SONOS TECHNOLOGY
Document Number: 001-88101

Rev.	ECN No.	Orig. of Change	Description of Change
**	4039244	HSTO	Initial Spec Release Qualification report published on Cypress.com is documented on memo ZIJ-98 and was transferred to qualification report spec template. Deleted Cypress obsolete referenced spec in Major package qualification details. Updated package availability based on current qualified test & assembly site.
*A	4431902	HSTO	Align qualification report based on the new template in the front page Update Cypress division from Memory Image Division (MID) to Memory Product Division (MPD) at page3.

Distribution: WEB

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