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# Cypress Semiconductor Product Qualification Report

**QTP# 091706 VERSION\*J**  
**September, 2014**

<b>72 Meg QDR/DDR Synchronous SRAM Family</b>	
<b>65nm (LL65P-18R) Technology, UMC Fab 12A</b>	
<b>CY7C11431KV18</b>	<b>18-Mbit QDRII+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)</b>
<b>CY7C11481/501KV18</b>	<b>18-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)</b>
<b>CY7C11651KV18</b>	<b>18-Mbit QDRII+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C11681/701KV18</b>	<b>18-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C13121KV18</b>	<b>18-Mbit QDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C13141KV18</b>	<b>18-Mbit QDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C13201KV18</b>	<b>18-Mbit DDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C21701KV18</b>	<b>18-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) With ODT</b>
<b>CY7C12651KV18</b>	<b>36-Mbit QDRII+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C12451KV18</b>	<b>36-Mbit QDRII+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)</b>
<b>CY7C12481KV18</b>	<b>36-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)</b>
<b>CY7C12501KV18</b>	<b>36-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)</b>
<b>CY7C12631KV18</b>	<b>36-Mbit QDRII+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C12681KV18</b>	<b>36-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C12701KV18</b>	<b>36-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C14121KV18</b>	<b>36-Mbit QDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C14141/251KV18</b>	<b>36-Mbit QDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C14181KV18</b>	<b>36-Mbit DDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C14201KV18</b>	<b>36-Mbit DDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C1512/14KV18</b>	<b>72-Mbit QDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C1513/15KV18</b>	<b>72-Mbit QDRII SRAM 4-Word Burst Architecture</b>

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<b>72 Meg QDR/DDR Synchronous SRAM Family</b> <b>65nm (LL65P-18R) Technology, UMC Fab 12A</b>	
<b>CY7C1518/20KV18</b>	<b>72-Mbit DDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C1523KV18</b>	<b>72-Mbit DDRII SIO SRAM 2-Word Burst Architecture</b>
<b>CY7C1525KV18</b>	<b>72-Mbit QDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C1526KV18</b>	<b>72-Mbit QDRII SRAM 4-Word Burst Architecture</b>
<b>CY7C1542KV18</b>	<b>72-Mbit QDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)</b>
<b>CY7C1543/45KV18</b>	<b>72-Mbit QDRII+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)</b>
<b>CY7C1548/50KV18</b>	<b>72-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)</b>
<b>CY7C1563/631/632KV18</b> <b>CY7C1565KV18</b>	<b>72-Mbit QDRII+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C1564KV18</b>	<b>72-Mbit QDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C1568/70KV18</b>	<b>72-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)</b>
<b>CY7C25442KV18</b>	<b>72-Mbit QDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency) with ODT</b>
<b>CY7C25632/652KV18</b>	<b>72-Mbit QDRII+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency) with ODT</b>
<b>CY7C25682/702KV18</b>	<b>72-Mbit DDRII+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency) with ODT</b>
<b>CY7C1518/20KV18</b>	<b>72-Mbit DDRII SRAM 2-Word Burst Architecture</b>
<b>CY7C1521KV18</b>	<b>72-Mbit DDRII SRAM 4-Word Burst Architecture</b>
<b>CY7C25422KV18</b>	<b>72-Mbit QDRII+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency) with ODT</b>

## FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT

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## QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
091706	Qualification of 65nm (LL65) Technology at UMC Fab 12A and New Device CY7C1553K Base Die Product Family	Aug 2009
093202	Qualification of UMC 65nm Process Improvement	Nov 2009

<b>PRODUCT DESCRIPTION (for qualification)</b>	
Qualification Purpose:	Qualify UMC Fab 12A 65nm (LL65P-18R) Technology and 7C1553K base die product family
Marketing Part #:	CY7C1514KV18, CY7C15631KV18
Device Description:	1.8V Commercial and Industrial available in 165-Ball FBGA (13 x 15 x 1.4 mm)
Cypress Division:	Cypress Semiconductor Corporation –Memory & Image Division
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. K
What ID markings on Die:	7C1553K

<b>TECHNOLOGY/FAB PROCESS DESCRIPTION – LL65P-18R</b>			
Number of Metal Layers:	5+RDL	Metal Composition:	Metal 1: Cu 0.18um Metal 2: Cu 0.22um Metal 3: Cu 0.22um Metal 4: Cu 0.36um Metal 5: Cu 1.25um Metal 6 (RDL): Al 1.2um
Passivation Type and Materials:	0.4um Oxide / 0.5um Nitride		
Free Phosphorus contents in top glass layer(%):	0 %		
Number of Transistors in Device	~600M		
Number of Logic Gates in Device	~300M		
Generic Process Technology/Design Rule (μ-drawn):	CMOS, 65nm		
Gate Oxide Material/Thickness (MOS):	19.5A		
Name/Location of Die Fab (prime) Facility:	UMC Fab 12		
Die Fab Line ID/Wafer Process ID:	L65LL		

#### PACKAGE AVAILABILITY

<b>PACKAGE</b>	<b>ASSEMBLY SITE FACILITY</b>
<b>165-Ball FBGA</b>	<b>ASE-Taiwan, CML Autoline</b>

**Note:** Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	KE-G2270 / Kyocera
Mold Compound Flammability Rating:	UL94, V-0
Oxygen Rating Index:	N/A
Substrate Material:	BT resin
Lead Finish, Composition / Thickness:	Sn63Pb37
Die Backside Preparation Method/Metallization:	Grinding
Die Separation Method:	Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	2025D
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-42742
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	13.7
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-06518
Name/Location of Assembly (prime) facility:	ASE-Taiwan/CML-Philippine

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Chipmos

**Note:** Please contact a Cypress Representative for other packages availability

### RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Boost Regulated at Core 1.45V, External 2.05V, 125°C /150°C JESD22-A108	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at LFR 80hrs, 500hrs & 1000hrs	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max= 2.25V, 150°C JESD22-A108	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 2.25V, -30°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130°C, 85%RH, 2.25V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Temperature Humidity Bias Test (THB)	JESD22-A101: 85°C/ 85% RH , 2.25V Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 PSIG Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Precondition	JESD22	P
High Temperature Storage	JESD22-A103:150°C No bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V, JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101	P
Electrostatic Discharge Machine Model (ESD-MM)	200V, JESD22-A115	P
Soft Error (Alpha Particle)	JESD89	P
Soft Error (Neutron/Proton)	JESD89	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Dynamic Latch-up	JESD78	P
Static Latch-up	125°C , ± 240mA, JESD78	P

### RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF <sup>3</sup>	Failure Rate
High Temperature Operating Life Early Failure Rate	9,007 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life <sup>1,2</sup> Long Term Failure Rate (150 °C)	89,000 DHRs	0	0.7	170	22 FIT
High Temperature Operating Life <sup>1,2</sup> Long Term Failure Rate (125 °C)	479,920 DHRs	0	0.7	55	

<sup>1</sup> Assuming an ambient temperature of 55 °C and a junction temperature rise of 15 °C.

<sup>2</sup> Chi-squared 60% estimations used to calculate the failure rate..

<sup>3</sup> Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[ \frac{E_A}{k} \left[ \frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

E<sub>A</sub> =The Activation Energy of the defect mechanism.

k = Boltzmann's constant = 8.62x10<sup>-5</sup> eV/Kelvin.

T<sub>1</sub> is the junction temperature of the device under stress and T<sub>2</sub> is the junction temperature of the device at use conditions.



## Reliability Test Data

**QTP #: 091706**

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Ass Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
<b>STRESS: ACOUSTIC, MSL3</b>							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	15	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	15	0	
<b>STRESS: AGE BOND STRENGTH</b>							
CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	5	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	5	0	
<b>STRESS: DYNAMIC LATCH-UP</b>							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V</b>							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	8	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	8	0	
<b>STRESS: ESD-CHARGE DEVICE MODEL, 500V</b>							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
<b>STRESS: ESD-MACHINE MODEL, 200V</b>							
CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	COMP	5	0	
<b>STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3</b>							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	128	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	128	77	0	
<b>STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C</b>							
CY7C1514KV18 (7C1553K)	8844020	610851583	TAIWN-G	1000	70	0	
<b>STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max</b>							
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	336	77	0	

## Reliability Test Data

QTP #: 091706

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
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**STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V**

CY7C15631KV18 (7C1553K)	8908001	610920385	TAIWN-G	96	2367	0	
CY7C15631KV18 (7C1553K)	8912000	610920386	TAIWN-G	96	2217	0	
CY7C15631KV18 (7C1553K)	8910015	610920548	TAIWN-G	96	1321	0	

**STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V**

CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	500	178	0	
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**STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V**

CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	178	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	178	0	

**STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 2.25V Vcc**

CY7C1514KV18 (7C1553K)	8842022	610852338	TAIWN-G	500	45	0	
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**STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3**

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	168	76	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	168	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	168	77	0	

**STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR**

CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	COMP	10	0	
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**STRESS: STATIC LATCH-UP TESTING, 125C, 3.42V, +/-240mA**

CY7C1514KV18 (7C1553K)	8844020	610854680	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	COMP	9	0	
CY7C1514KV18 (7C1553K)	8844021	610908348	TAIWN-G	COMP	9	0	
CY7C15631KV18 (7C1553K)	8911000	610922436	TAIWN-G	COMP	9	0	

**STRESS: TEMPERATURE CYCLE COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3**

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
CY7C1514KV18 (7C1553K)	8844020	610854240	TAIWN-G	1000	78	0	
CY7C1514KV18 (7C1553K)	8844022	610906896	TAIWN-G	1000	77	0	

**STRESS: STRESS: TEMPRATURE HUMIDITY TEST, 85C, 85%RH, 2.25V, PRE COND 192 HR 30C/60%RH, MSL3**

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	1000	77	0	
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## **Reliability Test Data**

**QTP #: 091706**

<b>Device</b>	<b>Fab Lot #</b>	<b>Assy Lot #</b>	<b>Ass Loc</b>	<b>Duration</b>	<b>Samp</b>	<b>Rej</b>	<b>Failure Mechanism</b>
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**STRESS: SER – ALPHA PARTICLE, 3-TEPM, 3-VOLTAGE, @ 85C, Vcc Nom**

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	3	0	
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**STRESS: X-SECTION/STEM XY AUDIT**

CY7C1514KV18 (7C1553K)	8842022	610851583	TAIWN-G	COMP	1WF		
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## Reliability Test Data

QTP #: 093202

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
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**STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V**

CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	COMP	8	0	
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**STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C**

CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	1000	80	0	
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**STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V**

CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	96	596	0	
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CY7C15631KV18 (7C1553K)	8910015	610921676	TAIWN-G	96	711	0	
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CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	96	1795	0	
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**STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, BOOST REGULATED AT CORE 1.45V, EXTERNAL 2.05V**

CY7C15631KV18 (7C1553K)	8912000	610921675	TAIWN-G	168	190	0	
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CY7C15631KV18 (7C1553K)	8911000	610922435	TAIWN-G	500	184	0	
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## Document History Page

Document Title: QTP 091706: LL65 72 MEG QDR/DDR SYNCHRONOUS PRODUCT QUALIFICATION REPORT  
Document Number: 001-58833

Rev.	ECN No.	Orig. of Change	Description of Change
**	2848621	ZIJ	Initial spec release. Added additional DDRII device/bond options to the current 65nm 72M QDR Product QTP report 091706 Rev1.4 Supporting documentation is as follows: - 7C11501K and 7C1523K -> Memo CS399 - 7C11701K and 7C12681K -> Memo CS404 - 7C14201K -> Memo CS408
*A	2880389	HGA	Added LL65nm 72M QDR devices/bond options: - (7C1553K) down bond option 7C13121K, memo CS-411 - (7C1553K) down bond options 7C12701K, 7C12481K, 7C12631K, 7C14121K and 7C14181K, memo- CS420 - (7C1553K) down bond option 7C12651K, memo CS-426
*B	2927484	ZIJ	Added QTP# 093202 reliability stress test data Revise the EFR sample size, LFR device hours and FIT rate Added LL65nm 72M QDR devices/bond options: - (7C1553K) down bond option 7C11431K, memo CS-429
*C	2933445	CS	Added LL65nm 72M QDR devices/bond option: - (7C1553K) down bond option 7C13141K, memo CS-433
*D	3065432	CS ZIJ	Added LL65nm 72M QDR devices/bond option: - (7C1553K) bond options 7C1564K and 7C2564K, memo CS-466 Made following changes to Latch-up test - Dynamic latch-up -> In accordance with Cypress Spec. 01-00081" - Static latch-up test -> In accordance with JESD78 and Cypress Spec. 01-00081 - Latch-up test condition correction (3.42V, +/-240mA) in the reliability database
*E	3156902	ZIJ	Per revision H design change, all 72M QDR ODT devices MFG part number will be changed by adding a "2" prior to the K. Example: Change CY7C2563KV18-* to CY25632KV18-* Reference memo: DEW-164 Removed part number CY7C2564KV18 that is not a MFG part.
*F	3386323	CS	Added LL65nm 72M QDR device/bond option: - (7C1553K) bond option 7C1542K, memo CS-526
*G	3895775	NSR	Added QTP 091706 in the spec title. Removed VERSION 2.0 in QTP# 091706 title page. Removed reference Cypress specs in the reliability tests performed table. Sunset Review.
*H	3989438	ILZ	Added device CY7C1518/20KV18(72-Mbit DDR-II SRAM 2-Word Burst

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Rev.	ECN No.	Orig. of Change	Description of Change
			Architecture ) and 7C1521KV18 (72-Mbit DDR-II SRAM 4-Word Burst Architecture ) on qualification coverage – front page Reliability Tests Performed Per Specification Requirement Deleted “3IR” in reflow step of HAST, PCT and TCT Deleted tolerance (+/-5) on HTS stress
*I	4241711	HSTO	Added device CY7C25422KV18 in the cover page in reference to memo GRW-418.
*J	4491532	JYF	-Updated QTP title page and Reliability Tests Performed table (EFR/LFR,HTSSL, LTOL, HAST, THB, PCT, HTS, Acoustic, Static/Dynamic Latch-Up) for template alignment. -Updated EFR quantity from 9,004 to 9,007 in Reliability Failure Rate Summary. -Updated stress duration of LFR-150°C from 1000 to 500 hours (Page 9).

Distribution: WEB

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