Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Cypress Semiconductor
Product Qualification Plan

QTP# 090604
August 2017

S8 K2 Product Qualification Non-Volatile SRAM Product Family Qualification Cypress, CMI (Fab 4)	
CY14B101LA (x8)/CY14B101NA (x16)	**3V 1M Parallel Non-RTC nvSRAM Device**
CY14B101KA (x8)/CY14B101MA (x16)	**3V 1M Parallel RTC nvSRAM Device**
CY14E101LA (x8)	**5V 1M Parallel Non-RTC nvSRAM Device**
CY14B256LA (x8) CY14B256NA (x16)	**3V 256K Parallel Non-RTC nvSRAM Device**
CY14B256KA (x8)	**3V 256K Parallel RTC nvSRAM Device**
CY14E256LA (x8)	**5V 256K Parallel Non-RTC nvSRAM Device**
CY14B101Q1/CY14B101Q2/CY14B101Q3	**3V 1M Serial Non-RTC nvSRAM Device**
CY14B101P	**3V 1M Serial RTC nvSRAM Device**
CY14B512Q1/CY14B512Q2/CY14B512Q3	**3V 512K Serial Non-RTC nvSRAM Device**
CY14B512P	**3V 512K Serial RTC nvSRAM Device**
CY14B256Q1/CY14B256Q2/CY14B256Q3	**3V 256K Serial Non-RTC nvSRAM Device**
CY14B256P	**3V 512K Serial RTC nvSRAM Device**
CY14V101LA/CY14V101NA	**1.8V 1M Parallel nvSRAM Device**
CY14V256LA	**1.8V 256K Parallel nvSRAM Device**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
reliability@cypress.com or via a CYLINK CRM CASE

Prepared By:
Josephine Pineda (JYF)
Staff Reliability Engineer

Reviewed By:
Yusaku Ota (YUOH)
Reliability Manager

Approved By:
David Hoffman (DHH)
Reliability Director

QUALIFICATION HISTORY

QTP#	Description of Qualification Purpose	Date Comp
071304	To qualify S8 SONOS technology and 4M nvSRAM devices CY14B104L / CY14B104N (7C14104AC base die) using S8TNV-5R, fabricated at Cypress Minnesota CMI (Fab4)	Nov 2008
090604	To qualify 1M nvSRAM K2 (with both RTC-Real Time Clock and bond options for Non-RTC) devices CY14B101*/CY14B512*/CY14E256* (7C14101CC base die) using S8TNV-5R, fabricated at Cypress Minnesota CMI (Fab4)	Sep 2009
100203	To qualify 1M nvSRAM K2 1.8V device option CY14V101LA/CY14V101NA (7C14121CC base die) using S8TNV-5R, fabricated at Cypress Minnesota CMI (Fab4)	July 2010

PRODUCT DESCRIPTION (for qualification)	
Purpose: Qualification of S8 technology & S8TNV-5R 1M nvSRAM product at CMI (Fab 4)	
Marketing Part #:	CY14B101*/CY14B512*/CY14B256*/ CY14V101*
Device Description:	1.8V, 3V & 5V Commercial/Industrial, available in 44-Lead TSOP II / 48-Lead SSOP / 32-Lead SOIC
Cypress Division:	Cypress Semiconductor Corporation – Memory Products Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	Proprietary	Metal Composition:	Proprietary
Passivation Type:		Proprietary	
Generic Process Technology/Design Rule (drawn):		Proprietary	
Gate Oxide Material/Thickness (MOS):		Proprietary	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4 / S8TNV-5R	

PACKAGE / ASSEMBLY INFORMATION	
Assembly Site:	ASE-TAIWAN / AMKOR-M
Package:	{48-Lead SSOP/44-Lead TSOP} / {32-Lead SOIC/16-Lead SOIC}
Mold Compound:	KEG600DA / G600
Die Attach:	Dexter QMI509 / Ablestik 8290
Die Size (Mils**):**	161.61 x 149.6
Leadframe Design:	{C7025-HALFHARD /8 DOT SLOTTED RMP} / {Cu/RMP (Reduced Metal Pad)}
Leadfinish/solder ball:	NiPdAu / Pure Sn
Wire (Al/Au) diam:	0.8 Mil / 1.0 Mil
MSL:	3
Solder Reflow Temp:	260C

Note: Package Qualification details upon request

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate (EFR)	Dynamic Operating Condition, 150°C, 2.7V/5.25V, 48 Hours	P
High Temperature Operating Life Latent Failure Rate (LFR)	Dynamic Operating Condition, 150°C, 2.7V/5.25V, 500 Hours	P
Pre/Post LFR AC/DC Char	AC/DC Critical Parameter Char at LFR 0hrs, 80hrs & 500hrs	P
Endurance	200K Cycles @ 90°C, Per datasheet	P
Endurance	1M Cycles @ 90°C	P
Data Retention	150°C, 1000 Hours	P
Temperature Cycle	-65°C to 150°C, JESD22-A-104	P
High Accelerated Saturation Test	130°C, 3.63V, 85%RH, JESD22-A-110	P
Pressure Cooker	121°C /100%RH, JESD22-A102	P
Precondition	JESD22 Moisture Sensitivity	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V, JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101	P
Electrostatic Discharge Machine Model (ESD-MM)	200V, JESD22-A115	P
Latch-up Sensitivity	5.4V,± 200mA, 125°C, EIA/JESD78	P
Age Bond Strength	Mil-Std-883, Method 2011	P
Acoustic	Per MSL3 Spec	P
Soft Error (Alpha Particle)	JESD89A	P
Soft Error (Neutron/Proton)	JESD89A	P
SEM X-Section	XY audit at center wafer and edge wafer	P
Low Temperature Operating Life Test	Dynamic Operating Condition, 2.7V, -30°C, 500 Hours	P
High Temp Steady State Life Test	Static Operating Condition, 2.7V, 150°C, 1000 Hours	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	4,009 Devices*	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate	387,000 DHRs*	0	0.7	170	14 FITs

* EFR data is based on QTP 090604 and QTP 100203 only, LFR data is based on QTP 071304, 090604 and 100203 data

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data
QTP # 071304

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.7V, Vcc Max							
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	48	1222	0	
CY14B104L (7C14104AC)	4814841	*610832326*	*CML-R*	48	1316	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	48	932	0	
CY14B104L (7C14104AC)	4819437	*610842294*	*CML-R*	48	813	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.7V, Vcc Max							
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	500	120	0	
CY14B104L (7C14104AC)	4814841	*610832326*	*CML-R*	500	120	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	500	119	0	
CY14B104L (7C14104AC)	4819437	*610842294*	*CML-R*	500	119	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	80/500	10	0	
CY14B104L (7C14104AC)	4814841	*610832326*	*CML-R*	80/500	10	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	80/500	10	0	
CY14B104L (7C14104AC)	4819437	*610842294*	*CML-R*	80/500	10	0	
STRESS: ENDURANCE, 200K CYCLES, 90C							
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	COMP	80	0	
CY14B104L (7C14104AC)	4817305	*610841260*	*CML-R*	COMP	77	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	COMP	160	0	
CY14B104L (7C14104AC)	4819437	*610842294*	*CML-R*	COMP	80	0	
CY14B104L (7C14104AC)	4817306/4818074		*CML-R*	COMP	3307	0	
STRESS: DATA RETENTION, 150C							
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	1000	77	0	
CY14B104L (WAFER)	4817306	*610830615*	*CML-R*	1008	228	0	
CY14B104L (7C14104AC)	4817305	*610841260*	*CML-R*	1000	80	0	
CY14B104L (WAFER)	4817305	*610841260*	*CML-R*	1008	216	0	
CY14B104L (7C14104AC)	4818074	*N/A*	*CML-R*	1000	80	0	
CY14B104L (WAFER)	4818074	*N/A*	*CML-R*	1008	402	0	

Reliability Test Data
QTP # 071304

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY14B104L (7C14104AC)	4807004	*610812949*	*CML-R*	COMP	8	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	COMP	8	0	
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY14B104L (7C14104AC)	4807004	*610812949*	*CML-R*	COMP	9	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	COMP	9	0	
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY14B104L (7C14104AC)	4807004	*610812949*	*CML-R*	COMP	5	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	COMP	5	0	
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	COMP	5	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 1.98V, PRE COND 192 HR 30C/60%RH, MSL3							
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	128	77	0	
CY14B104L (7C14104AC)	4814841	*610832326*	*CML-R*	128	80	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	128	77	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY14B104L (7C14104AC)	4807004	*610812949*	*CML-R*	168	77	0	
CY14B104L (7C14104AC)	4814841	*610832326*	*CML-R*	168	80	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	168	77	0	
STRESS: Temperature Cycle COND. C, -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY14B104L (7C14104AC)	4807004	*610812949*	*CML-R*	1000	77	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	1000	80	0	
CY14B104L (7C14104AC)	4814841	*610832326*	*CML-R*	500	80	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, ±200mA							
CY14B104L (7C14104AC)	4807004	*610812949*	*CML-R*	COMP	6	0	
CY14B104L (7C14104AC)	4814841	*610832326*	*CML-R*	COMP	6	0	
CY14B104L (7C14104AC)	4819437	*610842294*	*CML-R*	COMP	6	0	

Reliability Test Data
QTP # 071304

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: AGE BOND							
CY14B104L (7C14104AC)	4807004	*610812949*	*CML-R*	COMP	10	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	COMP	10	0	
CY14B104L (WAFER)	4818074	*N/A*	*CML-R*	COMP	10	0	
STRESS: ACOUSTIC-MSL3							
CY14B104L (7C14104AC)	4807004	*610812949*	*CML-R*	COMP	15	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	COMP	15	0	
CY14B104L (7C14104AC)	4814841	*610832326*	*CML-R*	COMP	15	0	
STRESS: SER – ALPHA PARTICLE, 3-TEPM, 3-VOLTAGE, FIT=550 FIT/Mbit @ 85C, Vcc Nom							
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	COMP	3	0	
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	COMP	3	0	
CY14B104L (7C14104AC)	4819437	*610842294*	*CML-R*	COMP	3	0	
STRESS: SER – NEUTRON/PROTON							
CY14B104L (7C14104AC)	4808220	*N/A*	*CML-R*	COMP	3	0	
STRESS: LOW TEMPERATURE OPERATING LIFE TEST, -30C, 2.7V, Vcc Max							
CY14B104L (7C14104AC)	4817306	*610830615*	*CML-R*	500	77	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.7V, Vcc Max							
CY14B104L (7C14104AC)	4811240	*610819876*	*CML-R*	1000	76	0	

Reliability Test Data
QTP # 090604

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.7V, Vcc Max							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	48	1153	0	
CY14101B8CC (7C14101CC)	4910444	*610922709*	*CML-R*	48	688	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.7V, Vcc Max							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	500	118	0	
STRESS: Pre-/ Post HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE CHAR							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	80/500	10	0	
STRESS: ENDURANCE (90C), 200K CYCLES+168 HOURS DATA RETENSION							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	COMP	80	0	
STRESS: DATA RETENTION (150C) + 200K ENDURANCE							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	1000	80	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	COMP	9	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	288	77	0	
STRESS: TEMPERATURE CYCLE COND. C, -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	1000	77	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, ±200mA							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	COMP	9	0	
STRESS: ACOUSTIC-MSL3							
CY14101B8C (7C14101CC)	4908403	610918063	*CML-R*	COMP	15	0	
STRESS: SER – ALPHA PARTICLE, 3-TEPM, 3-VOLTAGE, @ 85C, Vcc Nom							
CY14101B8C (7C14101CC)	4908403	610918063	*CML-R*	COMP	3	0	
STRESS: AGE BOND							
CY14101B8C (7C14101CC)	4908403	*610918063*	*CML-R*	COMP	3	0	
STRESS: ENDURANCE (90C) 1 MILLION CYCLES+168 HOURS DATA RETENTION							
CY14B101LA (7C1401B8CC)	4910267	*610935909*	*CML-R*	COMP	80	0	

Reliability Test Data
QTP # 100203

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ACOUSTIC-MSL3							
CY14V101LA (7C1421B8C)	4944705	*HA1011002*	*T-Taiwan*	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 5.25V, Vcc Max							
CY7C1421B8C (7C1421B8C)	4944705	*611017304*	*G-Taiwan*	48	2162	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 5.25V, Vcc Max							
CY7C1421B8C (7C1421B8C)	4944705	*611017304*	*G-Taiwan*	500	178	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY14V101LA (7C1421B8C)	4944705	*HA1011002*	*T-Taiwan*	COMP	8	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY14V101LA (7C1421B8C)	4944705	*HA1011002*	*T-Taiwan*	COMP	9	0	
STRESS: ESD-MACHINE MODEL, 200V							
CY14V101LA (7C1421B8C)	4944705	*HA1011002*	*T-Taiwan*	COMP	5	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 5.4V, ±140mA							
CY14V101LA (7C1421B8C)	4944705	*HA1011002*	*T-Taiwan*	COMP	6	0	
STRESS: TEMPERATURE CYCLE COND. C, -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY14V101LA (7C1421B8C)	4944705	*HA1011002*	*T-Taiwan*	500	80	0	

Document History Page

Document Title: QTP 090604: S8 K2 1M NVSRAM PRODUCT QUALIFICATION REPORT
Document Number: 001-58834

Rev.	ECN No.	Orig. of Change	Description of Change
**	2846750	ZIJ	Initial Spec Release Added 1 Million Endurance Qualification data from 4 Meg Evans nvSRAM QTP 092804
*A	2879283	NRG	Changed the version from Version 2 to Version 3 and month from January to February Changed the Assembly Site from CML-RA to CML-R and added ASE-Taiwan on Package / Assembly Information Table Changed all Assy Loc from CML-RA to CML-R Added 1 Million Endurance Cycling Test data to K2 1M QTP 090604
*B	3416227	NSR	Removed ** markers. Removed QTP version in front page Removed QTP#082704 and 092804 in qualification history page and QTP data Added QTP# 090604 in the title Added QTP#100203 in qualification history page and QTP data Added CY14V101LA/CY14V101NA devices in Title page Recomputed EFR and LFR failure rate Changed of QTP revision date in the title page.
*C	3888273	ZIJ	Sunset review Removed all Cypress spec reference number in page4 table.
*D	4257074	HSTO	Updated the “Technology/Fab Process Description” table in page3.
*E	5843960	JYF DCON	-Updated the following: CY logo, reference for Reliability personnel, CY division from MID to MPD, Technology/Fab Process table -Aligned cover page with template -Deleted CML-R Assy site in Package/Assy table -Deleted revision of Industry standard in Rel Tests performed table -Added CY14V256LA in MPN coverage. Removed Distribution and Posting information from Document History Page.