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Cypress Semiconductor Product Qualification Plan

**QTP# 080608
May 2013**

HIGH ACCURACY EPROM PROGRAMMABLE DEVICE FAMILY L28 TECHNOLOGY, TSMC-2A	
CY2077	High-Accuracy EPROM Programmable PLL Die for Crystal
CY5037	High-Accuracy EPROM Programmable PLL Die for Crystal Oscillator

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PACKAGE QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
99285	To qualify L28-TSMC Technology in TMS-2A	May 2003
080608	CY5037 (7C80383B die) L28 Process Transfer from CTI Fab2 to TSMC-2A	Aug 2008

PRODUCT DESCRIPTION (for qualification)	
Purpose: CY5037 (7C80383B die) L28 process transfer from CTI Fab2 to TSMC-2A	
Marketing Part #:	CY5037, CY2077
Device Description:	3.3V and 5V Commercial/Industrial, available in 8-Lead SOIC
Cypress Division:	Cypress Semiconductor Corporation –Data Communication Division (DCD)

TECHNOLOGY/FAB PROCESS DESCRIPTION :			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 400Å Ti / 1,000Å TiN/ 4,700Å AlSiCu/ 375Å TiN Metal 2: 1,500 Å Ti / 8,000Å AlSiCu / 375Å TiN
Passivation Type and Materials:	3,000Å SiN / 3,150Å SOG, 1,200Å SiN		
Generic Process Technology/Design	CMOS, Single Poly, Double Metal/0.65um		
Gate Oxide Material/Thickness	SiO ₂ / 125 Å		
Name/Location of Die Fab (prime)	TSMC-2A, Taiwan		
Die Fab Line ID/Wafer Process ID:	TSMC-2A/L28 TSMC		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
8-pin Pb-Free SOIC package	PHIL-M, CML-RA

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	SZ165
Package Outline, Type, or Name:	16-Lead Small Outline IC (SOIC)
Mold Compound Name/Manufacturer:	Sumitomo 6600H
Mold Compound Flammability Rating:	V-O per UL-94
Mold Compound Alpha Emission Rate	N/A
Oxygen Rating Index:	None
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Pure Tin
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	8290
Die Attach Method:	Eutectic
Bond Diagram Designation:	001-45703
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au 1.0mil
Thermal Resistance Theta JA °C/W:	192°C/W
Package Cross Section Yes/No:	No
Assembly Process Flow:	49-24026
Name/Location of Assembly (prime) facility:	Amkor Philippines (Phil-M)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C Dynamic Operating Condition, Vcc = 5.5V, 150°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V, 150°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity Level 1 (168 hrs, 85C/85%RH)	P
High Accelerated Saturation Test (HAST)	130C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs, 85C/85%RH)	P
High Temperature Steady Life Test	VCC=150C/3.63V	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7 2,200V JESD22, METHOD A114E	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101C	P
Low Temperature Operating Life	-30C, 3.8V	P
Pressure Cooker	121C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity Level 1 (168 Hrs, 85C/85%RH)	P
Data Retention	150C, No Bias	P
Latchup Sensitivity	110V, ± 200mA In accordance with JEDEC 17 125 C, ± 200mA, In accordance with JEDEC-78	P

RELIABILITY FAILURE RATE SUMMARY

QTP# 99285 Summary

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor ³	Failure Rate
High Temperature Operating Life Early Failure Rate	1019	0	N/A	N/A	0 PPM
High Temperature Operating Life ^{1,2} Long Term Failure Rate	181,660HRs	0	0.7	170	30FIT

QTP# 080608 Summary

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor ³	Failure Rate
High Temperature Operating Life Early Failure Rate	1500	0	N/A	N/A	0 PPM
High Temperature Operating Life ^{1,2} Long Term Failure Rate	240,828HRs	1	0.7	170	49FIT

¹ Assuming an ambient temperature of 150°C and a junction temperature rise of 15°C.

² Chi-squared 60% estimations used to calculate the failure rate.

³ Thermal Acceleration Factor is calculated from the

Arrhenius equation

$$AF = \exp \left[\frac{E_A}{k} \left[\frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

EA =The Activation Energy of the defect mechanism. k = Boltzmann's constant = 8.62x10⁻⁵ eV/Kelvin.

T1 is the junction temperature of the device under stress and T2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 99285

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: DATA RETENTION, PLASTIC, 150C							
CY2280-OC	2937109	619927291/2/3	CML-R	500	85	0	
STRESS: ESD-CHARGE DEVICE MODEL, (1000V)							
CY2280-OC	2937109	619927291/2/3	CMLI-R	COMP	3	0	
CY2280-OC	2937190	619928659/60/61	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER PER MIL STD 883, METHOD 3015 (2,200V)							
CY2280-OC	2937109	619927291/2/3	CML-R	COMP	3	0	
CY2280-OC	2937190	619928659/60/61	CML-R	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V, Vcc Max)							
CY2280-OC	2937109	619927291/2/3	CML-R	48	335	0	
CY2280-OC	2937190	619928659/60/61	CML-R	48	234	0	
CY2280-OC	2937190	619928659/60/61	CML-R	48	101	0	
CY2280-OC	2942829	619933793/4/5	CML-R	48	349	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V, Vcc Max)							
CY2280-OC	2937109	619927291/2/3	CML-R	80	120	0	
CY2280-OC	2937109	619927291/2/3	CML-R	500	120	0	
CY2280-OC	2937190	619928659/60/61	CML-R	80	120	0	
CY2280-OC	2937190	619928659/60/61	CML-R	500	120	0	
CY2280-OC	2942829	619933793/4/5	CML-R	80	125	0	
CY2280-OC	2942829	619933793/4/5	CML-R	500	123	0	
STRESS: HI-ACCEL SATURATION TEST (140C/85%RH/3.63V), PRECOND. 168 HRS 85C/85%RH							
CY2280-OC	2937109	619927291/2/3	CML-R	128	50	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (150C, 3.63V)							
CY2280-OC	2937109	619927291/2/3	CML-R	80	77	0	
CY2280-OC	2937109	619927291/2/3	CML-R	168	77	0	
STRESS: LOW TEMPERATURE OPERATING LIFE (-30C/8MHZ)							
CY2280-OC	2937190	619928659/60/61	CMLR	500	50	0	
STRESS: PRESSURE COOKER TEST, MSL 1 (121C, 100%RH)							
CY2280-OC	2937109	619927291/2/3	CML-R	168	53	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 168 HRS 85C/85%RH (MSL 1))							
CY2280-OC	2937109	619927291/2/3	CML-R	300	50	0	

Reliability Test Data

QTP #: 080608

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.5V, Vcc Max)							
CY2077E(7C80383B)	2820733	610825222/223/224	M-PHIL	48	1500	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 5.5V, Vcc Max)							
CY2077E(7C80383B)	2820733	610825222/223/224	M-PHIL	168	119	1	weak EPROM bits – FA 080608-1L1 CAR # 200835004
CY2077E(7C80383B)	2820733	610825222/223/224	M-PHIL	500	118	0	
STRESS: DATA RETENTION, PLASTIC, 150C							
CY2077E(7C80383B)	2820733	610825222/223/224	M-PHIL	500	77	0	
CY2077E(7C80383B)	2820733	610825222/223/224	M-PHIL	1000	77	0	
STRESS: ESD-CHARGE DEVICE MODEL, (500V)							
CY2077E(7C80383B)	2820733	610825222/223/224	M-PHIL	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-E, (2,200V)							
CY2077E(7C80383B)	2820733	610825222/223/224	M-PHIL	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, ±200mA, 8.25V)							
CY2077E(7C80383B)	2820733	610825222/223/224	M-PHIL	COMP	6	0	
STRESS: ETEST DATA							
CY2077E(7C80383B)	2820733		COMPARABLE				
STRESS: SORT YIELD							
CY2077E(7C80383B)	2820733		COMPARABLE				

Document History Page

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Rev.	ECN No.	Orig. of Change	Description of Change
**	4011453	ILZ	Initial Spec Release Qualification report published on Cypress.com is documented on memo HGA-603 and not in spec format. Initiated spec for QTP 080608 and data from HGA-603 was transferred to qualification report spec template

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