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Cypress Semiconductor
Product Qualification Report

QTP# 080602 VERSION*A
November, 2014

16 Meg Fast Asynchronous SRAM Family C9FD-3R Technology, Fab4	
CY7C1061DV33	16-Mbit (1M X 16) Static RAM
CY7C1069DV33	16-Mbit (2M x 8) Static RAM
CY7C1024DV33	3-Mbit (128K X 24) Static RAM
CY7C1034DV33	6-Mbit (256K X 24) Static RAM
CY7C1012DV33	12-Mbit (512K X 24) Static RAM
CY7C1062DV33	16-Mbit (512K X 32) Static RAM

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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Prepared By:
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
052207	C9FD-3R, Fab 4 New Process using CY7C104*D (4Meg Fast Synchronous SRAM) Product Family	Mar 06
080602	Qualification of Device 7C1061NC - 16Meg, C9FD-3R Technology (Fast Asynchronous SRAM) with RevB DDLIM Mask Fabricated at Fab4 (CMI)	Jun 08

PRODUCT DESCRIPTION (for qualification)	
Purpose: Qualify 16Meg (7C1061NC) Fast Asynchronous SRAM in C9FD-3R Technology	
Marketing Part #:	CY7C1061DV33, CY7C1069DV33, CY7C1024DV33, CY7C1034DV33, CY7C1012DV33, CY7C1062DV33
Device Description:	16M Fast Asynchronous SRAM
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION – C9FD-3R			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 100Å Ti / 3200Å Al / 300Å TiW Metal 2: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:		Si_2N_3 7000Å & SiO2 700Å (on metal2), Si_2N_3 9000Å & SiO2 1000Å (on flat)	
Generic Process Technology/Design Rule (□-drawn):		C9FD-3R/0.90µm	
Gate Oxide Material/Thickness (MOS):		20.5Å (LV) & 58Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/C9FD-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
54-Lead TSOPII	**ASE-Taiwan (G)**
119 BGA	**ASE-Taiwan (G)**
48 BGA	**ASE-Taiwan (G)**

Note: Package Qualification details upon request.

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZW54
Package Outline, Type, or Name:	54-Lead Thin Small Outline Packages (Type II)
Mold Compound Name/Manufacturer:	Hitachi CEL9200THFU
Mold Compound Flammability Rating:	NA
Mold Compound Alpha Emission Rate:	NA
Oxygen Rating Index:	NA
Lead Frame Material:	Copper base
Lead Finish, Composition / Thickness:	Pure Sn
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	100% Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8340
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-10041
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0mil
Thermal Resistance Theta JA °C/W:	50.38
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41043
Name/Location of Assembly (prime) facility:	ASE-Taiwan (G)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R

Note: Please contact a Cypress Representative for other package availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 3.77V, 150°C Dynamic Operating Condition, Vcc Max = 3.77V, 125°C JESD22-A108	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 3.77V, 150°C Dynamic Operating Condition, Vcc Max = 3.77V, 125°C JESD22-A108	P
Long Life Verification	Dynamic Operating Condition, Vcc = 3.77V, 150°C JESD22-A108	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max = 3.77V, 150°C Static Operating Condition, Vcc Max = 3.77V, 150°C JESD22-A108	P
High Accelerated Saturation Test (HAST)	JESD22-A110: 130°C, 3.63V/3.65V, 85%RH Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Pressure Cooker	JESD22-A102: 121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
High Temperature Storage	JESD22-A103: 150°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level (192 Hrs., 30°C, 60% RH, 260°C Reflow)	P
Static Latch up	125C, ± 200/200mA JESD-78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	2994 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	2,683,300 DHRs	6*	0.7	170	18 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

* Failures are fixed with reference corrective action (CAR) # 200613035.

Reliability Test Data
QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	15	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	15	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	10	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	10	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	10	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	48	1551	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	48	1518	1	LI DEFFECT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	48	3314	1	NON-VISUAL
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	80	1544	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	1542	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	80	1516	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	500	1514	3	SINGLE BIT & BLOCKED CONTACT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	80	1517	1	LOST REJECT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	500	1511	2	SINGLE BIT
STRESS: LONG LIFE VERIFICATION, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	400	0	
STRESS: HIGH TEMPERATURE STEADY STATE LIFE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	80	80	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	168	80	0	
STRESS: HIGH TEMPERATURE STORAGE							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	50	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	50	0	

Reliability Test Data
QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	9	0	
CY7C1041D (7C1541N)	4538630	*610610603*	CML-R	COMP	9	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	9	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	9	0	
CY7C1041D (7C1541N)	4530733	*610607231*	CML-R	COMP	9	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	9	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	9	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	3	0	
CY7C1041D (7C1541N)	4530733	*610607231*	CML-R	COMP	3	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	3	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	3	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-200mA							
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	3	0	
CY7C1046DV33 (7C1346N)	4538680	*610610605*	CML-R	COMP	3	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-300mA							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	3	0	

Reliability Test Data
QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: STATIC LATCH-UP TESTING, 125C, 8.5V, +/-200mA							
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	3	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	3	0	
CY7C1041D (7C1541N)	4552229	*610617290*	CML-R	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	128	45	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	128	45	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	128	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	168	46	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	168	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	288	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	168	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	288	50	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	300	45	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	45	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	45	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	300	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	500	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	1000	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	300	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	500	50	0	

Reliability Test Data
QTP #: 080602

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	COMP	15	0	
CY7C1061DV33 (7C1061NC)	4646309	610706778	TAIWAN-G	COMP	15	0	
CY7C1062DV33 (7C1062NC)	4648234	610730021	TAIWAN-G	COMP	15	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 3.77V, Vcc Max							
CY7C1061DV33 (7C1061NC)	4801414	610809978N	TAIWAN-G	96	1415	0	
CY7C1061DV33 (7C1061NC)	4802871	610814485	TAIWAN-G	96	918	0	
CY7C1061DV33 (7C1061NC)	4802871	610814485N	TAIWAN-G	96	217	0	
CY7C1061DV33 (7C1061NC)	4802871	610814485N1	TAIWAN-G	96	444	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 3.77V, Vcc Max							
CY7C1061DV33 (7C1061NC)	4801414	610809978N	TAIWAN-G	168	199	0	
CY7C1061DV33 (7C1061NC)	4801414	610809978N	TAIWAN-G	1000	199	0	
CY7C1061DV33 (7C1061NC)	4802871	610814485R222	TAIWAN-G	168	200	0	
CY7C1061DV33 (7C1061NC)	4802871	610814485R222	TAIWAN-G	1000	200	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	COMP	9	0	
CY7C1062DV33 (7C1062NC)	4713292	0TAIWAN-G	COMP	9	0		
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V							
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	COMP	8	0	
CY7C1062DV33 (7C1062NC)	4713292	0TAIWAN-G	COMP	8	0		
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.65V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	128	45	0	
STRESS: HIGH TEMPERATURE STEADY STATE LIFE, 150C, 3.77V, Vcc Max							
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	168	80	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	168	45	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-200mA							
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	COMP	3	0	

Reliability Test Data
QTP #: 080602

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	300	45	0	
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	500	44	0	
CY7C1061DV33 (7C1061NC)	4641622	610673799	TAIWAN-G	1000	44	0	
CY7C1061DV33 (7C1061NC)	4646309	610706778	TAIWAN-G	300	45	0	
CY7C1062DV33 (7C1062NC)	4648234	610730021	TAIWAN-G	300	50	0	
CY7C1062DV33 (7C1062NC)	4648234	610730021	TAIWAN-G	500	50	0	
CY7C1062DV33 (7C1062NC)	4648234	610730021	TAIWAN-G	1000	45	0	

Document History Page

Document Title: QTP 080602: 16 MEG FAST ASYNCHRONOUS SRAM FAMILY, C9FD-3R TECHNOLOGY, FAB4
Document Number: 001-84625

Rev.	ECN No.	Orig. of Change	Description of Change
**	3810634	NSR	Initial Spec Release.
*A	4577861	JYF	Sunset review: Updated QTP title page and Reliability Tests Performed table (HAST,PCT,TCT,LLV,Acoustic) for template alignment.

Distribution: WEB

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