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Cypress Semiconductor
Product Qualification Report

QTP# 073907
June 2013

FULLFLEX™ 2M/4M/9M/18M SYNC SDR DUAL PORT SRAM C9FQ-3R TECHNOLOGY, FAB 4	
CYD18S72Vxx	256K x 72 (18M) SDR - 1.2/1.5/1.8V
CYD09S72Vxx	128K x 72 (9M) SDR - 1.2/1.5/1.8V
CYD04S72Vxx	64K x 72 (4M) SDR - 1.2V/1.5V/1.8V
CYD18S36Vxx	512K x 36 (18M) SDR -1.2/1.5/1.8V
CYD09S36Vxx	256K x 36 (9M) SDR -1.2/1.5/1.8V
CYD04S36Vxx	128K x 36 (4M) SDR -1.2V/1.5V/1.8V
CYD02S36Vxx	64K x 36 (2M) SDR -1.2V/1.5V/1.8V
CYD18S18Vxx	1024K x 18 (18M) SDR - 1.2/1.5/1.8V
CYD09S18Vxx	512K x 18 (9M) SDR -1.2/1.5/1.8V
CYD04S18Vxx	256K x 18 (4M) SDR -1.2V/1.5V/1.8V

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
073907	Qualify C9FQ-3R Technology and 9M/18M Sync DP Devices, Fab4	Oct 07
073907	Add 2M and 4M Devices Options of 9M C9 DP	Dec 07

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify C9FQ-3R Technology and 9M/18M Sync DP Devices, Fab4			
Marketing Part #:	CYD02S36V18/12*, CYD04S72V18/12*, CYD09S72V18/12*, CYD18S72V18/12*	CYD04S18V18/12*, CYD09S18V18/12*, CYD18S18V18/12*,	CYD04S36V18/12*, CYD09S36V18/12*, CYD18S36V18/12*,
Device Description:	1.2V, 1.5V, 1.8V 2M, 4M, 9M and 18M Dual Port SDR SRAM (Industrial and Commercial)		
Cypress Division:	Cypress Semiconductor Corporation –Memory and Imaging Division		

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	4	Metal Composition:	Metal 1: 100A Ti + 3200A Al + 300A TiW Metal 2: 100A Ti + 3200A Al + 300A TiW Metal 3: 150A Ti + 4230A Al + 300A TiW Metal 4: 150A Ti + 8000A Al + 300A TiW
Passivation Type and Materials:			TEOS oxide of 1000A + Nitride of 9000A
Number of Transistors in device			104 Million (2M, 4M, 9M),205 Million (18M)
Number of Gates in device			22 Million (2M, 4M, 9M), 42 Million (18M)
Generic Process Technology/Design Rule (µ-drawn):			CMOS, 100nm
Gate Oxide Material/Thickness (MOS):			20.5A for LVFETs and 58A for HVFETs (Dual Gate Oxide)
Name/Location of Die Fab (prime) Facility:			CMI / Bloomington MN
Die Fab Line ID/Wafer Process ID:			Fab4, C9FQ-3RP

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
484-PBGA **256-FBGA**	**ASE-TAIWAN (G)**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BY484
Package Outline, Type, or Name:	484- Plastic Ball Grid Array (PBGA)
Mold Compound Name/Manufacturer:	G770-J
Mold Compound Flammability Rating:	UL-94 V-0
Oxygen Rating Index:	N/A
Lead Frame Material:	N/A
Lead Finish, Composition / Thickness:	SnAgCu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	2100A
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-03554
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 0.9mil
Thermal Resistance Theta JA °C/W:	14.03
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41046
Name/Location of Assembly (prime) facility:	ASE –TAIWAN (G)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
TEST LOCATION :	ASE, TAIWAN, CHIPMOS

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BW256
Package Outline, Type, or Name:	256-Very Fine Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	G2270
Mold Compound Flammability Rating:	UL-94 V-0
Oxygen Rating Index:	N/A
Lead Frame Material:	N/A
Lead Finish, Composition / Thickness:	SnAgCu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	2025D
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-07866
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 0.9mil
Thermal Resistance Theta JA °C/W:	16.4
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41040
Name/Location of Assembly (prime) facility:	ASE –TAIWAN (G)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
TEST LOCATION :	ASE- TAIWAN, CHIPMOS

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max=2.07V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max=2.07V, 125°C	P
High Temperature Steady State life	125°C, 2.06V, Vcc Max	P
High Accelerated Saturation Test (HAST)	130°C, 1.80V, 85%RH Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2200V MIL-STD-883, Method 3015.7 JESD22, Method A114-B/E	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101C	P
Acoustic Microscopy	J-STD-020	P
Age Bond Strength	200°C, 4 HRS MIL-STD-883, Method 883-2011	P
Alpha Particle Emission	0.001 CPH/Cm^2	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Dynamic Latch-up	3.09V & 8.00V	P
High Temperature Storage	150C, no bias	P
Static Latch-up	125C, ± 200mA	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate
High Temperature Operating Life Early Failure Rate[1]	1,697	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	519,360	1	0 .7	55	70 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #:073907

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CYD18S72V18 (7C08642A)	4546070	610610519	G-TAIWAN	COMP	16	0	
CYD18S72V18 (7C08642A)	4619133	610653400	G-TAIWAN	COMP	15	0	
CYD18S72V18 (7C08642A)	4626844	610660831	G-TAIWAN	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CYD18S72V18 (7C08642A)	4606179	610628791	G-TAIWAN	COMP	3	0	
CYD18S72V18 (7C08642A)	4626844	610660831	G-TAIWAN	COMP	45	0	
CYD18S72V18 (7C08642A)	4619133	610653400	G-TAIWAN	COMP	45	0	
STRESS: ALPHA PARTICLE EMISSION							
CYD09S18V18 (7C08332A)	4620518	610733675	G-TAIWAN	COMP	3	0	
CYD18S72V18 (7C08642A)	4549164	610624646	G-TAIWAN	COMP	3	0	
STRESS: DYNAMIC LATCH-UP, 3.09V & 8.0V							
CYD18S72V18 (7C08642A)	4606179	610628791	G-TAIWAN	COMP	2	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CYD18S72V18 (7C08642A)	4546070	610610519	G-TAIWAN	COMP	9	0	
CYD09S72V18 (7C08632A)	4607581	610628568	G-TAIWAN	COMP	9	0	
CYD18S72V18 (7C08642A)	4619133	610653400	G-TAIWAN	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-E, 2200V							
CYD18S72V18 (7C08642A)	4546070	610610519	G-TAIWAN	COMP	9	0	
CYD09S72V18 (7C08632A)	4616967	610658346	G-TAIWAN	COMP	9	0	
CYD18S72V18 (7C08642A)	4619133	610653400	G-TAIWAN	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2200V							
CYD18S72V18 (7C08642A)	4546070	610610519	G-TAIWAN	COMP	3	0	
CYD09S72V18 (7C08632A)	4616967	610658346	G-TAIWAN	COMP	3	0	
CYD18S72V18 (7C08642A)	4619133	610653400	G-TAIWAN	COMP	3	0	

Reliability Test Data

QTP #:073907

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (125C, 2.07V, Vcc Max)							
CYD09S18V18 (7C08332A)	4620518	610733675	G-TAIWAN	96	487	0	
CYD09S18V18 (7C08332A)	4620518	610728531	G-TAIWAN	96	513	0	
CYD18S72V18 (7C08642A)	4701013	610727901	G-TAIWAN	96	325	0	
CYD18S36V18 (7C085426A)	4718234	610736293	G-TAIWAN	96	372	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (125C, 2.07V, Vcc Max)							
CYD09S18V18 (7C08332A)	4620518	610733675	G-TAIWAN	168	200	0	
CYD18S72V18 (7C08642A)	4701013	610727901	G-TAIWAN	168	324	1	NVD (Suspected Particle Defect)
CYD18S36V18 (7C085426A)	4718234	610736293	G-TAIWAN	168	371	0	
CYD09S36V25 (7C08534A)	4629026	610667807N	G-TAIWAN	1000	198	0	
CYD18S36V18 (7C08542A)	4627153	610701547	G-TAIWAN	1000	171	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST (125C, 2.06V)							
CYD18S72V18 (7C08642A)	4546070	610610519	G-TAIWAN	168	76	0	
CYD18S72V18 (7C08642A)	4546070	610610519	G-TAIWAN	336	74	0	
STRESS: HIGH TEMPERATURE STORAGE, 150C, no bias							
CYD18S72V18 (7C08642A)	4549164	610624646	G-TAIWAN	500	45	0	
CYD18S72V18 (7C08642A)	4549164	610624646	G-TAIWAN	1000	45	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 1.80V), PRE COND 192 HR, 30C/60%RH, MSL3							
CYD36S18V18 (7C08352A)	4625265	610662212	G-TAIWAN	128	46	0	
CYD18S72V18 (7C08642A)	4606179	610628791	G-TAIWAN	128	48	0	
CYD18S72V18 (7C08642A)	4619133	610653400	G-TAIWAN	128	44	0	
STRESS: STATIC LATCH-UP TESTING (125C, 5.40V, ±200mA)							
CYD09S72V18 (7C08632A)	4607581	610628568	G-TAIWAN	COMP	3	0	
CYD18S72V18 (7C08642A)	4606179	610628791	G-TAIWAN	COMP	3	0	
CYD18S72V18 (7C08642A)	4619133	610653400	G-TAIWAN	COMP	3	0	

Reliability Test Data

QTP #:073907

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS, 30C/60%RH, MSL3							
CYD18S36V25 (7C08544A)	4615663	610645172	G-TAIWAN300		45	0	
CYD18S36V25 (7C08544A)	4619133	610659447	G-TAIWAN300		48	0	
CYD09S72V18 (7C08632A)	4607581	610628568	G-TAIWAN300		47	0	
CYD18S72V18 (7C08642A)	4549164	610624646	G-TAIWAN300		47	0	
CYD18S72V18 (7C08642A)	4619133	610653400	G-TAIWAN300		49	0	

Document History Page

Document Title: QTP # 073907 : FULLFLEX™ 2M/4M/9M/18M SYNC SDR DUAL PORT SRAM C9FQ-3R TECHNOLOGY, FAB 4
Document Number: 001-87928

Rev.	ECN No.	Orig. of Change	Description of Change
**	4027064	ILZ	Initial Spec Release Qualification report published on Cypress.com is documented on memo HGA-260 and not in spec format. Initiated spec for QTP 073907 and data from Memo # HGA-260 was transferred to qualification report spec template. Updated package availability based on current qualified test & assembly site. Deleted Cypress reference Spec and replaced with Industry Standards. Deleted previous package assembly information and replaced with existing and qualified assembly site

Distribution: WEB

Posting: None