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# Cypress Semiconductor Product Qualification Report

**QTP # 072501 VERSION\*C**  
**May, 2015**

<b>72 Meg QDR Synchronous SRAM Family</b> <b>R9Q-3R Technology, Fab4</b>	
CY7C1510JV18 CY7C1525JV18 CY7C1512JV18 CY7C1514JV18	72-Mbit QDR™-II SRAM 2-Word Burst Architecture (1.5 Cycle Read Latency)
CY7C1511JV18 CY7C1526JV18 CY7C1513JV18 CY7C1515JV18	72-Mbit QDR™-II SRAM 4-Word Burst Architecture (1.5 Cycle Read Latency)
CY7C1516JV18 CY7C1527JV18 CY7C1518JV18 CY7C1520JV18	72-Mbit DDR-II SRAM 2-Word Burst Architecture (1.5 Cycle Read Latency)
CY7C1517JV18 CY7C1528JV18 CY7C1519JV18 CY7C1521JV18	72-Mbit DDR-II SRAM 4-Word Burst Architecture (1.5 Cycle Read Latency)
CY7C1522JV18 CY7C1529JV18 CY7C1523JV18 CY7C1524JV18	72-Mbit DDR-II SRAM Separate I/O Architecture (1.5 Cycle Read Latency)
CY7C1540V18 CY7C1555V18 CY7C1542V18 CY7C1544V18	72-Mbit QDR™-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1541V18 CY7C1556V18 CY7C1543V18 CY7C1545V18	72-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1546V18 CY7C1557V18 CY7C1548V18 CY7C1550V18	72-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1547V18 CY7C1558V18 CY7C1549V18 CY7C1551V18	72-Mbit DDR-II+ SRAM 4-Word Burst Architecture (2.0 Cycle Read Latency)
CY7C1552V18 CY7C1559V18 CY7C1553V18 CY7C1554V18	72-Mbit DDR-II+ SRAM Separate I/O Architecture (2.0 Cycle Read Latency)
CY7C1560V18 CY7C1575V18 CY7C1562V18 CY7C1564V18	72-Mbit QDR™-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)

## 72 Meg QDR Synchronous SRAM Family

### R9Q-3R Technology, Fab4

CY7C1561V18 CY7C1576V18 CY7C1563V18 CY7C1565V18	72-Mbit QDR™-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1566V18 CY7C1577V18 CY7C1568V18 CY7C1570V18	72-Mbit DDR-II+ SRAM 2-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1567V18 CY7C1578V18 CY7C1569V18 CY7C1571V18	72-Mbit DDR-II+ SRAM 4-Word Burst Architecture (2.5 Cycle Read Latency)
CY7C1572V18 CY7C1579V18 CY7C1573V18 CY7C1574V18	72-Mbit DDR-II+ SRAM Separate I/O Architecture (2.5 Cycle Read Latency)

**FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT**  
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## PRODUCT QUALIFICATION HISTORY

<b>QTP Number</b>	<b>Description of Qualification Purpose</b>	<b>Date</b>
<b>033302</b>	<b>New Technology R9T-3R, Fab 4, and New Device CY7C137*/138*E (18Meg) Synchronous product family</b>	<b>Sept 04</b>
<b>051207</b>	<b>R9 18 Meg QDR, 7C1313D 4 Metal Layer Process</b>	<b>Mar 05</b>
<b>051901</b>	<b>New Device CY7C151*/7C152* AC (72Meg QDR/DDR/LW) Device Family, R9Q-3R Technology fabricated at Fab4</b>	<b>May 05</b>
<b>072501</b>	<b>RAM9Q-3R QDRII Qualification for Fab4 smaller or same base die area density</b>	<b>Sep 07</b>
<b>083816</b>	<b>R9 7C1553BC 72M QDRII+ Fast A1 and Output Register Noise and Decoupling Design Fix Mask Qualification</b>	<b>Jan 09</b>

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

### PRODUCT DESCRIPTION (for qualification)

Qualification Purpose: Qualify 7C1553AC base die, 72Meg QDR2 Synchronous product family in R9Q-3R Technology, Fab4

Marketing Part #: 510/2/4/25JV18, CY7C1511/3/5/26JV18, CY7C1516/8/20/27JV18, CY7C1517/9/21/28JV18, CY7C1522/3/4/9JV18, CY7C1540/2/4/55V18, CY7C1541/3/5/56V18, CY7C1546/8/50/57V18, CY7C1547/9/51/58V18, CY7C1552/3/4/9V18, CY7C1560/2/4/75V18, CY7C1561/3/5/76V18, CY7C1566/68/70/77V18, CY7C1567/9/71/78V18, CY7C1572/3/4/9V18

Device Description: 1.8V Commercial and Industrial available in 165-Ball FBGA

Cypress Division: Semiconductor Corporation –Memory Product Division

### TECHNOLOGY/FAB PROCESS DESCRIPTION

Number of Metal Layers:	4	Metal Composition:	Metal 1: 150Å Ti / 3200Å Al / 300Å TiW Metal 2: 150Å Ti / 6000 Å Al / 300Å TiW Metal 3: 150Å Ti / 6000Å Al / 300Å TiW Metal 4: 150Å Ti / 8000Å Al / 300Å TiW
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Passivation Type and Thickness: 1000Å Oxide TEOS / 9000Å Nitride

Generic Process Technology/Design Rule ( $\mu$ -drawn): CMOS, Quad Metal, 90 nm

Gate Oxide Material/Thickness (MOS): Nitridized SiO<sub>2</sub>, Thin GOX 20A, Thick GOX, 58A

Name/Location of Die Fab (prime) Facility: Cypress Semiconductor -- Bloomington, MN

Die Fab Line ID/Wafer Process ID: Fab4/R9Q-3R

### PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
165-Ball FBGA	ASE-Taiwan (G)

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BB165
Package Outline, Type, or Name:	165-Ball Thin Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	KE-G2270 / Kyocera
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	None
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	SnPb, SnAgCu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	100% Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	2025D
Die Attach Method:	Epoxy
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au. 1.0mil
Thermal Resistance Theta JA °C/W:	17.56
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-06518
Name/Location of Assembly (prime) facility:	ASE Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Chipmos

**Note:** Please contact a Cypress Representative for other package availability.

## RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	AEC-Q100-008 and JESD22-A108 Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 125°C Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 150°C	P
High Temperature Operating Life Latent Failure Rate	JESD22-A108 Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 125°C Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 150°C	P
High Temperature Steady State Life	JESD22-A108 Static Operating Condition, Vcc Max= 2.25V, 150°C	P
Low Temperature Operating Life	JESD22-A108 Dynamic Operating Condition, Vcc = 6.50V, -30°C	P
High Accelerated Saturation Test (HAST)	JESD22-A110 130°C, 3.63V,85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+ Reflow, 260°C+0, -5°C	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+Reflow, 260°C+0, -5°C 192 Hrs, 30°C/60%RH+Reflow, 220°C+0, -5°C	P
Pressure Cooker	JESD22-A102 121°C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+Reflow, 260°C+0, -5°C 192 Hrs, 30°C/60%RH+Reflow, 220°C+0, -5°C	P
High Temperature Storage	JESD22-A103 150°C ± 5°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-A101	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	JEDEC JSTD-020	P
Dynamic Latchup	In accordance with JEDEC 17	P
Static Latchup	125C, ± 200mA In accordance with JEDEC 17	P

## RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF <sup>3</sup>	Failure Rate
High Temperature Operating Life Early Failure Rate	3,731 Devices	1	N/A	N/A	268 PPM
High Temperature Operating Life <sup>1,2</sup> Long Term Failure Rate	485, 000 DHRs	0	0.7	170	7 FIT
High Temperature Operating Life <sup>1,2</sup> Long Term Failure Rate	1,049,548 DHRs	0	0.7	55	

<sup>1</sup> Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

<sup>2</sup> Chi-squared 60% estimations used to calculate the failure rate.

<sup>3</sup> Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp \left[ \frac{E_A}{k} \left[ \frac{1}{T_2} - \frac{1}{T_1} \right] \right]$$

where:

$E_A$  = The Activation Energy of the defect mechanism.

$K$  = Boltzmann's constant =  $8.62 \times 10^{-5}$  eV/Kelvin.

$T_1$  is the junction temperature of the device under stress and  $T_2$  is the junction temperature of the device at use conditions.





## Reliability Test Data

### QTP #:033302

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: ACOUSTIC, MSL3</b>							
CY7C1470V33 (7C1470A)	4330156	610417279	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4321389	610417280	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4323794	610348235	TAIWN-G	COMP	15	0	
<b>STRESS: AGE BOND STRENGTH</b>							
CY7C1370DV33 (7C1370E)	4421235	610447674	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4406200	610435906	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4410258	610437891	CML-R	COMP	5	0	
<b>STRESS: BALL SHEAR</b>							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	10	0	
<b>STRESS: BOND PULL</b>							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	10	0	
<b>STRESS: DYNAMIC LATCH-UP</b>							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	3	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V</b>							
CY7C1470V33 (7C1470A)	4352888	610425832	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	610425833	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	610417723	CML-R	COMP	3	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V</b>							
CY7C1470V33 (7C1470A)	4352888	610425832	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	610425833	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4345377	610417723	CML-R	COMP	9	0	
<b>STRESS: ESD-CHARGE DEVICE MODEL, 500V</b>							
CY7C1470V33 (7C1470A)	4352888	610425832	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	610425833	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4345377	610417723	CML-R	COMP	9	0	
<b>STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C</b>							
CY7C1470V33 (7C1470A)	4323794	610348234	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	610348234	TAIWN-G	1000	47	0	



## Reliability Test Data QTP #:033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)</b>							
CY7C1370DV33 (7C1370E)	4345377	610424939	CML-R	48	193	0	
CY7C1370DV33 (7C1370E)	4345377	610422227	CML-R	48	951	0	
CY7C1370DV33 (7C1370E)	4406200	610435906	CML-R	48	1246	0	
CY7C1370DV33 (7C1370E)	4410258	610437891	CML-R	48	1382	1	Non-Visual (033302-3E1)
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Max (Core)</b>							
CY7C1370DV33 (7C1370E)	4345377	610424939	CML-R	500	170	0	
CY7C1370DV33 (7C1370E)	4406200	610435906	CML-R	500	400	0	
CY7C1370DV33 (7C1370E)	4410258	610437891	CML-R	500	400	0	
<b>STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max</b>							
CY7C1470V33 (7C1470A)	4405088	610418824	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	610418824	TAIWN-G	168	85	0	
<b>STRESS: INTERNAL VISUAL</b>							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	5	0	
<b>STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.50V, Vcc</b>							
CY7C1470V33 (7C1470A)	4333765	610349455	CML-R	500	45	0	
<b>STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3</b>							
CY7C1370DV33 (7C1370E)	4345377	610422227	CML-R	168	50	0	
CY7C1370DV33 (7C1370E)	4406200	610435906	CML-R	168	50	0	
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	168	43	0	
<b>STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3</b>							
CY7C1370DV33 (7C1370E)	4406200	610435906	CML-R	128	50	0	
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	128	47	0	
CY7C1470V33 (7C1470A)	4330156	610417279	CML-R	128	44	0	
<b>STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/-300mA</b>							
CY7C1470V33 (7C1470A)	4352888	610425832	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	610425833	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	610417723	CML-R	COMP	3	0	



## Reliability Test Data

### QTP #:033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3</b>							
CY7C1370DV33 (7C1370E)	4345377	610422227	CML-R	300	50	0	
CY7C1370DV33 (7C1370E)	4345377	610422227	CML-R	500	49	0	
CY7C1370DV33 (7C1370E)	4345377	610422227	CML-R	1000	49	0	
CY7C1470V33 (7C1470A)	4330156	610417279	CML-R	300	43	0	
CY7C1470V33 (7C1470A)	4330156	610417279	CML-R	500	43	0	
CY7C1470V33 (7C1470A)	4330156	610417279	CML-R	1000	42	0	
CY7C1470V33 (7C1470A)	4321389	610417280	CML-R	300	34	0	
CY7C1470V33 (7C1470A)	4321389	610417280	CML-R	500	33	0	
CY7C1470V33 (7C1470A)	4321389	610417280	CML-R	1000	33	0	
<b>STRESS: THERMAL SHOCK</b>							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	100	46	0	
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	200	46	0	
<b>STRESS: X-RAY</b>							
CY7C1470V33 (7C1470A)	4321389	610417278	CML-R	COMP	15	0	



## Reliability Test Data

**QTP #:051207**

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
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**STRESS: ESD-CHARGE DEVICE MODEL, 500V**

CY7C1314BV18 (7C1314D)	4444085	610507866	TAIWN-G	COMP	9	0	
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**STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V**

CY7C1314BV18 (7C1314D)	4444085	610507866	TAIWN-G	COMP	9	0	
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**STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V**

CY7C1314BV18 (7C1314D)	4444085	610507866	TAIWN-G	COMP	3	0	
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**STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.25V, Vcc Max (Core)**

CY7C1312BV18 (7C1312D)	4440030	610465503	TAIWN-G	96	1803	0	
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**STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 2.25V, Vcc Max (Core)**

CY7C1312BV18 (7C1312D)	4440030	610465503	TAIWN-G	168	1395	0	
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CY7C1312BV18 (7C1312D)	4440030	610465503	TAIWN-G	500	359	0	
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**STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3**

CY7C1313BV18 (7C1313D)	4436152	610459993	TAIWN-G	168	50	0	
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CY7C1313BV18 (7C1313D)	4436152	610459993	TAIWN-G	288	50	0	
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**STRESS: STATIC LATCH-UP TESTING, 125C, 4.5V, +/-300mA**

CY7C1314BV18 (7C1314D)	4444085	610507866	TAIWN-G	COMP	3	0	
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**STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3**

CY7C1313BV18 (7C1313D)	4436152	610459993	TAIWN-G	300	50	0	
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CY7C1313BV18 (7C1313D)	4436152	610459993	TAIWN-G	500	50	0	
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CY7C1313BV18 (7C1313D)	4436152	610459993	TAIWN-G	1000	50	0	
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## Reliability Test Data

### QTP #:051901

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: ESD-CHARGE DEVICE MODEL, 500V</b>							
CY7C1514V18 (7C1514A)	4412759	610452856	TAIWN-G	COMP	9	0	
CY7C1515V18 (7C1515A)	4347629	610436891	TAIWN-G	COMP	9	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V</b>							
CY7C1512V18 (7C15121A)	4406161	610437889	TAIWN-G	COMP	3	0	
CY7C1515V18 (7C1515A)	4347629	610436891	TAIWN-G	COMP	3	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V</b>							
CY7C1512V18 (7C15121A)	4406161	610437889	TAIWN-G	COMP	9	0	
CY7C1515V18 (7C1515A)	4347629	610436891	TAIWN-G	COMP	6	0	
CY7C1514V18 (7C1514A)	4412759	610452856	TAIWN-G	COMP	6	0	
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.25V, Vcc Max (Core)</b>							
CY7C1512V18 (7C15121A)	4451052	610510951	TAIWN-G	96	1613	0	
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 2.25V, Vcc Max (Core)</b>							
CY7C1512V18 (7C15121A)	4425371	61059092	TAIWN-G	168	862	0	
CY7C1512V18 (7C15121A)	4425371	61059092	TAIWN-G	500	612	0	
CY7C1512V18 (7C15121A)	4422351	61059094	TAIWN-G	168	696	0	
CY7C1512V18 (7C15121A)	4422351	61059094	TAIWN-G	500	696	0	
<b>STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3</b>							
CY7C1512V18 (7C15121A)	4413923	610445193	TAIWN-G	168	48	0	
CY7C1512V18 (7C15121A)	4413923	610445193	TAIWN-G	288	48	0	
<b>STRESS: STATIC LATCH-UP TESTING, 125C, 5.0V, +/-300mA</b>							
CY7C1512V18 (7C15121A)	4406161	610437889	TAIWN-G	COMP	3	0	
<b>STRESS: STATIC LATCH-UP TESTING, 125C, 5.5V, +/-300mA</b>							
CY7C1515V18 (7C1515A)	4347629	610436891	TAIWN-G	COMP	6	0	
<b>STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3</b>							
CY7C1512V18 (7C15121A)	4413923	610445193	TAIWN-G	300	48	0	
CY7C1512V18 (7C15121A)	4413923	610445193	TAIWN-G	500	48	0	
CY7C1512V18 (7C15121A)	4413923	610445193	TAIWN-G	1000	48	0	



## Reliability Test Data

**QTP #:072501**

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
<b>STRESS: ESD-CHARGE DEVICE MODEL, 500V</b>							
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	COMP	9	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V</b>							
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	COMP	3	0	
<b>STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114, 2,200V</b>							
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	COMP	9	0	
<b>STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.25V, Vcc Max (Core)</b>							
CY7C1565AC (7C1565AC)	4709084	610724209	TAIWN-G	96	1682	1	Single bit, non-visual (072501-4E1)
CY7C1565AC (7C1565AC)	4724391	610743432	TAIWN-G	48	1499	0	
CY7C1565AC (7C1565AC)	4724391	610743432	TAIWN-G	96	1499	0	
CY7C1520 (7C1520JC)	4713527	610738770	TAIWN-G	48	550	0	
CY7C1520 (7C1520JC)	4713527	610738770	TAIWN-G	96	550	0	
<b>STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3</b>							
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	168	47	0	
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	288	47	0	
<b>STRESS: STATIC LATCH-UP TESTING, 125C, 3.0V, +/-200mA</b>							
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	COMP	3	0	
<b>STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3</b>							
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	300	46	0	
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	500	45	0	
CY7C1565AC (7C1565AC)	4551740	610613815N1	TAIWN-G	1000	44	0	



## Reliability Test Data

**QTP #: 083816**

<i>Device</i>	<i>Fab Lot #</i>	<i>Assy Lot #</i>	<i>Assy Loc</i>	<i>Duration</i>	<i>Samp</i>	<i>Rej</i>	<i>Failure Mechanism</i>
<b>STRESS: E-TEST YIELD</b>							
7C1553BC	4836288	N/A	N/A	COMPARABLE			
<b>STRESS: SORT YIELD</b>							
7C1553BC	4836288	N/A	N/A	COMPARABLE			

## Document History Page

Document Title: 72-MBIT DDR/QDR(TM)-II SRAM 2/4-WORD BURST ARCHITECTURE (1.5/2.0 CYCLE READ LATENCY) QUALIFICATION REPORT

Document Number: 001-60011

Rev.	ECN No.	Orig. of Change	Description of Change
**	2888833	NSR	Initial Spec Release
*A	3977872	JYF	<p>Removed Versions 2.1 in QTP# 072501 title page;</p> <p>Updated division of device from "Memory &amp; Image Division" to "Memory Product Division" in Product Description Table;</p> <p>Deleted bond diagram designation specs 001-06654 and 001-07655 in Major Package Information Table. Specs have been obsoleted since 7C1565A device using BB/BW165 (device used during QTP) are no longer in prodtree;</p> <p>Updated Reliability Test Performed Table:</p> <ul style="list-style-type: none"> <li>- Included referenced industry standards of HTOL, HTSSL, HAST, PCT, HTS, ESD-CDM and Acoustic Microscopy.</li> <li>- Deleted revisions of Jedec standards on ESD-HBM and TCT. Revision changes from time to time.</li> <li>- Deleted Cypress' referenced specs 25-00020, 22-00029, 25-00104 and 001-00081</li> <li>- Deleted Current Density, internal requirement only</li> </ul>
*B	4362946	JYF	<p>Sunset review:</p> <p>Updated QTP title page for template alignment.</p>
*C	4752691	JYF	<p>Sunset review:</p> <p>Updated reference for Reliability Director.</p>

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