Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Cypress Semiconductor
Product Qualification Report

QTP# 064203
June 2013

CSM 0.35um LOGIC SALICIDE CHARTER SEMICONDUCTOR	
CY2CC810 **CY2CC910**	**1:10 CLOCK FANOUT BUFFER**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

Zhaomin Ji
Principal Reliability Engineer
(408) 432-7021

Mira Ben-Tzur
Quality Engineering Director
(408) 943-2675

PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
I000006	Qualification Summary for Cypress Acquisition of IMI Devices and Packages (Feb. 23, 2001)	Feb 03
I000006	Added new device data gathered, B35C qualified base die (CY2LL843*, CY2SSTV16859*,CY2AVC16835*)	May 04
064203	Metal mask change to B35C09A bond option	Dec 06

DIE QUALIFICATION TEST RESULTS

B35C base die platform (0.35 uM, 3 layers metal, CMOS, CSM-Singapore)

Test	Military or Industry Standard	Conditions	Test Points	Test Results	Comments
Life Test	MIL-STD-883 Method 1005	125^{o}C/5V	500 1000	0/116 0/116	Lot C1035-B35C
Life Test	MIL-STD-883 Method 1005	125^{o}C/5V	500 1000	0/116 0/116	Lot C1035-B35C
ESD	MIL-STD-883 Method 3015	HBM	2000V 3000V 4000V 5000V	0/3 0/3 0/3 3/3	Lot C1035-B35C
Latch-up	JESD78		200 mA	0/5	Lot C1035-B35C

PACKAGE QUALIFICATION TEST RESULTS

SSOP ,0.295 wide

Test	Military or Industry Standard	Conditions	Test Points	Test Results	Comments
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{o}C	500	0/76	Preconditioned Units, OSE, lot C1138
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{o}C, 2 atm	168	0/76	Preconditioned Units, OSE, lot C1138
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{o}C	500	0/76	Preconditioned Units, OSE, lot C1035
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{o}C, 2 atm	168	0/76	Preconditioned Units, OSE, lot C1035
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{o}C	500	0/76	Preconditioned Units, OSE, lot C1009
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{o}C, 2 atm	168	0/76	Preconditioned Units, OSE, lot C1009
Temperature Cycle	MIL-STD-883 Method 1010	50 hours /5V,130^{o}C, 85%RH	50	0/76	Preconditioned Units, OSE, lot C1009
Pressure Pot	JEDEC Std. 22 Test Method 102	1000 Hours, 85% RH, 85^{o}C,	1000	0/76	Preconditioned Units, OSE, lot C1009
Temperature Cycle	MIL-STD-883 Method 1010	500 cycles, -65/+ 150^{o}C	500	0/76	Preconditioned Units, CWT, lot T2706
Pressure Pot	JEDEC Std. 22 Test Method 102	168 Hours, 100% RH, 121^{o}C, 2 atm	168	0/76	Preconditioned Units, CWT, lot T2706
Physical Dimension	JEDEC Spec.	Applicable drawing	N/A	0/12	Performed by OSE
Resistance to Solvent	MIL-STD-883 Method 2015		N/A	0/12	Performed by OSE
Solderability	MIL-STD-883 Method 2003	260 Deg, 5 sec 95% Min Coverage	N/A	0/5	Performed by OSE
Coplanarity	JEDEC Spec.	Max = 4 Mil	N/A	0/20	Performed by OSE
Physical Dimension	JEDEC Spec.	Applicable drawing	N/A	0/12	Performed by CWT
Resistance to Solvent	MIL-STD-883 Method 2015		N/A	0/12	Performed by CWT
Solderability	MIL-STD-883 Method 2003	260 Deg, 5 sec 95% Min Coverage	N/A	0/5	Performed by CWT
Coplanarity	JEDEC Spec.	Max = 4 Mil	N/A	0/20	Performed by CWT

Reliability Test Data

B35C BASE DIE

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY2SSTV16859 (7C826859A)	9210123	*610334679*	KOREA-L	COMP	2	0	
CY2AVC16835 (7C81635ER)	9202732	*610303336*	TAIWAN-T	COMP	2	0	
CY2SSTV16859 (7C826859A)	9210123	*610249055*	KOREA-GQ	COMP	3	0	
CY2LL843 (7C82LL843CR)	9213233	*610218031*	TAIWAN-CH	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL, 750V							
CY2SSTV16859 (7C826859A)	9210123	*610334679*	KOREA-L	COMP	1	0	
CY2SSTV16859 (7C826859A)	9210123	*610249055*	KOREA-GQ	COMP	3	0	
CY2LL843 (7C82LL843CR)	9213233	*610218031*	TAIWAN-CH	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 1100V							
CY2SSTV16859 (7C826859A)	9210123	*610334679*	KOREA-L	COMP	1	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2000V							
CY2AVC16835 (7C81635ER)	9202732	*610303336*	TAIWAN-T	COMP	2	0	
CY2LL843 (7C82LL843CR)	9213233	*610218031*	TAIWAN-CH	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2200V							
CY2SSTV16859 (7C826859A)	9210123	*610334679*	KOREA-L	COMP	2	0	
CY2AVC16835 (7C81635ER)	9202732	*610303336*	TAIWAN-T	COMP	2	0	
CY2SSTV16859 (7C826859A)	9210123	*610249055*	KOREA-GQ	COMP	3	0	
CY2LL843 (7C82LL843CR)	9213233	*610218031*	TAIWAN-CH	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2400V							
CY2AVC16835 (7C81635ER)	9202732	*610303336*	TAIWAN-T	COMP	2	0	
CY2SSTV16859 (7C826859A)	9210123	*610249055*	KOREA-GQ	COMP	3	0	
CY2LL843 (7C82LL843CR)	9213233	*610218031*	TAIWAN-CH	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.0V, ±300mA							
CY2SSTV16859 (7C826859A)	9210123	*610334679*	KOREA-L	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, ±300mA							
CY2AVC16835 (7C81635ER)	9202732	*610303336*	TAIWAN-T	COMP	2	0	
CY2SSTV16859 (7C826859A)	9210123	*610249055*	KOREA-GQ	COMP	2	0	
CY2LL843 (7C82LL843CR)	9213233	*610218031*	TAIWAN-CH	COMP	3	0	

Reliability Test Data

QTP# 064203

Device	*Fab Lot #*	*Assy Lot #*	*Assy Loc*	*Duration*	*Samp*	*Rej*	*Failure Mechanism*
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY2CC810OI-1 (7C8C810A)	8635004	*610663117*	TAIWAN-T	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V							
CY2CC810OI-1 (7C8C810A)	8635004	*610663117*	TAIWAN-T	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY2CC810OI-1 (7C8C810A)	8635004	*610663117*	TAIWAN-T	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, **±200mA**							
CY2CC810OI-1 (7C8C810A)	8635004	*610663117*	TAIWAN-T	COMP	3	0	

Document History Page

Document Title: QTP # 064203 : CSM 0.35um LOGIC SALICIDE (CY2CC810/CY2CC910), CHARTER SEMICONDUCTOR
Document Number: 001-87923

Rev.	ECN No.	Orig. of Change	Description of Change
**	4026939	ILZ	Initial Spec Release Qualification report published on Cypress.com is documented on memo LGQ-636 and not in spec format. Initiated spec for QTP 064203 and data from LGQ-636 was transferred to qualification report spec template.

Distribution: WEB

Posting: None