Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Cypress Semiconductor
Product Qualification Report

QTP# 063901 VERSION *B
April 2015

16 Meg MoBL Devices RAM8NLD-1.8V, GSMC (Fab 5)	
CY62165DV18 MoBL® CY62165DV30 MoBL®	16-Mb (1M x 16) Static RAM Die
CY62167DV18 MoBL2™	16M (1024K x 16) Static RAM
CY62167DV20 MoBL2®	16-Mb (1024K x 16) Static RAM
CY62167DV30 MoBL® CY62167DG30 MoBL®	16-Mbit (1M x 16) Static RAM
CY62168DV30 MoBL®	16-Mbit (2M x 8) MoBL® Static RAM
CY62177DV30 MoBL®	32-M (2M X 16) STATIC RAM

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
reliability@cypress.com or via a CYLINK CRM CASE

Prepared By:
Honesto Sintos
Reliability Engineer

Reviewed By:
Zhaomin Ji
Reliability Manager

Approved By:
Don Darling
Reliability Director

PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
063901	Qualify 16Meg, MoBL Static RAM CY62167DV* device and family on RAM8NLD-1.8 Technology at GSMC Foundry (Fab 5)	Mar 07
070203	Full Qualification of GSMC AMAT PSG Tool using 16M MoBL SRAM, R8NLD-18 Technology	Mar 07
071203	R8NLD-18 process change (LICM1) at GSMC	May 07
083301	Qualify MM2 minor mask-change for RAM8 16M MoBL family (7G62161DK/ 7C62161DC/7C62171D) fabricated at Fab5	Nov 08

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify CY62167DV* device and family, RAM8NLD-1.8 Technology at GSMC (Fab 5)	
Marketing Part #:	CY62165/7DV18, CY62167DV20, CY62167/8DV30, CY62167DG30, CY62177DV30*
Device Description:	1.8V - 3V, Industrial available in 48-ball FBGA and 48-Lead TSOP
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION – RAM8NLD-1.8			
Number of Metal Layers:	2	Metal Composition	Metal 1: 150 Å Ti/250 Å TiN/3500 Å Al Metal 2: 300 Å Ti/200 Å TiN/4500 Å Al/500 Å TiN
Passivation Type and Materials:		1000Å TEOS / 9000Å Si3N4	
Generic Process Technology/Design Rule (µ-drawn):		0.13 µm	
Gate Oxide Material/Thickness (MOS):		32Å	
Name/Location of Die Fab (prime) Facility:		Grace Semiconductor-China	
Die Fab Line ID/Wafer Process ID:		Fab5/RAM8NLD-1.8V	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
48-Ball FBGA	**TAIWAN-G, CML-RA**
48-Pin TSOP	**TAIWAN-G**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION		
Package Designation:	BA48	
Package Outline, Type, or Name:	48-Ball Fine Pitch Ball Grid Array (VFBGA)	
Mold Compound Name/Manufacturer:	KE-G2270	
Mold Compound Flammability Rating:	V-O per UL94	
Oxygen Rating Index:	NA	
Substrate Material:	BT Resin	
Lead Finish, Composition / Thickness:	SnPb	SnAgCu
Die Backside Preparation	Backgrind	
Die Separation Method:	100%	
Die Attach Supplier:	Ablestik	
Die Attach Material:	Ablestik 2025D	
Die Attach Method:	Epoxy	
Bond Diagram Designation:	10-06162	10-07075
Wire Bond Method:	Thermosonic	
Wire Material/Size:	Au. 1.0mil	Au. 0.8mil
Thermal Resistance Theta JA °C/W:	28.37 °C/W	
Package Cross Section Yes/No:	N/A	
Assembly Process Flow:	49-41032	001-06964
Name/Location of Assembly (prime) facility:	Taiwan-G	CML-RA
MSL Level	3	
Reflow Profile	220C	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	**CML-R**

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.35V, 125°C	**P**
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 2.35V, 150°C	**P**
High Temperature Steady State Life Test	Static Operating Condition, Vcc Max = 2.35V, 150°C	**P**
Low Temperature Operating Life Test	Dynamic Operating Condition, Vcc Max = 2.35V, -30°C	**P**
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110: 130C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH, 220 ºC Reflow	**P**
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65 ºC to 150 ºC Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH, 220 ºC Reflow	**P**
Pressure Cooker	JESD22-A102: 121 ºC , 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH, 220 ºC Reflow	**P**
Acoustic Microscopy	J-STD-020	**P**
Age Bond	MIL-STD 883, Method 2011	**P**
Current Density	Meets the Technology Device Level Reliability Specifications	**P**
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114-B	**P**
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	**P**
High Temperature Storage	JESD22-A103, 150 ºC, no bias	**P**
Static Latch-up	125C, ± 200mA/ ± 140mA JESD78B	**P**

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF [1,3]	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	8,552 Devices	2	N/A	N/A	234 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate	642,500 DHRs	0	0.7	169	8 FITs

[1] Assuming an ambient temperature of 55ºC and a junction temperature rise of 15 ºC.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation
[4] Fit rate calculation based on limited sample size and device hours

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 063901

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	COMP	15	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	COMP	15	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	COMP	15	0	
STRESS: AGE BOND							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	COMP	10	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	COMP	10	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	COMP	10	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	COMP	9	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	COMP	9	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	COMP	8	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	COMP	8	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	COMP	8	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.35V, Vcc Max							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	96	1540	1	LICON-Poly Narrow Spacing[1]
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	96	961	0	
CY62167DV30LL (7G62162DK)	9650743	*610675324*	*TAIWN-G*	96	257	0	
CY62167DV30LL (7G62162DK)	9650743	*610703289*	*TAIWN-G*	96	252	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	96	996	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	96	812	1	Particle Defect[2]

1. CAR#200710021.1- process fix to increase LICON-Poly space, QTP# 071203 passed EFR and objective spec audit.

2. CAR# 200710033.1 – test program improvement to screen out random particle defect.

Reliability Test Data

QTP #: 063901

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.35V, Vcc Max							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	80	500	0	
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	500	500	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	80	495	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	500	491	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	500	150	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.35V, Vcc Max							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	80	80	0	
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	168	80	0	
STRESS: LOW TEMPERATURE OPERATING LIFE TEST, -30C, 2.35V, Vcc Max							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	500	45	0	
STRESS: HIGH TEMPERATURE STORAGE, 150C, no bias							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	500	50	0	
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	1000	50	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.6V, PRE COND 192 HR 30C/60%RH, MSL3							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	128	44	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	128	44	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	128	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	168	44	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	168	45	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	288	45	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	168	48	0	

Reliability Test Data

QTP #: 063901

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	300	43	0	
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	500	43	0	
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	1000	43	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	300	43	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	500	43	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	1000	43	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	300	44	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	500	44	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, ±200mA							
CY62167DV30LL (7G62162DK)	9649742	*610673573*	*TAIWN-G*	COMP	3	0	
CY62167DV30LL (7G62162DK)	9650743	*610675172*	*TAIWN-G*	COMP	3	0	
CY62167DV30LL (7G62162DK)	9703749	*610704375*	*TAIWN-G*	COMP	3	0	

Reliability Test Data

QTP #: 070203

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62167DV30LL (7G62162DK)	9703749	*610704374*	*TAIWN-G*	COMP	9	0	
CY62167DV30LL (7G62162DK)	9705754	*610706804*	*TAIWN-G*	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY62167DV30LL (7G62162DK)	9703749	*610704374*	*TAIWN-G*	COMP	8	0	
CY62167DV30LL (7G62162DK)	9705754	*610706804*	*TAIWN-G*	COMP	8	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.35V, Vcc Max							
CY62167DV30LL (7G62162DK)	9703749	*610704374*	*TAIWN-G*	96	1504	0	
CY62167DV30LL (7G62162DK)	9705754	*610706804*	*TAIWN-G*	96	1499	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.35V, Vcc Max							
CY62167DV30LL (7G62162DK)	9703749	*610704374*	*TAIWN-G*	500	144	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 1.98V, PRE COND 192 HR 30C/60%RH, MSL3							
CY62167DV30LL (7G62162DK)	9703749	*610704374*	*TAIWN-G*	128	44	0	
CY62167DV30LL (7G62162DK)	99705754	*610706804*	*TAIWN-G*	128	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY62167DV30LL (7G62162DK)	9703749	*610704374*	*TAIWN-G*	168	79	0	
CY62167DV30LL (7G62162DK)	9705754	*610706804*	*TAIWN-G*	168	77	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY62167DV30LL (7G62162DK)	9703749	*610704374*	*TAIWN-G*	500	78	0	
CY62167DV30LL (7G62162DK)	9703749	*610704374*	*TAIWN-G*	1000	77	0	
CY62167DV30LL (7G62162DK)	9705754	*610706804*	*TAIWN-G*	500	76	0	
CY62167DV30LL (7G62162DK)	9705754	*610706804*	*TAIWN-G*	1000	68	0	

Reliability Test Data

QTP #: 071203

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.35V, Vcc Max							
CY62167DV30LL (7G62162DK)	9709761	*610714797*	*TAIWAN-G*	96	731	0	

Reliability Test Data

QTP #: 083301

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: E-TEST YIELD							
CY62177DV30 (7C62171D)	4829459	N/A	N/A	COMPARABLE			
CY62167DV30 (7C62161D)	4833178	N/A	N/A	COMPARABLE			
CY62167DV30 (7G62161D)	4835716	N/A	N/A	COMPARABLE			
STRESS: SORT YIELD							
CY62177DV30 (7C62171D)	4829459	N/A	N/A	COMPARABLE			
CY62167DV30 (7C62161D)	4833178	N/A	N/A	COMPARABLE			
CY62167DV30 (7G62161D)	4835716	N/A	N/A	COMPARABLE			

Document History Page

Document Title: QTP 063901: 16 MEG MOBL DEVICES (CY62167D AND FAMILY) RAM8NLD-1.8V, FAB 5
Document Number: 001-87387

Rev.	ECN No.	Orig. of Change	Description of Change
**	3986168	ILZ	Initial Spec Release Documented & converted Memo # HGA-647 into qualification report spec format Removed Version 4.0 in the title page. Removed Cypress reference specs in the reliability tests performed table. Technology/Fab Process Description – Page 3 Corrected Generic Process Technology/Design Rule (µ-drawn) data from 0.15µm to 0.13µm
*A	4362868	HSTO	Align qualification report based on the new template in the front page. Update Cypress division on page 3 from Memory Image Division (MID) -> Memory Product Division (MPD)
*B	4749323	HSTO	Update reference for Reliability Director

Distribution: WEB

Posting: None