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Cypress Semiconductor
Product Qualification Report

QTP# 062401 VERSION *A
July 2014

64K/256K NVSAM Device Family 0.8µ Technology	
CY22E016L	5V 16K Non-Volatile SRAM (2K x 8)
CY14E064L	5V 64K Non-Volatile SRAM (8K x 8)
CY14E256L	5V 256K Non-Volatile SRAM (32K x 8)

FOR ANY QUESTIONS ON THIS REPORT, PLEAE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
062401	16/64/256K NVSRAM Device using 0.8umTechnology, Chartered Semiconductor	Sep 06

PRODUCT DESCRIPTION (for qualification)	
Purpose: Qualify CY14E064*/CYE256*/CY22E016 64/256K NVSRAM Products on (0.8µ) Technology fabricated at Chartered Semiconductor	
Marketing Part #:	CY14E064, CY14E256, CY22E016
Device Description:	5V Commercial and Industrial available in 28/32-Lead SOIC (300mils) Package
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION	
Metal Composition Passivation Type and Materials:	8000A Al-Si-Cu, 1000A TI/TIN 7000A Silicon Nitride, 3000A Silicon Dioxide
Generic Process Technology/Design Rule (-drawn):	0.8um 8F2 DT Technology
Gate Oxide Material/Thickness (MOS):	SiO2 Thickness
Name/Location of Die Fab (prime) Facility:	Chartered Semiconductor, Singapore
Die Fab Line ID/Wafer Process ID:	2N822-734-00A, 2N822-700-00A

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
28/32-Lead SOIC	**AMKOR-PHILS**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	SZ32
Package Outline, Type, or Name:	32-Lead SOIC (300mils)
Mold Compound Name/Manufacturer:	G600 Sumitomo
Mold Compound Flammability Rating:	UL94-V0
Oxygen Rating Index:	None
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	100% Matte Sn
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Sawing
Die Attach Supplier:	Ablestik
Die Attach Material:	8290
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.2 mil
Thermal Resistance Theta JA °C/W:	44.3°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	PHIL-M
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	KYEC-Taiwan

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate (w/ Wafer Level Burn-In)	Dynamic Operating Condition, Vcc Max = 5.5V, 125°C	P
High Temperature Operating Life Latent	Dynamic Operating Condition, Vcc Max = 5.5V, 125°C	P
Low Temperature Operating Life	Dynamic Operating Condition, Vcc = 6.5V, -30°C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Pressure Cooker	121°C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C/60%RH+3IR-Reflow, 260°C+0, -5°C	P
Data Retention	150°C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	1,500/1,700V JEDEC EIA/JESD22-A114-B	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Current Density	Meets the technology device level reliability specifications	P
Age Bond	200°C, 4HRS MIL-STD- 883, Method 883-2011	P
Capacitance	MIL-STD-883 Method 3012	P
Soft Error	JESD89 -1	P
Acoustic Microscopy	J-STD-020	P
Cross Section	MIL-STD-883, Method 2018	P
Static Latch-up	125C, ± 150mA JEDEC 78	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate (w/ Wafer Level Burn-In)	13,235 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	1,196,500 DHRs	0	0.7	55	14 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

[2] Chi-squared 60% estimations used to calculate the failure rate.

[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #:062401

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY14E256L		*CA0885E*	PHIL-M	COMP	15	0	
CY14E256L		*CA0870E*	PHIL-M	COMP	15	0	
STRESS: AGE BOND							
CY14E256L		*CA0704E*	PHIL-M	COMP	3	0	
STRESS: ENDURANCE TEST							
CY14E256L		*MIXED LOTS*	PHIL-M	100K hrs	655	0	
CY14E256L		*MIXED LOTS*	PHIL-M	500K hrs	655	0	
CY14E256L		*MIXED LOTS*	PHIL-M	1 Mil hrs	655	0	
CY14E064L		*MIXED LOTS*	PHIL-M	100K hrs	858	0	
CY14E064L		*MIXED LOTS*	PHIL-M	500K hrs	858	0	
CY14E064L		*MIXED LOTS*	PHIL-M	1 Mill hrs	858	0	
STRESS: DATA RETENTION, 150C							
CY14E256L		*MIXED LOTS*	PHIL-M	592	719	0	
CY14E256L		*MIXED LOTS*	PHIL-M	1000	719	0	
CY14E064L		*MIXED LOTS*	PHIL-M	592	1084	0	
CY14E064L		*MIXED LOTS*	PHIL-M	1000	1084	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
STK14C88	B52900.1	*CA0761E*	PHIL-M	COMP	9	0	
STK14C88	B52900.1	*CA0762E*	PHIL-M	COMP	9	0	
STK14C88	b44358.1	*CA0773E*	PHIL-M	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 1,500V							
CY14E256L		*CA0002E*	PHIL-M	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 1,700V							
CY14E064L	A33017.1	*CA0102E*	PHIL-M	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 70C, +/-150mA							
CY14E256L	A08267.1	*CA0002E*	PHIL-M	COMP	5	0	
CY14E064L	A33017.1	*CA0102E*	PHIL-M	COMP	6	0	
STRESS: STATIC LATCH-UP TESTING, 85C, +/-150mA							
CY14E256L	A19175.1	*CA0011E*	PHIL-M	COMP	5	0	
CY14E064L	A48223.1	*M0002E*	PHIL-M	COMP	5	0	

Reliability Test Data

QTP #: 062401

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 5.5V, Vcc Max							
CY14E256L		*MIXED LOTS*	PHIL-M	48	663	0	
CY14E256L	A46062.1	*CA0624E*	PHIL-M	48	7000	0	
CY14E064L		*MIXED LOTS*	PHIL-M	48	572	0	
CY14E064L	A44149.1	*CA0263E*	PHIL-M	48	5000	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 125C, 5.5V, Vcc Max							
CY14E256L		*MIXED LOTS*	PHIL-M	168	663	0	
CY14E256L		*MIXED LOTS*	PHIL-M	500	663	0	
CY14E256L		*MIXED LOTS*	PHIL-M	1000	663	0	
CY14E064L		*MIXED LOTS*	PHIL-M	168	572	0	
CY14E064L		*MIXED LOTS*	PHIL-M	500	572	0	
CY14E064L		*MIXED LOTS*	PHIL-M	1000	495	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.5V, Vcc							
CY14E256L		*CA0848E*	PHIL-M	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY14E256L		*CA0885E*	PHIL-M	168	50	0	
CY14E256L		*CA0885E*	PHIL-M	288	45	0	
CY14E256L		*CA0870E*	PHIL-M	168	49	0	
CY14E256L		*CA0870E*	PHIL-M	288	49	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY14E256L		*CA0885E*	PHIL-M	300	50	0	
CY14E256L		*CA0885E*	PHIL-M	500	50	0	
CY14E256L		*CA0885E*	PHIL-M	1000	50	0	
CY14E256L		*CA0870E*	PHIL-M	300	50	0	
CY14E256L		*CA0870E*	PHIL-M	500	50	0	
CY14E256L		*CA0870E*	PHIL-M	1000	50	0	

Document History Page

Document Title: QTP# 062401: 64K/256K NVSAM Device Family "CY22E016L/CY14E064L/CY14E256L" 0.8u Technology
Document Number: 001-88311

Rev.	ECN No.	Orig. of Change	Description of Change
**	4049878	HSTO	Initial Spec Release Qualification report published on Cypress.com is documented on memo HGA-357 and was transferred to qualification report spec template. Deleted Cypress obsolete referenced spec in Major package qualification details. Updated package availability based on current qualified test & Assembly site.
*A	4431902	HSTO	Align qualification report based on the new template in the front page Update Cypress division from Memory Image Division (MID) to Memory Product Division (MPD) at page3.

Distribution: WEB

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