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Cypress Semiconductor
Product Qualification Report

QTP# 052207 VERSION*D
March 2015

4 Meg / 2Meg / 8Meg Fast Asynchronous SRAM Family C9FD-3R Technology, Fab4	
CY7C1010DV33	**2-Mbit (256K x 8) Static RAM**
CY7C1011DV33	**2-Mbit (128K x 16) Static RAM**
CY7C1041D	**4-Mbit (256K x 16) Static RAM**
CY7C1041DV33	**4-Mbit (256K x 16) Static RAM**
CY7C1046D	**4-Mbit (1M x 4) Static RAM**
CY7C1046DV33	**4-Mbit (1M x 4) Static RAM**
CY7C1049D	**4-Mbit (512K x 8) Static RAM**
CY7C1049DV33	**4-Mbit (512K x 8) Static RAM**
CY7C1051DV33	**8-Mbit (512K x 16) Static RAM**
CY7C1059DV33	**8-Mbit (1M x 8) Static RAM**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
reliability@cypress.com or via a CYLINK CRM CASE

Prepared By:
Honesto Sintos
Reliability Engineer

Reviewed By:
Zhaomin Ji
Reliability Manager

Approved By:
Richard Oshiro
Reliability Director

PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
052207	C9FD-3R, Fab 4 New Process using CY7C104*D (4Meg Fast Synchronous SRAM) Product Family	Mar 06
061804	MM1 Mask Change on C9FD-3R, Fab 4 using 4Meg CY7C1041NC	Jul 06
064301	Rev. E MM1 Mask Qualification for 4Meg Devices	Nov 06
071802	Rev B. LITRM + DDLICM Mask Qualification for 4Meg Devices	Jun 07
080305	Qualify 4 Meg Fast Async Rev.B Mask DDLIM Fix	Apr 08
114502	Qualify PMM Mask Change for C9 4M Fast Async SRAM in C9FD- 3R Technology in Fab 4	Feb 12

PRODUCT DESCRIPTION (for qualification)	
Purpose: Qualify PMM Mask Change for C9 4M Fast Async SRAM in C9FD- 3R Technology in Fab 4	
Marketing Part #:	CY7C1010DV33, CY7C1011DV33, CY7C1041D, CY7C1041DV33, CY7C1046D, CY7C1046DV33, CY7C1049D, CY7C1049DV33, CY7C1051DV33, CY7C1059DV33
Device Description:	4M Asynchronous SRAM
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)

TECHNOLOGY/FAB PROCESS DESCRIPTION – C9FD-3R			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 100Å Ti / 3200Å Al / 300Å TiW Metal 2: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:		1000Å Oxide TEOS / 9000Å Nitride	
Generic Process Technology/Design Rule (□-drawn):		CMOS, Double Metal, 0.09µm	
Gate Oxide Material/Thickness (MOS):		23Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor – Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/C9FD-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
44-Lead TSOPII	**JCET-China (JT)**
32/36/44-Lead SOJ	**JCET-China (JT)**
48-Ball BGA	**ASE-Taiwan (G)**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZW44
Package Outline, Type, or Name:	44-Lead Thin Small Outline Packages (Type II)
Mold Compound Name/Manufacturer:	Hitachi CEL9200CYRU
Mold Compound Flammability Rating:	NA
Mold Compound Alpha Emission Rate:	N/A
Oxygen Rating Index:	NA
Lead Frame Material:	Copper base
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Back grind
Die Separation Method:	100% Saw Through
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-33621
Wire Bond Method:	Ultrasonic
Wire Material/Size:	Au, 0.8mil
Thermal Resistance Theta JA °C/W:	71.53°C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	001-64160
Name/Location of Assembly (prime) facility:	Cypress Philippines (CML-R)
MSL Level	3
Reflow Profile	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-R

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	AEC-Q100-008 and JESD22-A108 Dynamic Operating Condition, Vcc Max = 3.77V, 150□C	P
High Temperature Operating Life Latent Failure Rate	JESD22-A108 Dynamic Operating Condition, Vcc Max = 3.77V, 150□C	P
Long Life Verification	JESD22-A108 Dynamic Operating Condition, Vcc = 3.77V, 150□C	P
High Temperature Steady State Life	JESD22-A108 Static Operating Condition, Vcc Max = 3.77V, 150□C	P
High Accelerated Saturation Test (HAST)	JESD22-A110, 130□C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30□C/60%RH+ Reflow, 260□C+0, -5□C 130□C, 3.65V, 85%RH	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65□C to 150□C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30□C/60%RH+ Reflow, 260□C+0, -5□C	P
Pressure Cooker	JESD22-A102, 121□C, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30□C/60%RH+ Reflow, 260□C+0, -5□C	P
High Temperature Storage	JESD22-A103, 150□C, no bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114-E	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-A101	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	JEDEC JSTD-020	P
Static Latch up	JESD78 125C, ± 200/300mA	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	11,838 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	2,481,000 DHRs	6*	0.7	170	18 FIT

Note:
LFR data was from initial C9 technology/product qualification completed in March 2006 and met Cypress 31 FITs qualification requirement. Process improvements and test screens were implemented to fix and eliminate the defects.

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

- Failures are fixed with reference corrective action (CAR) # 200613035.

Reliability Test Data

QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	15	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	15	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	10	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	10	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	10	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	48	1551	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	48	1518	1	LI DEFFECT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	48	3314	1	NON-VISUAL
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	80	1544	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	1542	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	80	1516	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	500	1514	3	SINGLE BIT & BLOCKED CONTACT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	80	1517	1	LOST REJECT
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	500	1511	2	SINGLE BIT
STRESS: LONG LIFE VERIFICATION, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	400	0	
STRESS: HIGH TEMPERATURE STEADY STATE LIFE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	80	80	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	168	80	0	
STRESS: HIGH TEMPERATURE STORAGE							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	50	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	50	0	

Reliability Test Data

QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	9	0	
CY7C1041D (7C1541N)	4538630	*610610603*	CML-R	COMP	9	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	9	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	9	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	9	0	
CY7C1041D (7C1541N)	4530733	*610607231*	CML-R	COMP	9	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	9	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	9	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	3	0	
CY7C1041D (7C1541N)	4530733	*610607231*	CML-R	COMP	3	0	
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	3	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	3	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-200mA							
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	COMP	3	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	COMP	3	0	
CY7C1046DV33 (7C1346N)	4538680	*610610605*	CML-R	COMP	3	0	
CY7C1049DV33 (7C1349N)	4538680	*610611051*	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.5V, +/-300mA							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 052207

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: STATIC LATCH-UP TESTING, 125C, 8.5V, +/-200mA							
CY7C1049D (7C1549N)	4538680	*610611050*	CML-R	COMP	3	0	
CY7C1046D (7C1346N)	4538680	*610610606*	CML-R	COMP	3	0	
CY7C1041D (7C1541N)	4552229	*610617290*	CML-R	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	128	45	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	128	45	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	128	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	168	46	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	168	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	288	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	168	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	288	50	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	300	45	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	500	45	0	
CY7C1041DV33 (7C1341N)	4533793	*610553668*	CML-R	1000	45	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	300	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	500	50	0	
CY7C1041DV33 (7C1341N)	4536828	*610558451*	CML-R	1000	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	300	50	0	
CY7C1041DV33 (7C1341N)	4530733	*610607229*	CML-R	500	50	0	

Reliability Test Data

QTP #: 061804

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1041DV33 (7C1541N)	4552229	610617290	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1041DV33 (7C1541N)	4552229	610617290	CML-R	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1041DV33 (7C1541N)	4552229	610617290	CML-R	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.5V, +/-200mA							
CY7C1041DV33 (7C1541N)	4552229	610617290	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 071802

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: E-TEST							
7C1041NC	4709075	N/A	N/A	COMP	COMPARABLE		
7C1041NC	4708714	N/A	N/A	COMP	COMPARABLE		
7C1041NC	4709032	N/A	N/A	COMP	COMPARABLE		
STRESS: SORT YIELD							
7C1041NC	4709075	N/A	N/A	COMP	COMPARABLE		
7C1041NC	4708714	N/A	N/A	COMP	COMPARABLE		
7C1041NC	4709032	N/A	N/A	COMP	COMPARABLE		

Reliability Test Data

QTP #: 080305

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.77V, Vcc Max							
CY7C1041DV33 (7C1341N)	4750244	610807572	N/A	48	5306	0	
CY7C1041DV33 (7C1341N)	4750244	610807575	N/A	48	4460	0	
CY7C1041DV33 (7C1341N)	4750244	610807576	N/A	48	2072	0	

Reliability Test Data

QTP #: 114502

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: E-TEST							
7C1041NC	4142220	N/A	N/A	COMP	COMPARABLE		
STRESS: SORT YIELD							
7C1041NC	4142220	N/A	N/A	COMP	COMPARABLE		

Document History Page

Document Title: QTP# 052207: 4 MEG / 2 MEG / 8 MEG FAST ASYNCHRONOUS SRAM FAMILY, C9FD-3R TECHNOLOGY, FAB4
Document Number: 001-76195

Rev.	ECN No.	Orig. of Change	Description of Change
**	3528439	NSR	Initial spec release. Original latest qual report was released in memo HGA-410. Added QTP#114502 data
*A	3553259	NSR	Added 2 Meg and 8M in the Title page.
*B	3922787	JYF	Removed Version 5.1 in QTP# 052207 title page; Deleted CML-R in Assembly Site Facility Table and replaced with JCET-China (JT); Deleted obsolete referenced spec 11-20047 and 001-00318 in Major Package Information Table and replaced with 001-64160 and 001-33621; Updated Rel Tests Performed Table: - Deleted “3IR” in reflow step of HAST, TCT and PCT stresses. - Deleted Cypress’ referenced specs and replaced with industry standards. - Deleted Current Density (internal requirement only).
*C	4305023	HSTO	Align qualification report based on the new template in the front page
*D	4678942	HSTO	Align qualification report based on the new template in the front page

Distribution: WEB

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