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Cypress Semiconductor
Product Qualification Report

QTP# 052103
June 2013

MoBL DUAL PORT (SPLIT VOLTAGE) RAM FAMILY R52LD3 TECHNOLOGY, FAB4	
CYDC256B16 **CYDC128B16** **CYDC064B16** **CYDC128B08** **CYDC064B08**	**1.8V 4K/8K/16K x 16 and 8K/16K x 8 Consumer Dual–Port Static RAM**
CYDM256B16 **CYDM128B16** **CYDM064B16** **CYDM128B08** **CYDM064A08**	**1.8V 4K/8K/16K x 16 and 8K/16K x 8 MoBL® Dual–Port Static RAM**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

QUAL REPORT		DESCRIPTION OF QUALIFICATION PURPOSE		DATE COMP.
99075		New Technology R52LD-3 / New Slow Low Power MoBL SRAM, CY62137V		Apr 99
052103		Qualify 256K Dual Port (Split Voltage) Device Family, R52LD3 Technology from Fab4		Nov 05

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify MoBL Dual Port (Split Voltage) RAM Device Family using R52LD3 Technology, Fab4	
Marketing Part #:	CYDC256B16, CYDC128B16, CYDC064B16, CYDC128B08, CYDC064B08, CYDM256B16, CYDM128B16, CYDM064B16, CYDM128B08, CYDM064B08
Device Description:	1.8V 256K (16x16) MoBL Dual Port and Density Width Derivatives
Cypress Division:	Cypress Semiconductor Corporation – DataCom Division (DCD)
Overall Die (or Mask) REV:	Rev. A
What ID markings on Die:	7C02628A

TECHNOLOGY/FAB PROCESS DESCRIPTION – R52LD3			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500 Å-TiW/6000 Å Al-Cu/500 Å TiW Metal 2: 300 Å-Ti/8000 Å Al-Cu/300 Å TiW
Passivation Type and Materials:			1,000A TEOS + 9,000A SiN
Free Phosphorus contents in top glass layer (%):			0%
Die Coating(s), if used:			N/A
Number of Transistors in Device:			294,920
Number of Gates in Device:			735,205
Generic Process Technology/Design Rule (-drawn):			R52 TDR (01-30065), 0.25um Technology
Gate Oxide Material/Thickness (MOS):			55Å
Name/Location of Die Fab (prime) Facility:			Cypress Semiconductor – Bloomington Minnesota
Die Fab Line ID/Wafer Process ID:			7C02628AC

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
100-Ball PBGA	ASE Taiwan (TAIWN-G), CML-RA
100-Lead TQFP	CML-RA, JCET, China

Note: Package Qualification details upon request.

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BZ100
Package Outline, Type, or Name:	100-Ball, Plastic Ball Grid Array (FBGA)
Mold Compound Name/Manufacturer:	KE2270
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	N/A
Substrate Material:	BT
Lead Finish, Composition / Thickness:	SnAgCu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	100%
Die Attach Supplier:	Ablestik
Die Attach Material:	2025D
Die Attach Method:	Epoxy
Bond Diagram Designation:	001-00425
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 0.8mil
Thermal Resistance Theta JA °C/W:	44.21□C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-00011
Name/Location of Assembly (prime) facility:	ASE Taiwan (TAIWN-G)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-RA, KYEC,Taiwan
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability.

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	AZ100
Package Outline, Type, or Name:	100-Lead Thin Qual Flat Pack (TQFP) Lead Free
Mold Compound Name/Manufacturer:	CEL9200CY(R)-V
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	N/A
Substrate Material:	Cooper
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	100%
Die Attach Supplier:	Dexter
Die Attach Material:	QMI 509
Die Attach Method:	Epoxy
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 0.8mil
Thermal Resistance Theta JA °C/W:	50C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	CML-R

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	CML-RA, KYEC,TAIWAN
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 3.45V, 150C Dynamic Operating Condition, Vcc Max = 3.8V, 150C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 3.45V, 150C Dynamic Operating Condition, Vcc Max = 3.8V, 150C	P
Long Life Verification	Dynamic Operating Condition, Vcc Max = 3.8V, 150C	P
High Temperature Steady State Life	Static Operating Condition, Vcc Max = 3.63V, 150C	P
Low Temperature Operating Life	-30C, 3.8V, 8 MHz	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30□C/60%RH+3IR-Reflow, 220C+0, -5C	P
Pressure Cooker	121C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220C+0, -5C	P
High Accelerated Saturation Test (HAST)	140C, 3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH+3IR-Reflow, 220C+0, -5C	P
High Temperature Storage	165C, no bias	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22, Method A114-B	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015	P
Static Latch-up	125C, 6.5V/11.5V, 300mA In accordance with JEDEC 17	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Acceleration Factor[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	3,999 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	400,500 HRs	1	0.7	170	15 FITs

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[1] Assuming an ambient temperature of 55C and a junction temperature rise of 15C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism. k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 99075

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	COMP	3	0	
CY62137V-ZSIB	4851023	*619907600*	CSPI-R	COMP	3	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V, >Vcc Max)							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	48	1505	0	
CY62137V-ZSIB	4902501	*619905577*	CSPI-R	48	1504	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V, >Vcc Max)							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	80	405	0	
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	500	405	1	UNKNOWN
CY62137V-ZSIB	4902501	*619905577*	CSPI-R	80	396	0	
CY62137V-ZSIB	4902501	*619905577*	CSPI-R	500	396	0	
STRESS: LONG LIFE VERIFICATION, (150C, 3.8V, >Vcc Max)							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	1000	404	0	
STRESS: HIGH TEMP DYNAMIC STEADY STATE LIFE TEST, (150C, 3.63V, >Vcc Max)							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	80	80	0	
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	168	80	0	
STRESS: LOW TEMPERATURE OPERATING LIFE, (-30C, 3.8V, 8 MHZ)							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	500	45	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	COMP	3	0	
CY62137V-ZSIB	4851023	*619907600*	CSPI-R	COMP	3	0	
STRESS: HIGH TEMPERATURE STORAGE, 165C, no bias							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	336	47	0	
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	1000	47	0	
CY62137V-ZSIB	4902501	*619905577*	CSPI-R	336	48	0	
STRESS: TC CONDITION C, -65C TO 150C, PRE COND 192 HRS 30C/60% RH, MSL3							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	300	48	0	
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	1000	48	0	
CY62137V-ZSIB	4902501	*619905577*	CSPI-R	300	48	0	
CY62137V-ZSIB	4902501	*619905577*	CSPI-R	1000	48	0	

Reliability Test Data

QTP #: 99075

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192HRS 30C/60%RH, MSL3							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	168	48	(	
STRESS: HI-ACCEL SATURATION TEST, (140C, 3.63V), 85%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	128	48	0	
CY62137V-ZSIB	4852210	*619903364*	CSPI-R	256	48	0	
CY62137V-ZSIB	4902501	*619905577*	CSPI-R	128	48	0	
CY62137V-ZSIB	4902501	*619905577*	CSPI-R	256	48	0	
CY62137V-ZSIB	4903568	*619907944*	CSPI-R	128	48	0	

Reliability Test Data

QTP #: 052103

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 3.45V, Vcc Max							
CYDC256B16 (7C02628A)	4531145	*610540035*	TAIWN-G	48	330	0	
CYDC256B16 (7C02628A)	4531145	*610540036*	TAIWN-G	48	328	0	
CYDC256B16 (7C02628A)	4531145	*610540037*	TAIWN-G	48	332	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CYDM256B16 (7C02628A)	4531145	*610539449*	TAIWN-G	COMP	9	0	
CYDC256B16 (7C02628A)	4531145	*610540035/6/7*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V							
CYDM256B16 (7C02628A)	4531145	*610539449*	TAIWN-G	COMP	9	0	
CYDC256B16 (7C02628A)	4531145	*610540035/6/7*	TAIWN-G	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CYDM256B16 (7C02628A)	4531145	*610539449*	TAIWN-G	COMP	3	0	
CYDC256B16 (7C02628A)	4531145	*610540035/6/7*	TAIWN-G	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING (125C, 7.0V, +/-300mA)							
CYDM256B16 (7C02628A)	4531145	*610539449*	TAIWN-G	COMP	3	(	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CYDM256A16 (7C02618A)	4503160	*610510254*	TAIWN-G	168	50	0	
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CYDM256A16 (7C02618A)	4503160	*610510254*	TAIWN-G	300	50	0	
CYDM256A16 (7C02618A)	4503160	*610510254*	TAIWN-G	500	50	0	
CYDM256A16 (7C02618A)	4503160	*610510254*	TAIWN-G	1000	50	0	

Document History Page

Document Title: QTP # 052103 : MoBL DUAL PORT (SPLIT VOLTAGE) RAM FAMILY R52LD3 TECHNOLOGY, FAB4
Document Number: 001-87925

Rev.	ECN No.	Orig. of Change	Description of Change
**	4026981	ILZ	Initial Spec Release Qualification report published on Cypress.com is documented on memo LGQ-385 in spec format. Initiated spec for QTP 052103 and all data from Memo LGQ-385 was transferred to qualification report spec template. Deleted package qualification details on package qualification history table Deleted Cypress reference Spec and replaced with Industry Standards Updated package availability based on current qualified test & assembly site

Distribution: WEB

Posting: None