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Cypress Semiconductor
Product Qualification Report

QTP# 042205 VERSION *E
May 2015

9 Meg Synchronous SRAM Family ***Technology R9T-3R, Fab4***	
CY7C1354C CY7C1356C	**9-Mbit (256K x 36/512K x 18) Pipelined SRAM with NoBL™ Architecture**
CY7C1354CV25 CY7C1356CV25	**9-Mbit (256K x 36/512K x 18) Pipelined SRAM with NoBL™ Architecture**
CY7C1355C CY7C1357C	**9-Mbit (256K x 36/512K x 18) Flow-Through SRAM with NoBL™ Architecture**
CY7C1360C CY7C1362C	**9-Mbit (256K x 36/512 x 18) Pipelined SRAM**
CY7C1361C CY7C1363C/D	**9-Mbit (256K x 36/512 x 18) Flow-Through SRAM**
CY7C1364C	**9-Mb (256K x 32) Pipelined Sync SRAM**
CY7C1365C	**9-Mb (256K x 32) Flow-Through Sync SRAM**
CY7C1366C CY7C1367C	**9-Mbit (256K x 36/512 x 18) Pipelined DCD Sync SRAM**
CY7C1368C	**9-Mb (256K x 32) Pipelined DCD Sync SRAM**
CY7C1378C	**9-Mbit (256K x 32) Pipelined SRAM with NoBL™ Architecture**
CY7C1379C	**9-Mbit (256K x 32) Flow-Through SRAM with NoBL™ Architecture**
CY7C1354D	**9-Mbit (256K x 36) Pipelined SRAM with NoBL™ Architecture**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
reliability@cypress.com or via a CYLINK CRM CASE

Prepared By:
Honesto Sintos
Reliability Engineer

Reviewed By:
Zhaomin Ji
Reliability Manager

Approved By:
Don Darling
Reliability Director

PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
033302		New Technology R9T-3R, Fab 4, and New Device CY7C137*/138*E (18Meg) Synchronous product family		Sep 04
042205		New Device CY7C1360C, (9 Meg) Synchronous Product Family in R9T-3R Technology, Fab 4		Sep 04
053405		Manufacturability of CY7C1360CC, 9Meg Synchronous Product Family in R9T-3R Technology		Sep 05

Cypress products are manufactured using qualified processes. The technology qualification for this product is referenced above and must be considered to get a complete and thorough evaluation of the reliability of the product.

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify CY7C1360C Synchronous Product Family in qualified Technology R9T-3R, Fab 4			
Marketing Part #:	CY7C1354C, CY7C1355C, CY7C1356C, CY7C1357C, CY7C1354CV25, CY7C1356CV25, CY7C1360C, CY7C1361C, CY7C1362C, CY7C1363C/D, CY7C1364C, CYC71365C, CY7C1366C, CYC71367C, CY7C1368C, CYC71378C, CY7C1379C		
Device Description:	2.5V, 3.3V, Commercial and Industrial		
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. C	
What ID markings on Die:	7C1360C		

TECHNOLOGY/FAB PROCESS DESCRIPTION – R9T-3R			
Number of Metal Layers:	3	Metal Composition:	Metal 1: 100ª CoTi, 3200ª Al, 300ª TiW Metal 2: 150Å Ti / 6000Å Al / 300Å TiW Metal 3: 150Å Ti / 8000Å Al / 300Å TiW
Passivation Type and Materials:		1000Å Oxide TEOS / 9000Å Nitride	
Free Phosphorus contents in top glass layer (%):		0%	
Number of Transistors in Device		~5.8.E+07	
Number of Logic Gates in Device		~1.2.E+06	
Generic Process Technology/Design Rule (□-drawn):		CMOS, Triple Metal, 90 nm	
Gate Oxide Material/Thickness (MOS):		Nitridized SiO_2, 23Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor – Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/R9T-3R	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
100-Lead TQFP	**JCET-China (JT)**
119/165-Ball BGA	**TAIWN-G**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	AZ0AA
Package Outline, Type, or Name:	100L TQFP
Mold Compound Name/Manufacturer:	KEG6000 / Kyocera
Mold Compound Flammability Rating:	V-O per UL94
Mold Compound Alpha Emission Rate:	0.002 CPH/cm2
Oxygen Rating Index: >28%	N/A
Lead Frame Designation:	Reduced Metal Pad
Lead Frame Material:	Copper
Substrate Material:	N/A
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Wafersaw
Die Attach Supplier:	Henkel
Die Attach Material:	QMI 509
Bond Diagram Designation	001-14561, 001-33059, 001-30701
Wire Bond Method:	Thermosonic
Wire Material/Size:	0.9mil / Au
Thermal Resistance Theta JA □C/W:	11.3 C/W
Package Cross Section Yes/No:	Yes
Assembly Process Flow:	001-64159
Name/Location of Assembly (prime) facility:	JT-JCET China
MSL LEVEL	3
REFLOW PROFILE	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	Cypress Philippines (CML-R), Chipmos-Taiwan (Taiwn-GO)
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	JESD22-A108: Dynamic Operating Condition, Vcc Max (Core) = 2.25V, 150ºC	P
High Temperature Operating Life Latent Failure Rate	JESD22-A108: Dynamic Operating Condition, Vcc Max (Core)=2.25V, 150 ºC	P
High Temperature Steady State Life	JESD22-A108: Static Operating Condition, Vcc Max= 2.25V, 150 ºC	P
Low Temperature Operating Life	JESD22-A108: Dynamic Operating Condition, Vcc = 6.50V, -30 ºC	P
High Accelerated Saturation Test (HAST)	JEDEC STD 22-A110 130 ºC ,3.63V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30 ºC /60%RH, 260 ºC Reflow	P
Temperature Cycle	MIL-STD-883, Method 1010, Condition C, -65 ºC to 150 ºC Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30 ºC /60%RH, 260 ºC Reflow	P
Pressure Cooker	JESD22-A102: 121ºC, 100%RH , 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30 ºC /60%RH, 260 ºC Reflow	P
High Temperature Storage	JESD22-A103, 150 ºC, No bias	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JEDEC EIA/JESD22-A114	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V JESD22-C101	P
Current Density	Meets the Technology Device Level Reliability Specifications	P
Age Bond Strength	200°C, 4HRS MIL-STD-883, Method 883-2011	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30 ºC /60%RH, 260 ºC Reflow	P
Dynamic Latch up	JEDEC 17	P
Static Latch up	125C, 7.5V, ± 300mA, JEDEC 17	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[3]	Failure Rate
High Temperature Operating Life Early Failure Rate	8,541 Devices	1	N/A	N/A	117 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	485,000 DHRs	0	0.7	170	11 FIT

[1] Assuming an ambient temperature of 55□C and a junction temperature rise of 15□C.
[2] Chi-squared 60% estimations used to calculate the failure rate..
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
K = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	COMP	15	0	
CY7C1470V33 (7C1470A)	4323794	*610348235*	TAIWN-G	COMP	15	0	
STRESS: AGE BOND STRENGTH							
CY7C1370DV33 (7C1370E)	4421235	*610447674*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	COMP	5	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	COMP	5	0	
STRESS: BALL SHEAR							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: BOND PULL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	10	0	
STRESS: DYNAMIC LATCH-UP							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4421235	*610446833*	CML-R	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	9	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	9	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	9	0	
STRESS: HIGH TEMPERATURE STORAGE, PLASTIC, 150C							
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	500	47	0	
CY7C1470V33 (7C1470A)	4323794	*610348234*	TAIWN-G	1000	47	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	48	193	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	48	951	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	48	1246	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	48	1382	1	Non-Visual
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1370DV33 (7C1370E)	4345377	*610424939*	CML-R	500	170	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	500	400	0	
CY7C1370DV33 (7C1370E)	4410258	*610437891*	CML-R	500	400	0	
STRESS: HIGH TEMP STEADY STATE LIFE TEST, 150C, 2.25V, Vcc Max							
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	80	85	0	
CY7C1470V33 (7C1470A)	4405088	*610418824*	TAIWN-G	168	85	0	
STRESS: INTERNAL VISUAL							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	5	0	
STRESS: LOW TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, -30C, 6.50V, Vcc							
CY7C1470V33 (7C1470A)	4333765	*610349455*	CML-R	500	45	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, 15 Psig, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	168	50	0	
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	168	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	168	43	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 3.63V, PRE COND 192 HR 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4406200	*610435906*	CML-R	128	50	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	128	47	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	128	44	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1470V33 (7C1470A)	4352888	*610425832*	TAIWN-G	COMP	3	0	
CY7C1470V33 (7C1470A)	4401980	*610425833*	TAIWN-G	COMP	3	0	
CY7C1370DV33 (7C1370E)	4345377	*610417723*	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 033302

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRE COND 192 HRS 30C/60%RH, MSL3							
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	300	50	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	500	49	0	
CY7C1370DV33 (7C1370E)	4345377	*610422227*	CML-R	1000	49	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	300	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	500	43	0	
CY7C1470V33 (7C1470A)	4330156	*610417279*	CML-R	1000	42	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	300	34	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	500	33	0	
CY7C1470V33 (7C1470A)	4321389	*610417280*	CML-R	1000	33	0	
STRESS: THERMAL SHOCK							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	100	46	0	
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	200	46	0	
STRESS: X-RAY							
CY7C1470V33 (7C1470A)	4321389	*610417278*	CML-R	COMP	15	0	

Reliability Test Data
QTP #: 042205

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY7C1354C (7C13540C)	4423932	*610441270*	CML-R	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JEDEC EIA/JESD22-A114-B, 2,200V							
CY7C1354C (7C13540C)	4423932	*610441270*	CML-R	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY7C1354C (7C13540C)	4423932	*610441270*	CML-R	COMP	9	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1354C (7C13540C)	4423932	*610442997*	CML-R	48	2138	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, +/300mA							
CY7C1354C (7C13540C)	4423932	*610441270*	CML-R	COMP	3	0	

Reliability Test Data

QTP #: 053405

Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 150C, 2.25V, Vcc Max (Core)							
CY7C1360C (7C13600C)	4512530	*610528202*	CML-R	48	2846	0	
CY7C1360C (7C13600C)	4511189	*610528203*	CML-R	48	2851	0	
CY7C1360C (7C13600C)	4514016	*610528948*	CML-R	48	1281	0	
CY7C1360C (7C13600C)	4514016	*610528948M*	CML-R	48	1563	1	METAL STRINGER

Document History Page

Document Title: QTP 042205: 9 MEG SYNCHRONOUS SRAM FAMILY (CY7C1360CC)TECHNOLOGY R9T-3R, FAB4
Document Number: 001-61281

Rev.	ECN No.	Orig. of Change	Description of Change
**	2923845	HGA	Initial spec release
*A	3989507	NSR	Corrected the QTP# from 053405 to 042205 and updated the spec title. Changed the purpose of QTP 053405 from GOOBI to Manufacturability. Package information used is for CML, Conventional which is already obsolete. Replaced all package information on page 4 from JCET package qual which is the current qualified site for this device Removed Cypress reference specs and replaced with Industry standards in the reliability tests performed table on page 5 Deleted “3IR” in reflow step of HAST, PCT and TCT on reliability stress performed table, page 5
*B	4039660	JYF	Added CY7C1363D part no. in the qual report device coverage; Updated division from MID to MPD; Updated Assembly Site Facility from CML-R to JCET-China (JT) in Package Availability table; Added industry standard references of EFR, LFR, HTSSL, LTOL, HAST and PCT in Reliability Test Performed table.
*C	4092546	HSTO	Added device CY7C1354D in the cover page in reference to memo GRW-409.
*D	4376528	HSTO	Align qualification report based on the new template in the front page
*E	4768500	HSTO	Update reference for Reliability Director

Distribution: WEB

Posting: None