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Cypress Semiconductor
Product Qualification Report

QTP# 041406 VERSION*A
February 2019

4 MEG (1.8V/3.0V) MOBL DEVICES RAM8NLD-1.8 TECHNOLOGY, Skywater	
CY62146DV30	**4-Mbit (256K x 16) Static RAM**
CY62147DV18 MoBL2™	**4 Mb (256K x 16) Static RAM**
CY62147DV18 MoBL2™	**4 Mb (256K x 16) Static RAM Die**
CY62147DV30	**4 Mb (256K x 16) Static RAM**
CY62147DV30 MoBL®	**4 Mb (256K x 16) Static RAM Die**
CY62148DV30	**4Mb (512K x 8) MoBL® Static RAM**

FOR ANY QUESTIONS ON THIS REPORT, PLEASE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
041406	New Device Qual, 4 Meg (1.8V/3.0V) MoBL (7C62145EC/7C62345EC) using RAM8NLD-18 Technology from Skywater	Apr 04
042001	New Device Qual, Metal Mask Option, 4 Meg MoBL (7C62142EC) using RAM8NLD-1.8 Technology from Skywater	May 04

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify CY62147DV* (1.8V/3.0V) device option and family, RAM8NLD-1.8 Technology, Skywater		
Marketing Part #:	CY62146DV*, CY62147DV*, CY62148DV*	
Device Description:	2.2V-3.6V, Industrial available in 36/48 FBGA, 32/44 TSOP II package.	
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. E
What ID markings on Die:	7C62145E	

TECHNOLOGY/FAB PROCESS DESCRIPTION – RAM8NLD-1.8			
Number of Metal Layers:	Proprietary	Metal Composition:	Proprietary
Passivation Type and Materials:	Proprietary		
Free Phosphorus contents in top glass layer	Proprietary		
Number of Transistors in Device	Proprietary		
Number of Gates in Device	Proprietary		
Generic Process Technology/Design Rule	Proprietary		
Gate Oxide Material/Thickness (MOS):	Proprietary		
Name/Location of Die Fab (prime) Facility:	Skywater -- Bloomington, MN		
Die Fab Line ID/Wafer Process ID:	RAM8NLD-1.8V/3.0V		

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
36/48-ball FBGA	**TAIWN-G, CML-RA**
32/44-lead TSOP II	**CML-RA, TAIWN-T, CHINA-JT**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	ZW44
Package Outline, Type, or Name:	44L TSOPII
Mold Compound Name/Manufacturer:	KEG6000
Mold Compound Flammability Rating:	V-O per UL94
Mold Compound Alpha Emission Rate:	N/A
Oxygen Rating Index: >28%	N/A
Lead Frame Designation:	Reduced Metal Pad
Lead Frame Material:	Copper
Substrate Material:	N/A
Lead Finish, Composition / Thickness:	NiPdAu
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	Wafersaw
Die Attach Supplier:	Henkel
Die Attach Material:	QMI 509
Bond Diagram Designation	10-06506
Wire Bond Method:	Thermosonic
Wire Material/Size:	0.9mil / Au (23um)
Package Cross Section Yes/No:	Yes
Assembly Process Flow:	001-64159
Name/Location of Assembly (prime) facility:	JT-JCET China
MSL LEVEL	3
REFLOW PROFILE	260C

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	**CML-R, KYEC**
Fault Coverage:	100%

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BV48
Package Outline, Type, or Name:	48-ball Fine Pitch Ball Grid Array (VFBGA)
Mold Compound Name/Manufacturer:	Shinetsu KMC211-VAA-EC
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	100%
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 8355F
Die Attach Method:	Epoxy
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0mil (25um)
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	11-20034
Name/Location of Assembly (prime) facility:	CML -RA / Taiwan-G

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	**CML-RA, KYEC**
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.4V, 125^{0}C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 2.4V, 150 ^{0}C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65^{0}C to 150^{0}C Precondition: JESD22 Moisture Sensitivity MSL3 192 Hrs, 30C/60%RH , 235^{0}C +5, 0^{0}C Reflow	P
Pressure Cooker	121^{0}C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30C/60%RH , 235^{0}C +5, 0^{0}C Reflow	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V JESD22, Method A114-B	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101C	P
Static Latch-up	125C, 6.0V, 300mA 125C, 7.5V, 300mA In accordance with JEDEC 17	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	34 67	0	N/A	N/A	0 PPM
High Temperature Operating Life[1, 2,] Long Term Failure Rate	197,660 DHRs	0	0.7	170	27 FIT

1 Assuming an ambient temperature of 55C and a junction temperature rise of 15C.
2 Chi-squared 60% estimations used to calculate the failure rate.
3 Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

Where:

E_A =The Activation Energy of the defect mechanism. k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 041406

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V							
CY62147DV30L (7C62147E)	4346463	*610414072N*	*CML-R*	COMP	9	0	
CY62147DV18LL (7C62347E)	4346463	*610413728M*	*CML-R*	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62147DV30L (7C62147E)	4346463	*610414072N*	*CML-R*	COMP	3	0	
CY62147DV18LL (7C62347E)	4346463	*610413728M*	*CML-R*	COMP	3	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62147DV30L (7C62147E)	4346463	*610414072N*	*CML-R*	COMP	9	0	
CY62147DV18LL (7C62347E)	4346463	*610413728M*	*CML-R*	COMP	9	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.4V, Vcc Max							
CY62147DV30L (7C62147E)	4339029	*610352577*	*TAIWN-G*	96	3467	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.4V, Vcc Max							
CY62147DV30L (7C62147E)	4339029	*610352577*	*TAIWN-G*	80	397	0	
CY62147DV30L (7C62147E)	4339029	*610352577*	*TAIWN-G*	500	395	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 192 HR 30C/60%RH, MSL3							
CY62147DV30L (7C62147E)	4339029	*610352577*	*TAIWN-G*	168	50	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, □300mA							
CY62147DV30L (7C62147E)	4346463	*610414072N*	*CML-R*	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 6.0V, □300mA							
CY62147DV18LL (7C62347E)	4346463	*610413728M*	*CML-R*	COMP	3	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY62147DV30L (7C62147E)	4339029	*610352577*	*TAIWN-G*	300	50	0	
CY62147DV30L (7C62147E)	4339029	*610352577*	*TAIWN-G*	500	50	0	
CY62147DV30L (7C62147E)	4339029	*610352577*	*TAIWN-G*	1000	50	0	

Reliability Test Data

QTP #: 042001

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62148DV30L (7C62142E)	4348963	*610418768/9/70*	*TAIWN-T*	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER JESD22, METHOD A114-B, 2,200V							
CY62148DV30L (7C62142E)	4348963	*610418768/9/70*	*TAIWN-T*	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62148DV30L (7C62142E)	4348963	*610418768/9/70*	*TAIWN-T*	COMP	3	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.5V, □300mA							
CY62148DV30L (7C62142E)	4348963	*610418768/9/70*	*TAIWN-T*	COMP	3	0	

Document History Page

Document Title: QTP# 041406 : 4 MEG (1.8V/3.0V) MOBL DEVICES RAM8NLD-1.8 TECHNOLOGY, SKYWATER
Document Number: 001-87794

Rev.	ECN No.	Orig. of Change	Description of Change
**	4018106	ILZ	Initial Spec Release Qualification report published on Cypress.com is documented on memo LGQ-58 and not in spec format. Initiated spec for QTP 041406 and data from LGQ-58 was transferred to qualification report spec template. Updated package availability based on current qualified test & assembly site. Deleted Cypress reference Spec and replaced with Industry Standards. Deleted previous package assembly information and replaced with existing and qualified assembly site
*A	6481539	HSTO FRA	Alignment of Qualification report template Update Cypress logo Update “TECHNOLOGY/FAB PROCESS DESCRIPTION” table Update “MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION” table Replaced “Fab4/CMI” with Skywater Removed Distribution and Posting in document history page.