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Cypress Semiconductor
Product Qualification Report

QTP# 025007
May 2013

16 Meg MoBL Devices RAM8NLD-1.8V Technology, Fab4	
CY62167DV20	16M (1024K x 16) Static RAM
CY62167DV18 MoBL2™	16M (1024K x 16) Static RAM
CY62167DV30 MoBL®	16M (1024K x 16) Static RAM
CY62167DV30 MoBL®	16 Mb (1M x 16) Static RAM
CY62168DV30 MoBL®	16M (2048K x 8) Static RAM
CY62177DV30 MoBL®	32M (2M X 16) Static RAM

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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PRODUCT QUALIFICATION HISTORY

Qual Report	Description of Qualification Purpose	Date Comp
025007	New Device Qual , 16Meg, MoBL Static RAM CY62167DV* device and family on RAM8NLD-1.8 Technology	Jul 03
034203	New Mask, P1M, LI1M, CTM1, for 7C62165DC/7C62365DC (16Meg MoBL) using RAM8NLD-1.8 Technology , Fab 4	Nov 03
035101	Qualify Rev. B Mask change (P1M, LI1M, MM1, VIA) for 7C62165DC/7C62365DC (16Meg MoBL) using RAM8NLD-1.8 Fab4 Process	Dec 03
083301	Qualify MM2 minor mask-change for RAM8 16M MoBL family (7G62161DK/ 7C62161DC/ 7C62171D) fabricated at Fab4 and Fab5	Nov 08

PRODUCT DESCRIPTION (for qualification)		
Qualification Purpose: Qualify CY62167DV* device and family, RAM8NLD-1.8 Technology		
Marketing Part #:	CY62165DV*, CY62167DV*, CY62168DV*, CY62367DV*, CY62177DV30*	
Device Description:	1.8V - 3V, Industrial available in 48-ball FBGA package.	
Cypress Division:	Cypress Semiconductor Corporation –Memory Product Division (MPD)	
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. D
What ID markings on Die:	7C62167D	

TECHNOLOGY/FAB PROCESS DESCRIPTION – RAM8NLD-1.8			
Number of Metal Layers:	2	Metal Composition:	Metal 1: T 150 Å, Al 300 Å, 300 Å Cu Metal 2: Ti 300 Å, Al 8000 Å
Passivation Type and Materials:		1000Å TEOS / 9000Å Si3N4	
Free Phosphorus contents in top glass layer(%):		N/A	
Number of Transistors in Device		~124 million	
Number of Gates in Device		~32 million	
Generic Process Technology/Design Rule (µ-		0.13 µm	
Gate Oxide Material/Thickness (MOS):		32Å	
Name/Location of Die Fab (prime) Facility:		Cypress Semiconductor -- Bloomington, MN	
Die Fab Line ID/Wafer Process ID:		Fab4/RAM8NLD-1.8V	

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY SITE FACILITY
48-ball FBGA	**TAIWN-G**

Note: Package Qualification details upon request

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	BA48
Package Outline, Type, or Name:	48-ball Fine Pitch Ball Grid Array (VFBGA)
Mold Compound Name/Manufacturer:	Toshiba G1270
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>34%
Substrate Material:	BT Resin
Lead Finish, Composition / Thickness:	Solder Ball, 63%Sn, 37%Pb
Die Backside Preparation Method/Metallization:	Backgrind
Die Separation Method:	100%
Die Attach Supplier:	Ablestik
Die Attach Material:	Ablestik 2025D
Die Attach Method:	Epoxy
Bond Diagram Designation:	10-05014
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0um
Thermal Resistance Theta JA °C/W:	73 °C/W
Package Cross Section Yes/No:	N/A
Assembly Process Flow:	49-41032
Name/Location of Assembly (prime) facility:	Taiwan-G

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	**CML-R, KYEC**
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc Max = 2.4V, 125°C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc Max = 2.4V, 150°C	P
High Accelerated Saturation Test (HAST)	130°C, 3.6V, 85%RH Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C / 60%RH, 260°C Reflow	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65°C to 150°C Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C / 60%RH, 260°C Reflow	P
Pressure Cooker	121ºC, 100%RH, 15 Psig Precondition: JESD22 Moisture Sensitivity MSL 3 192 Hrs, 30°C / 60%RH, 260°C Reflow	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V, JESD22-A114E	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	500V, JESD22-C101C	P
Static Latch-up	125°C , ± 200mA, In accordance with JESD78	P
Acoustic Microscopy, MSL 3	J-STD-020	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal AF[4]	Failure Rate
High Temperature Operating Life Early Failure Rate	1,525	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2,] Long Term Failure Rate	409,160 DHRs	0	0.7	170	13 FIT

[1] Assuming an ambient temperature of 55°C and a junction temperature rise of 15°C.

[2] Chi-squared 60% estimations used to calculate the failure rate.

[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism. k = Boltzmann's constant = 8.62x10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

Reliability Test Data

QTP #: 025007

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ACOUSTIC-MSL3							
CY62167DV30L (7C62167D)	4309094	*610316588*	*TAIWN-G*	COMP	15	0	
CY62167DV30L (7C62167D)	4309094	*610316809*	*TAIWN-G*	COMP	15	0	
CY62167DV30L (7C62167D)	4310393	*610318262*	*TAIWN-G*	COMP	45	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE, 125C, 2.4V, Vcc Max							
CY62167DV30L (7C62167D)	4309094	*610316958N*	*TAIWN-G*	96	741	0	
CY62167DV30L (7C62167D)	4306632	*610311763*	*TAIWN-G*	96	784	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE, 150C, 2.4V, Vcc Max							
CY62167DV30L (7C62167D)	4309094	*610316958N*	*TAIWN-G*	80	410	0	
CY62167DV30L (7C62167D)	4309094	*610316958N*	*TAIWN-G*	500	410	0	
CY62167DV30L (7C62167D)	4306632	*610311763*	*TAIWN-G*	80	409	0	
CY62167DV3L0 (7C62167D)	4306632	*610311763*	*TAIWN-G*	500	408	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62167DV30L (7C62167D)	4306632	*610311763*	*TAIWN-G*	COMP	9	0	
CY62167DV30L (7C62167D)	4309094	*610316958*	*TAIWN-G*	COMP	9	0	
CY62167DV18L (7C62367D)	4306632	*610313591*	*TAIWN-G*	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62167DV30L (7C62167D)	4306632	*610311763*	*TAIWN-G*	COMP	9	0	
CY62167DV30L (7C62167D)	4309094	*610316958*	*TAIWN-G*	COMP	9	0	
CY62167DV18L (7C62367D)	4306632	*610313591*	*TAIWN-G*	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 10V, ±300mA							
CY62167DV30L (7C62167D)	4306632	*610311763*	*TAIWN-G*	COMP	3	0	
CY62167DV30L (7C62167D)	4309094	*610316958*	*TAIWN-G*	COMP	3	0	
CY62167DV18L (7C62367D)	4306632	*610313591*	*TAIWN-G*	COMP	3	0	
STRESS: PRESSURE COOKER TEST, 121C, 100%RH, PRE COND 192 HR 30C/60%RH, MSL3							
CY62167DV30L (7C62167D)	4309094	*610316588*	*TAIWN-G*	168	40	0	
CY62167DV30L (7C62167D)	4309094	*610316958*	*TAIWN-G*	168	45	0	
STRESS: HI-ACCEL SATURATION TEST, 130C, 85%RH, 1.98V, PRE COND 192 HR 30C/60%RH, MSL3							
CY62167DV30L (7C62167D)	4309094	*610316588*	*TAIWN-G*	128	44	0	

Reliability Test Data

QTP #: 025007

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: TC COND. C -65C TO 150C, PRECONDITION 192 HRS 30C/60%RH, MSL3							
CY62167DV30L (7C62167D)	4309094	*610316588*	*TAIWN-G*	300	45	0	
CY62167DV30L (7C62167D)	4309094	*610316588*	*TAIWN-G*	500	45	0	
CY62167DV30L (7C62167D)	4309094	*610316588*	*TAIWN-G*	1000	43	0	
CY62167DV30L (7C62167D)	4309094	*610316809*	*TAIWN-G*	300	44	0	
CY62167DV30L (7C62167D)	4309094	*610316809*	*TAIWN-G*	500	44	0	
CY62167DV30L (7C62167D)	4309094	*610316809*	*TAIWN-G*	1000	44	0	
CY62167DV30L (7C62167D)	4310393	*610318262*	*TAIWN-G*	300	45	0	
CY62167DV30L (7C62167D)	4310393	*610318262*	*TAIWN-G*	500	45	0	
CY62167DV30L (7C62167D)	4310393	*610318262*	*TAIWN-G*	1000	45	0	

Reliability Test Data

QTP #:034203

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62167DV30L (7C62167D)	4330158	610345044M	TAIWN-G	COMP	9	0	
CY62367DV30L (7C62367D)	4330158	610345043M	TAIWN-G	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62167DV30L (7C62167D)	4330158	610345044M	TAIWN-G	COMP	9	0	
CY62367DV30L (7C62367D)	4330158	610345043M	TAIWN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 7.9V, **±300mA**							
CY62167DV30L (7C62167D)	4330158	610345044M	TAIWN-G	COMP	3	0	
CY62367DV30L (7C62367D)	4330158	610345043M	TAIWN-G	COMP	3	0	

Reliability Test Data

QTP #:035101

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015, 2,200V							
CY62167DV30L (7C62167D)	4319090	610332912	TAIWN-G	COMP	9	0	
STRESS: ESD-CHARGE DEVICE MODEL, 500V							
CY62167DV30L (7C62167D)	4319090	610332912	TAIWN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING, 125C, 8.5v, ±300mA							
CY62167DV30L (7C62167D)	4319090	610332912	TAIWN-G	COMP	3		

QTP #:083301

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: E-TEST YIELD							
CY62177DV30 (7C62171D)	4829459	N/A	N/A	COMPARABLE			
CY62167DV30 (7C62161D)	4833178	N/A	N/A	COMPARABLE			
CY62167DV30 (7G62161D)	4835716	N/A	N/A	COMPARABLE			
STRESS: SORT YIELD							
CY62177DV30 (7C62171D)	4829459	N/A	N/A	COMPARABLE			
CY62167DV30 (7C62161D)	4833178	N/A	N/A	COMPARABLE			
CY62167DV30 (7G62161D)	4835716	N/A	N/A	COMPARABLE			

Document History Page

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Rev.	ECN No.	Orig. of Change	Description of Change
**	4007536	ILZ	Initial Spec Release Qualification report published on Cypress.com is documented on memo HGA-648 and not in spec format. Initiated spec for QTP 025007 and data from HGA-648was transferred to qualification report spec template

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