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Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

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Cypress Semiconductor
Product Qualification Report

QTP# 012003
June 2013

TIMING TECHNOLOGY - PC PRODUCT TSMC 0.5 TECHNOLOGY TSMC FAB 2B	
W320-03	**200 - MHz Spread Spectrum Clock Synthesizer/ Driver with Differential CPU Outputs**

CYPRESS TECHNICAL CONTACT FOR QUALIFICATION DATA:

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Quality Engineering Director
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PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
005201		New device TT105 - W305B, Frequency Controller with Sys Recovery for Intel Integrated Core Logic in TSMC 0.5um Technology, TSMC fab 2B		Jul 01
012003		New device, TT113 - W320-03, 200 - MHz Spread Spectrum Clock Synthesizer/ Driver with Differential CPU Outputs		Sep 01

PRODUCT DESCRIPTION (for qualification)			
Qualification Purpose: Qualify TT113 - W320 - 03 in TSMC 0.5um Technology, TSMC fab 2B			
Marketing Part #:	W320 - 03		
Device Description:	3.3V, Commercial available in 56-pin SSOP and 56-lead TSSOP package		
Cypress Division:	Cypress Semiconductor Corporation - Timing Technology Division (SJ)		
Overall Die (or Mask) REV Level (pre-requisite for qualification):		Rev. Z	
What ID markings on Die:	TT113 - 320 - 03AA		

TECHNOLOGY/FAB PROCESS DESCRIPTION			
Number of Metal Layers:	2	Metal Composition:	Metal 1: Al-Cu/ /TiN Metal 2: Al-Cu//TiN
Passivation Type and Materials:		PE SiO_2 / PESIN	
Free Phosphorus contents in top glass layer(%):		0%	
Number of Transistors in Device:		30,134	
Number of Gates in Device:		17,658	
Generic Process Technology/Design Rule (-)		CMOS, Single Poly, Double Metal, TSMC 0.50 m Logic	
Gate Oxide Material/Thickness (MOS):		SiO_2 / 85Å	
Name/Location of Die Fab (prime) Facility:		TSMC fab 2B, Hsinchu - Taiwan	
Die Fab Line ID/Wafer Process ID:		TSMC Fab 2B / 05UTW 15LD5	

PACKAGE AVAILABILITY

PACKAGE TYPE	ASSEMBLY SITE FACILITY
56-lead TSSOP / 56-lead SSSOP	**CML-RA TAIWAN –G . TAIWAN – T, CHINA, JCET**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	05615
Package Outline, Type, or Name:	56-lead Shrunk Small Outline Package (SSOP)
Mold Compound Name/Manufacturer:	Sumitomo EME6300HR
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plate, 85%Sn - 15% Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Method:	Epoxy
Die Attach Supplier:	Ablestik
Die Attach Material:	84-1 LMISA
Wire Bond Method:	Thermosonic
Wire Material/Size:	Gold, 1.2mil
Thermal Resistance Theta JA °C/W:	91.87°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	OSE Taiwan

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	KYEC, Taiwan,CML-R
Fault Coverage:	100%

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENTS

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 4.8V, 150ºC	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 4.8V, 150ºC	P
Long Life Verification	Dynamic Operating Condition, Vcc = 4.8V, 150ºC	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65ºC to 150ºC Precondition: JESD22 Moisture Sensitivity MSL 1 168 hrs, 85ºC, 85%RH+3IR-Reflow, 220 ºC +5, -0 ºC	P
High Accelerated Saturation Test (HAST)	130ºC, 85%RH, 3.63V Precondition: JESD22 Moisture Sensitivity MSL 1 168 hrs, 85ºC, 85%RH , 220C+5, -0C Reflow	P
Pressure Cooker	121C, 100%RH Precondition: JESD22 Moisture Sensitivity MSL 1 168 hrs, 85ºC, 85%RH , 220C+5, -0C Reflow	P
Electrostatic Discharge Human Body Model (ESD-HBM)	2,200V/ 2,000V MIL-STD-883, Method 3015.7	P
Acoustic Microscopy	J-STD-020 Precondition: JESD22 Moisture Sensitivity Level	P
Latchup Sensitivity	125ºC, 10V, 300mA In accordance with JEDEC 17	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	2,332 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	298,000 DHRs	0	0.7	170	18 FIT

[1] Assuming an ambient temperature of 55□C and a junction temperature rise of 15□C.
[2] Chi-squared 60% estimations used to calculate the failure rate.
[3] Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism. k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

[4] **EFR Failure Rate and FIT Rate based on QTP #005201.**

Reliability Test Data

QTP #: 005201

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 4.8V, Vcc Max)							
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	48	1320	0	
W305B-OC (W3052A)	B64523	*B64523*	TAIWN-G	48	1012	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 4.8V, Vcc Max)							
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	80	119	0	
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	500	119	0	
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	1000	119	0	
W305B-OC (W3052A)	B64523	*B64523*	AIWN-G	80	120	0	
W305B-OC (W3052A)	B64523	*B64523*	TAIWN-G	500	120	0	
STRESS: LONG LIFE VERIFICATION (150C, 4.8V)							
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	1000	119	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,000V)							
W305B-OC (W3052A)	BR7138	BR7138-8000	TAIWN-G	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 10V, +/300mA)							
W305B-OC (W3052A)	BR0022	BR0022-90100	TAIWN-G	COMP	3	0	
STRESS: ACOUSTIC-MSL1							
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	COMP	15	0	
W305B-OC (W3052A)	BP6870	*BP6870-81*	TAIWN-G	COMP	15	0	
W305B-OC (W3052A)	BR7109	BR7109-21	TAIWN-G	COMP	15	0	
W305B-OC (W3052A)	BR7138	BR7138-8000	TAIWN-G	COMP	15	0	
STRESS: PRESSURE COOKER TEST (121C, 100%RH), PRE COND 168 HR 85C/85%RH,MSL1)							
W305B-OC (W3052A)	B64523	B64523	TAIWN-G	168	48	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 3.63V, PRE COND 168 HR 85C/85%RH,MSL1)							
W305B-OC (W3052A)	B64523	B64523	TAIWN-G	128	48	0	
STRESS: TC COND. C -65C TO 150C, PRECONDITION 168 HRS 85C/85%RH (MSL1)							
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	300	50	0	
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	500	50	0	
W305B-OC (W3052A)	BP6873	*BP6873-11*	TAIWN-G	1000	50	0	
W305B-OC (W3052A)	BP6870	BP6870-81	TAIWN-G	300	50	0	
W305B-OC (W3052A)	BP6870	BP6870-81	TAIWN-G	500	50	0	
W305B-OC (W3052A)	BP6870	BP6870-81	TAIWN-G	1000	50	0	
W305B-OC (W3052A)	B64523	B64523	TAIWN-G	300	48	0	
W305B-OC (W3052A)	B64523	B64523	TAIWN-G	500	48	0	
W305B-OC (W3052A)	B64523	B64523	TAIWN-G	1000	48	0	

Reliability Test Data

QTP #: 012003

Device	Fab Lot #	Assy Lot #	Ass Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
W320-03-OC (W32003Z)	9118396	*610116265*	TAIWN-T	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 10V, +/300mA)							
W320-03-OC (W32003Z)	B64904	*B64904*	TAIWN-T	COMP	3	0	

Document History Page

Document Title: QTP # 012003 : SPREAD SPECTRUM SYNTHESIZER/DRIVER, (TT113 - W320-03), TSMC 0.5UM TECHNOLOGY, TSMC FAB 2B
Document Number: 001-87828

Rev.	ECN No.	Orig. of Change	Description of Change
**	4020459	ILZ	Initial Spec Release Qualification report published on Cypress.com is not in spec format. Initiated spec for QTP 012003 and removed all Cypress reference spec and replaced with Industry standard. Updated package availability based on current qualified assembly

Distribution: WEB

Posting: None