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Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.

Cypress Semiconductor
Product Qualification Report

QTP# 003907 VERSION *A
June 2013

High Frequency Programmable PECL Clock Generator R42LDHA Technology, Fab 4	
CY2213ZC-1	**125-400 MHz**

FOR ANY QUESTIONS ON THIS REPORT, PLEAE CONTACT
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PRODUCT QUALIFICATION HISTORY

Qual Report		Description of Qualification Purpose		Date Comp
98357		New Technology R42D with Hot Al / 1Meg with NoBL Architecture, CY7C1350/CY7C1352		Sep 98
003907		New High Frequency Programmable PECL Clock Generator CY2213ZC-1		Apr 01

PRODUCT DESCRIPTION (for qualification)	
Qualification Purpose: Qualify CY2213ZC-1, R42LDHA technology, Fab 4.	
Marketing Part #:	CY2213ZC-1
Device Description:	3.3V, Commercial available in 16-lead TSSOP Package.
Cypress Division:	Cypress Semiconductor Corporation – Timing Technology Division (ICD) WA
Overall Die (or Mask) REV Level (pre-requisite for qualification):	Rev. A
What ID markings on Die:	7C80810A

TECHNOLOGY/FAB PROCESS DESCRIPTION - R42D			
Number of Metal Layers:	2	Metal Composition:	Metal 1: 500Å TiW/6000Å Al -5%Cu/1200Å TiW Metal 2: 500Å TiW/8000Å Al -5%Cu/300Å TiW
Passivation Type and Materials:			3,000Å SiO_2 + 6000Å Si_3N_4
Free Phosphorus contents in top glass layer (%):			0%
Number of Transistors in Device:			8,000
Number of Gates in Device:			1,400
Generic Process Technology/Design Rule (□-			CMOS, Double Metal /0.35 □m
Gate Oxide Material/Thickness (MOS):			SiO_2 / 70Å
Name/Location of Die Fab (prime) Facility:			Cypress Semiconductor - Bloomington, MN
Die Fab Line ID/Wafer Process ID:			Fab4/R42D (with Hot AL)

PACKAGE AVAILABILITY

PACKAGE	ASSEMBLY FACILITY SITE
16-lead TSSOP	**JT-China, OSE Taiwan,**

MAJOR PACKAGE INFORMATION USED IN THIS QUALIFICATION	
Package Designation:	Z1613
Package Outline, Type, or Name:	16-lead Thin Small Outline Package (TSSOP)
Name Manufacturer / Mold Compound:	Hitachi CEL 9200 IV 77
Mold Compound Flammability Rating:	V-O per UL94
Oxygen Rating Index:	>28%
Lead Frame Material:	Copper
Lead Finish, Composition / Thickness:	Solder Plated, 85%Sn, 15%Pb
Die Backside Preparation Method/Metallization:	N/A
Die Separation Method:	Wafer Saw
Die Attach Supplier:	Ablestik
Die Attach Material:	84-1LMISR4
Wire Bond Method:	Thermosonic
Wire Material/Size:	Au, 1.0 mil
Thermal Resistance Theta JA °C/W:	109.28°C/W
Package Cross Section Yes/No:	N/A
Name/Location of Assembly (prime) facility:	OSE Taiwan (TAIWN-T)

ELECTRICAL TEST / FINISH DESCRIPTION	
Test Location:	KYEC Taiwan
Fault Coverage:	100%

Note: Please contact a Cypress Representative for other packages availability.

RELIABILITY TESTS PERFORMED PER SPECIFICATION REQUIREMENT

Stress/Test	Test Condition (Temp/Bias)	Result P/F
High Temperature Operating Life Early Failure Rate	Dynamic Operating Condition, Vcc = 3.8 V□ 150C	P
High Temperature Operating Life Latent Failure Rate	Dynamic Operating Condition, Vcc = 3.8V□ 150C	P
High Accelerated Saturation Test (HAST)	130C, 85%RH, 3.63V Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235C+5, -0C	P
Temperature Cycle	MIL-STD-883C, Method 1010, Condition C, -65C to 150C Precondition: JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235C+5, -0C	P
Pressure Cooker Test	No bias, 121C, 100%RH Precondition:JESD22 Moisture Sensitivity Level 3 192 Hrs, 30C/60%RH+3IR-Reflow, 235C+5, -0C	P
Electrostatic Discharge Human Body Model (ESD-HBM)	MIL-STD-883, Method 3015.7	P
Electrostatic Discharge Charge Device Model (ESD-CDM)	JESD22-C101C	P
Latchup Sensitivity	125C, 8.5V, ±300mA 125C, 9.9V, ±200mA In accordance with JEDEC 17.	P

RELIABILITY FAILURE RATE SUMMARY

Stress/Test	Device Tested/ Device Hours	# Fails	Activation Energy	Thermal[3] A.F	Failure Rate[4]
High Temperature Operating Life Early Failure Rate	1500 Devices	0	N/A	N/A	0 PPM
High Temperature Operating Life[1,2] Long Term Failure Rate	412,168 DHRs	1	0 .7	170	29 FIT

1 Assuming an ambient temperature of 55C and a junction temperature rise of 15C.
2 Chi-squared 60% estimations used to calculate the failure rate.
3 Thermal Acceleration Factor is calculated from the Arrhenius equation

$$AF = \exp\left[\frac{E_A}{k}\left[\frac{1}{T_2} - \frac{1}{T_1}\right]\right]$$

where:

E_A =The Activation Energy of the defect mechanism.
k = Boltzmann's constant = 8.62×10^{-5} eV/Kelvin.
T_1 is the junction temperature of the device under stress and T_2 is the junction temperature of the device at use conditions.

RELIABILITY TEST DATA

QTP#: 98357

DEVICE	ASSY-LOC	FABLOT#	ASSYLOT#	DURATION	S/S	REJ	FAIL MODE
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-EARLY FAILURE RATE (150C, 3.8V)							
CY7C1350-AC	CSPI-R	4812418	619805770	48	750	0	
CY7C1350-AC	CSPI-R	4815594	619807192	48	684	0	
CY7C1352-AC	CSPI-R	4824383	619809153	48	66	0	
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY7C1352-AC	CSPI-R	4824383	619809153	COMP	3	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (4,400V)							
CY7C1352-AC	CSPI-R	4824383	619809153	COMP	3	0	
STRESS: STATIC LATCH-UP (125C, 9.9V, 200mA)							
CY7C1352-AC	CSPI-R	4824383	619809153	COMP	3	0	
STRESS: HI-ACCEL SATURATION TEST (130C, 85%RH, 3.63V), PRECOND. 192 HRS 30C/60%RH							
CY7C1350-AC	CSPI-R	4816713	619808643	128	48	0	
STRESS: HIGH TEMP DYNAMIC OPERATING LIFE-LATENT FAILURE RATE (150C, 3.8V)							
CY7C1350-AC	CSPI-R	4812418	619805770	80	392	1	1 UNKNOWN
CY7C1350-AC	CSPI-R	4812418	619805770	500	390		0
CY7C1350-AC	CSPI-R	4815594	619807192	80	396		0
CY7C1350-AC	CSPI-R	4815594	619807192	548	396		0
STRESS: PRESSURE COOKER TEST (121C, 100%RH)							
CY7C1352-AC	CSPI-R	4816713	619808642	168	45	0	
CY7C1352-AC	CSPI-R	4816713	619808642	288	45	0	
STRESS: TC COND. C, -65 TO 150C, PRECOND. 192 HRS 30C/60%RH (MSL 3)							
CY7C1350-AC	CSPI-R	4812418	619805769	300	45	0	
CY7C1350-AC	CSPI-R	4812418	619805770	300	45	0	
CY7C1350-AC	CSPI-R	4815594	619807192	300	45	0	

Reliability Test Data

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Device	Fab Lot #	Assy Lot #	Assy Loc	Duration	Samp	Rej	Failure Mechanism
STRESS: ESD-CHARGE DEVICE MODEL (500V)							
CY2213ZC (7C80810A)	4034663	*340000384*	TAIWN-T	COMP	9	0	
CY2213ZC (7C80810A)	4104824	*610107924*	TAIWN-T	COMP	9	0	
STRESS: ESD-HUMAN BODY CIRCUIT PER MIL STD 883, METHOD 3015 (2,200V)							
CY2213ZC (7C80810A)	4034663	*340000384*	TAIWN-T	COMP	9	0	
CY2213ZC (7C80810A)	4104824	*610107924*	TAIWN-T	COMP	9	0	
STRESS: STATIC LATCH-UP TESTING (125C, 8.5V, +/-300mA)							
CY2213ZC (7C80810A)	4034663	*340000384*	TAIWN-T	COMP	3	0	
CY2213ZC (7C80810A)	4104824	*610107924*	TAIWN-T	COMP	3	0	

Document History Page

Document Title: QTP# 003907: High Frequency Programmable PECL Clock Generator "CY2213ZC-1" R42LDHA Technology, Fab 4
Document Number: 001-88051

Rev.	ECN No.	Orig. of Change	Description of Change
**	4035926	HSTO	Initial Spec Release Qualification report published on Cypress.com was transferred to qualification report spec template. Deleted Cypress obsolete referenced spec in Major package qualification details. Deleted Cypress reference Spec and replaced with Industry Standards in Reliability Test Performed Table. Updated package availability based on current qualified test & assembly site.
*A	4432506	HSTO	Align qualification report based on the new template in the front page

Distribution: WEB

Posting: None