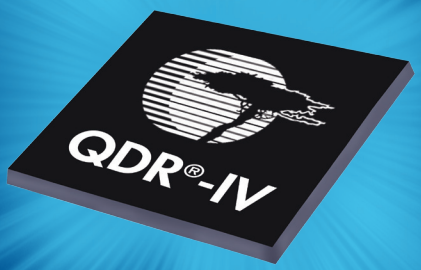
CYPRESS

QDR®-IV SRAM

The Next Generation of the Highest-Performance Memory Standard



PRODUCT OVERVIEW

THE NEXT GENERATION OF THE HIGHEST-PERFORMANCE MEMORY STANDARD

The worldwide leader in SRAM now offers the newest and highest performing member of the consortium-defined QDR® family: QDR-IV. Cypress's QDR-IV SRAM provides Random Transaction Rate (RTR) performance that is orders of magnitude faster than other memories. QDR-IV also brings a number of added benefits to the QDR family, including on-chip ECC and bi-directional ports.

Cypress's QDR-IV is the highest performing standardized memory on the market, and is ideally suited for next-generation networking and high performance computing systems.

QDR-IV FEATURES

- 1066 MHz Frequency (QDR-IV XP)
  667 MHz Frequency (QDR-IV HP)
- 2132 MT/s RTR (QDR-IV XP)
  1334 MT/s RTR (QDR-IV HP)
- 144 Mb or 72 Mb Density
- x18 or x36 Data Bus Width
- 2 Word Burst Length
- 8 Cycle Read Latency (QDR-IV XP)
  5 Cycle Read Latency (QDR-IV HP)
- Two Bi-directional Data Ports
- On-Chip ECC and Address Parity
- Bus Inversion (Programmable)
- Per-Bit Deskew Training
- HSTL/SSTL I/O 1.2 V/1.25 V
  POD I/O 1.1 V/1.2 V
- On-Die Termination (ODT) (Programmable)

Part Number	Product	Frequency (MHz)	RTR (MT/s)	Read Latency	Density (Mbit)	Bus Width
CY7C4122KV13	QDR-IV XP	1066 933	2132 1866	8	144	x18
CY7C4142KV13						x36
CY7C4022KV13					72	x18
CY7C4042KV13						x36
CY7C4121KV13	QDR-IV HP	667 600	1334 1200	5	144	x18
CY7C4141KV13						x36
CY7C4021KV13					72	x18
CY7C4041KV13						x36

RTR = Random Transaction Rate. The rate of random memory access expressed in mega-transactions per second (MT/s) or giga-transactions per second (GT/s)

ADVANTAGES

- High random transaction rate enables higher packet rates
- Two bi-directional data ports allows concurrent access to the memory array to support workloads with unbalanced read/write operations
- On-chip ECC and address parity provides data and address integrity
- Dynamic data and address bus inversion reduces signal noise and power consumption
- Per-bit deskew training improves signal capture at high frequency
- Programmable interface signaling options (HSTL/SSTL and POD) facilitates system design

APPLICATIONS

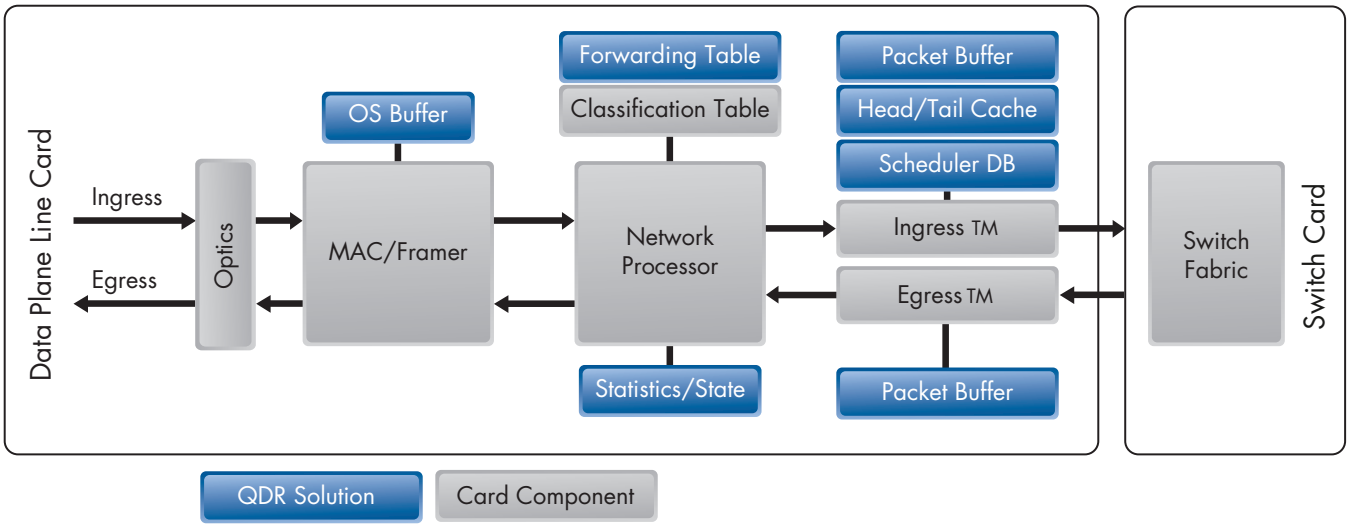
- Networking infastructure
- Enterprise network switches and routers
- High performance computing
- Medical imaging
- Military and aerospace
- Imaging and video

CYPRESS PERFORM

CYPRESS ENABLES THE NEXT GENERATION OF NETWORKING

Streaming video, cloud services, and mobile data have fueled the continuing growth of global network traffic. To support this growth, the next generation of networking systems must provide faster line rates and process millions of packets every second. Packets arrive in a random order and each packet requires several memory transactions to process. In 100 G and higher networking systems, the high flow of packets demands hundreds of millions of memory transactions per second to look up routes from a forwarding table or to update statistics. As a result, packet rates are directly proportional to the rate of random memory access. Next-generation networking equipment requires memories with very high RTR performance to keep pace with ever-increasing network traffic.

Cypress's QDR-IV SRAM is designed specifically for high RTR performance and satisfies the demanding network functions of packet buffering, updating statistics, tracking flow states, scheduling packets, and performing table lookups.



QDR SRAM Solutions for Networking

QDR-IV ARCHITECTURE

The QDR-IV SRAM architecture provides the true random memory access capabilities needed for networking and other high-performance applications. Other common memory technologies are optimized for long bursts of sequential memory access which is not optimal for networking applications. These memory technologies have performance overhead for operations like refreshing charge and activating rows. This overhead forces system designers to replicate memory banks in order to achieve the necessary RTR performance, but memory replication increases board space, cost and power consumption.

With QDR-IV, random memory access performance is guaranteed and there are no delays. QDR-IV SRAM provides read or write access to any memory location on every clock cycle. Performance is constant and does not depend on which memory location was accessed in the previous clock cycle. For networking applications such as statistics and forwarding these capabilities are critical to achieve high network line rates and ensure consistent performance.

GET STARTED NOW

To learn more about QDR-IV and all Cypress Synchronous SRAM products, visit sync.cypress.com.
To purchase QDR-IV parts, visit www.cypress.com/buyonline.

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