

CYPRESS

QDR®-IV SRAM XILINX® VIRTEX® 7 FPGA MEMORY INTERFACE DESIGN



PRODUCT OVERVIEW

INTRODUCTION

The Cypress QDR®-IV SRAM interface design is a fully synthesizable controller and physical layer (PHY) on Xilinx® Virtex®-7 FPGAs. QDR-IV, the latest generation of the high-performance QDR SRAM family, provides a Random Transaction Rate (RTR) of 2132 MT/s on two independent bi-directional data ports.

FUNCTIONAL OVERVIEW

The QDR-IV memory interface design takes user commands clocked at quarter rate, converts them to the QDR-IV protocol at full-rate and provides the converted commands to the QDR-IV memory. The memory interface enables the user to execute concurrent read/write commands on both ports on every cycle facilitating the exceptional RTR performance. Figure 1 shows the top-level QDR-IV memory interface design architecture in a Xilinx Virtex-7 FPGA.

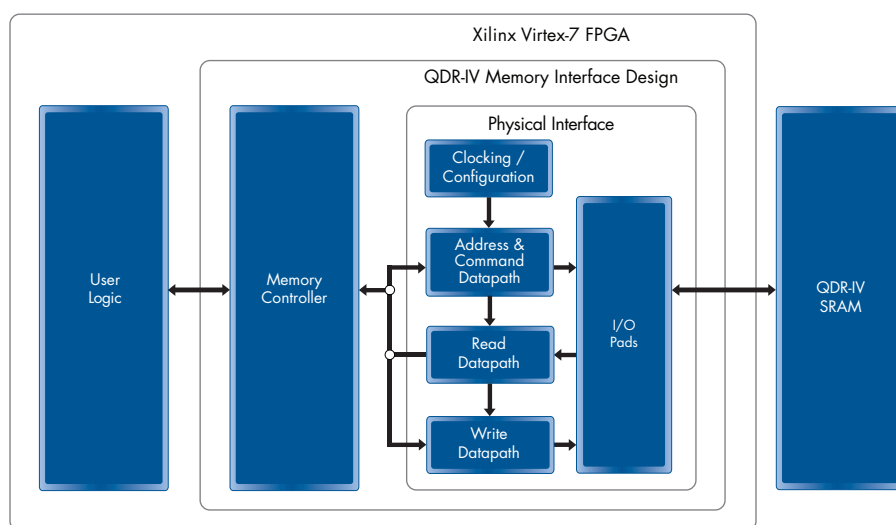


Figure-1: Block Diagram

RTR = Random Transaction Rate. The rate of random memory access expressed in mega-transactions per second (MT/s) or giga-transactions per second (GT/s)

FEATURES

- Reference design for Xilinx Virtex-7 and Kintex-7 FPGAs
- I/O Interface speed of 600 MHz (1200 MT/s RTR) for both QDR-IV HP and QDR-IV XP SRAMs
- x18 and x36 I/O bus width
- 72 Mb and 144 Mb densities
- Two-word burst length operation
- 4:1 ratio between FPGA core and I/O clock rate
- Address bus parity error protection
- Data and address bus inversion to reduce power and simultaneous switching noise
- Single-address port used to control both data ports
 - Double data rate (DDR) address signaling
- Dual independent bi-directional data ports
 - Double data rate (DDR) data
 - Concurrent read/write transactions on both ports
- QDR-IV memory initialization after power-on reset
- Calibration of I/O interface to maximize data capture window by the FPGA

MEMORY CONTROLLER

The User Logic interfaces with the Memory Controller using a simple read/write command protocol. The Memory Controller converts read/write commands from the User Logic to the Physical Interface protocol. All signals are Single Data Rate (SDR) and triggered on the positive edge of the quarter-rate clock in the Memory Controller.

PHYSICAL INTERFACE

The physical interface (PHY) is the core of the memory interface and forms the read and write data paths. It streams DDR data at full clock rate.

The write data path consists of the address, data and control signals necessary to execute a write operation. This path incorporates the OUT_FIFO, PHASER_OUT, PHY_CONTROL and OSERDES primitives available in 7 series FPGAs to implement the DDR write signaling.

The read data path includes the address, data and control signals necessary to execute a read operation. The PHY in the read path center aligns the data output clocks from the QDR-IV SRAM with respect to the data valid window for optimum read data capture. This path incorporates IN_FIFO, PHASER_IN, BUFMR and ISERDES primitives available in 7 series FPGAs to properly secure the DDR read signaling.

Figure 2 shows the QDR-IV SRAM Xilinx Memory Controller validation platform.

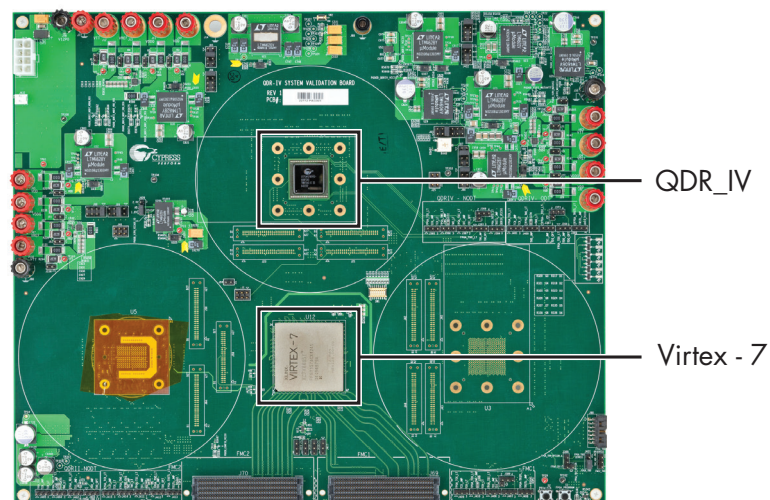


Figure-2: QDR-IV SRAM Xilinx Validation platform

GET STARTED NOW

To learn more about QDR-IV controllers and all Cypress Synchronous SRAM products, visit sync.cypress.com

To purchase QDR-IV parts, visit <http://www.cypress.com/buyonline>

Cypress Semiconductor Corporation

198 Champion Court, San Jose CA 95134
 phone +1 408.943.2600 fax +1 408.943.6848
 toll free +1 800.858.1810 (U.S. only) Press "1" to reach your local sales representative

© 2014-2017 Cypress Semiconductor Corporation. All rights reserved. All other trademarks are the property of their respective owners.
 Doc#001-91218 Rev*A

