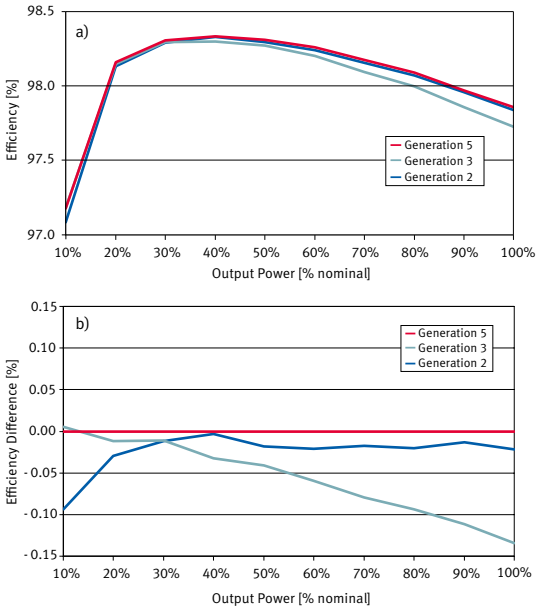
Product Brief

650V SiC thinQ!™ Generation 5 Diodes

Improved Efficiency and Price Performance

ThinQ!™ Generation 5 represents Infineon's leading edge technology for SiC Schottky Barrier diodes. The Infineon proprietary diffusion soldering process, already introduced with G3, is now combined with a new, more compact design and thin wafer technology. The result is a new family of products showing improved efficiency over all load conditions, coming from both the improved thermal characteristics and a lower figure of merit (Q_c x V_F).

The new thinQ!™ Generation 5 has been designed to complement our 650V CoolMOS™ families, this ensures meeting the most stringent application requirements in this voltage range.



Experimental results
Efficiency comparison among the three IFX generations of 8A SiC diodes
a) Absolute values
b) Referred to thinQ!™ Gen 5
(CCM PFC, High line,
P_{out} max = 1800W, f_{SW} = 65kHz,
T_{HS} = 60°C, MOSFET: IPW60R075CP)

Key Features

- V_{BR} at 650V
- Improved Figure of Merit (Q_c x V_F)
- No reverse recovery charge
- Soft switching reverse recovery waveform
- Temperature independent switching behavior
- High operating temperature ($T_{j\ max}$ = 175°C)
- Improved surge current capability

Key Benefits

- Higher safety margin against overvoltage; best match with CoolMOS™ products
- Improved efficiency over all load conditions
- Reduced EMI
- Highly stable switching performance
- Reduced cooling requirements and increased system reliability

Applications

- Telecom / Server
- Solar / UPS
- PC Silverbox
- LED / LCD TV
- Motor Drives
- HID lighting

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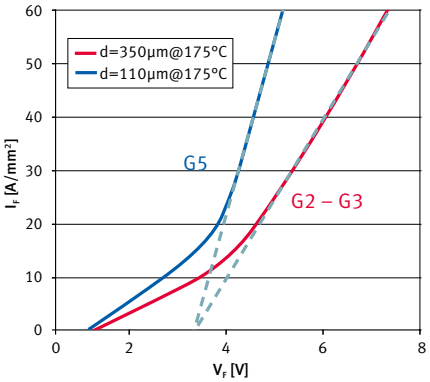
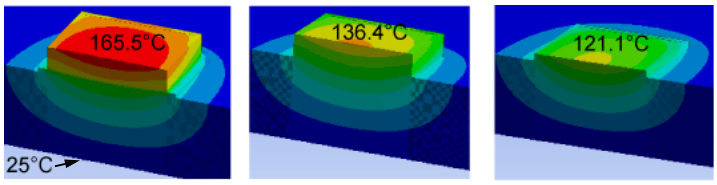
An important achievement with Gen 5 is the industrial implementation of a thinning process which allows reducing the wafer thickness to almost 1/3 while maintaining the proven quality and yield levels. The thinning reduces the resistive contribution of the substrate (see picture on the right) and one of its most striking benefits is a consistent improvement of the surge current robustness, now at comparable level or even higher (for I_F <10A) than that for G2 in spite of a smaller chip size. In combination with our proprietary diffusion soldering, the reduced thickness further contributes to decrease the overall thermal resistance in the package. The pictures below show the temperature increase at the junction under given forward current conditions for the same device area.



Left: 350µm chip with 60µm soft solder; middle: 350µm chip with diff. solder; right: 110µm chip with diff. solder



Product Portfolio

I_F [A]	TO-220 R2L	TO-247	D²PAK R2L	ThinPAK 8x8
2	IDH02G65C5		IDK02G65C5	IDL02G65C5
3	IDH03G65C5		IDK03G65C5	
4	IDH04G65C5		IDK04G65C5	IDL04G65C5
5	IDH05G65C5		IDK05G65C5	
6	IDH06G65C5		IDK06G65C5	IDL06G65C5
8	IDH08G65C5		IDK08G65C5	IDL08G65C5
9	IDH09G65C5		IDK09G65C5	
10	IDH10G65C5	IDW10G65C5	IDK10G65C5	IDL10G65C5
12	IDH12G65C5	IDW12G65C5	IDK12G65C5	IDL12G65C5
16	IDH16G65C5	IDW16G65C5		
20	IDH20G65C5	IDW20G65C5		
30		IDW30G65C5		
40		IDW40G65C5		

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