Professional Education Seminar S17

Practical Application of 600 V GaN HEMTs in Power Electronics

Monday March 16, 2015  8:30 – 12:00

Eric Persson, GaN Applications
Seminar Outline

- Limitations of today’s 600 V Silicon
- Topologies where superjunction performs well
- Topologies where superjunction application is limited
- GaN HEMT characteristics
  - Depletion-mode, cascode, enhancement-mode
  - GaN applied to hard and soft-switching topologies
- Gate drive considerations for GaN
- PFC Application examples
  - Standard boost, dual boost, totem-pole bridgeless
- LLC converter example
- ZVS phase-shifted full-bridge example
- Motor drive example
What needs improvement?

For same Rds(on), improve all the charge parameters:

- Reduce Coss nonlinearity
  - Nonlinearity makes timing and dv/dt control challenging
- Reduce Qoss (and therefore Eoss) magnitude
- Reduce Coss dissipation factor
- Improve body diode dynamic performance
  - Reduce/eliminate Qrr
- Reduce gate charge
- All of the above at affordable cost
Topologies where superjunction works well

- Unipolar current flow, hard or soft-switched
- Two-transistor forward
  - Hard switched, partial valley switched
- Boost PFC
  - CCM or CrCM
- Flyback
  - Hard switched, partial valley switched

- Why?
  - Superjunction has low \( \text{Rds(on)} \times \text{Eoss} \) figure of merit
  - Body diode performance is not important
2-Transistor Forward Converter (2TF)
2TF voltage and current waveforms

Ref: Thierry Sutto, “2 switch forward current mode converter,” ON semi app note AND8373/D
2TF FET turn-on loss measurement

Ref: Thierry Sutto, “2 switch forward current mode converter,” ON semi app note AND8373/D
2TF FET turn-on loss analysis

- This accounts for the “crossover” loss
  - Where the transistor is supporting simultaneous V and I

- What is missing?
- This suggests that if \( \Delta t \) goes to 0, Turn-on loss = 0

Ref: Thierry Sutto, “2 switch forward current mode converter,” ON semi app note AND8373/D
What about the Eoss of the FET itself?

Equivalent Circuit

Simplified Schematic

Current Commutation
Qsw Discharge

Note: This is not Qrr
2TF FET turn-off loss

- Turn-off losses limited entirely by gate drive
  - If you can turn-off the gate extremely fast, get ZVS

Ref: Thierry Sutto, “2 switch forward current mode converter,” ON semi app note AND8373/D
2 Transistor Forward Summary

- This is a unipolar topology
  - Superjunction already works well
  - Body diode performance is unimportant

- Switch losses are dominated by:
  - Conduction
  - Turn-on speed
  - Eoss
  - Turn-off speed

- Possible switch improvements
  - For a given $R_{ds(on)}$:
    - Reduced Eoss (stored energy in device $C_{oss}$)
    - Reduced $Q_g$ to enable faster switching
Flyback Converter

- Avalanche risk

![Diagram of Flyback Converter]

Vin

Vds

Vgs

Measure

Value

P1 freq(C1) | 47.0535 kHz
P2 freq(C2) | 47.9612 kHz
P3 width(C1) | 2.2407 µs
P4 min(C4) | 1.82 A
P5 max(C4) | 1.39 A
P7... | 
P8... | 

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Flyback turn-on timing is critical

- Eoss dissipated proportional to $V_{ds}^2$
- Strong dependence on timing turn-on to waveform
  - Turning on at peak versus valley – big difference in Eoss
Flyback Summary

- This is a unipolar topology
  - Superjunction already works well
  - Body diode performance is unimportant
  - Avalanche or overvoltage capability likely necessary

- Switch losses are dominated by:
  - Conduction
  - Turn-on speed
  - Eoss (valley switching can minimize loss)
  - Turn-off speed

- Possible switch improvements
  - For a given Rds(on):
  - Reduced Eoss (stored energy in device Coss)
  - Reduced Qg to enable faster switching
Standard boost PFC

- $S_B$ typically superjunction
- $D_B$ SiC Schottky for lowest loss
- Can achieve >96% efficiency

Standard boost PFC

- **Typical operating frequency** <70 kHz
  - Keep fundamental and 2\(^{nd}\) harmonic below 150 kHz EMI
  - Increasing frequency increases switching loss

- **Control mode typically Continuous Conduction Mode**
  - CCM balances ripple current losses and switching loss

- **Can be operated Discontinuous or Critical mode**
  - Much higher ripple current
  - But ZVS or near ZVS possible, much lower switching loss

- **Either way, dominant loss is input bridge rectifier**
  - 1-2% total efficiency loss due to input bridge
  - Even a “perfect” zero loss switch can’t make-up for bridge
Standard boost PFC summary

- This is a unipolar topology
  - Superjunction already works well
  - Body diode performance is unimportant

- Switch losses are dominated by:
  - Conduction (especially severe for high ripple CrCM and DCM)
  - Turn-on speed
  - Eoss (only for CCM)
  - Turn-off speed

- Possible switch improvements
  - For a given Rds(on):
    - Reduced Eoss (stored energy in device Coss)
    - Reduced Qg to enable faster switching
What about bridgeless PFC topologies?

- Dual boost – semi bridgeless
- S1 S2 commonly superjunction, D1 D2 SiC

Dual boost PFC summary

- This is a unipolar topology
  - Superjunction already works well
  - Body diode performance is unimportant

- Switch losses are dominated by:
  - Conduction (especially severe for high ripple CrCM and DCM)
  - Turn-on speed
  - Eoss (only for CCM)
  - Turn-off speed

- Possible switch improvements
  - For a given Rds(on):
    - Reduced Eoss (stored energy in device Coss)
    - Reduced Qg to enable faster switching

Tradeoff: eliminate 1 diode drop, add an entire boost stage
Why not totem-pole PFC with superjunction?

- Hard-switched half-bridge requires good body-diode

Hard-switched half-bridge

\[ V_{SW} = V_{DS(Q2)} \]

\[ I_L \]

\[ I_{Q2} \]

\[ I_{Q1} \]

\[ P(t)_{Q2} \]

This is Q1 Eoss. Q2 Eoss discharge current is internal, not seen externally.
Summary: topologies with limited superjunction use

- Bipolar current flow topologies
  - Anywhere diode recovery is important
- Half-bridge hard-switching
  - Totem-pole bridgeless boost CCM (except line polarity switch)
  - Inverters, motor drives
- Half-bridge soft-switching or resonant? Depends...
  - Limited frequency range
  - Risk of hard-switching
  - Frequency dependent losses in Qoss
GaN High Electron Mobility Transistor (HEMT)

- Depletion-mode basic HEMT
  - Normally-on is a problem for power electronics
- 2 methods to achieve normally-off
  - Cascode
  - Enhancement-mode

- GaN cascode characteristics
- GaN enhancement-mode characteristics
- GaN application summary
  - Hard-switching
  - Soft-switching & resonant
GaN High Electron Mobility Transistor (HEMT)

- Depletion-mode (normally-on) HEMT
- Si substrate for low cost
- Normally-on potential problem for power electronics

Depletion-mode HEMT

- Normally-on
  - Essentially a resistor that can be turned-off with -gate bias
  - Potential issues with power-up and power-down
  - Requires additional master enable switch
  - Requires negative gate drive

- Low area specific on-resistance

- Bi-directional conduction
  - No intrinsic body diode

- Can be made bi-directional blocking

- Lateral device – monolithic integration possibilities
Cascode Provides Normally-OFF Function

- Native d-mode GaN HEMT + LV Si FET in cascode
  - $R_{ds(on)}$ is compromised to shift threshold positive
- Cascode has easy gate drive
- Cascode includes excellent body diode
- 2-chip solution no more difficult than IGBT
- Almost zero "Miller Effect"
  - $C \frac{dv}{dt}$ immunity
  - Enables turn-off ZVS in almost any topology

Depletion-Mode GaN HEMT

Low Voltage Si MOSFET

Hybrid Semiconductor Device, US Pat. 8,017,978
Hybrid semiconductor device having a GaN transistor and a Silicon MOSFET, US Pat. 8,368,120
Cascode Conduction Modes

Body diode reverse-recovery

- >100x lower Qrr for GaN cascode
Comparing GaN cascode to superjunction

1st Generation GaN cascode

<table>
<thead>
<tr>
<th>Parameter</th>
<th>GaN cascode</th>
<th>Equivalent SJ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package</td>
<td>6x8 mm PQFN</td>
<td>8x8 mm PQFN</td>
</tr>
<tr>
<td>Vdss</td>
<td>600 V</td>
<td>650 V</td>
</tr>
<tr>
<td>Rdson typ 25°C</td>
<td>135 mΩ</td>
<td>115 mΩ</td>
</tr>
<tr>
<td>Rdson typ 125°C</td>
<td>225 mΩ</td>
<td>230 mΩ</td>
</tr>
<tr>
<td>Qg (10V Vgs, 480V Vds)</td>
<td>8.8 nC</td>
<td>35 nC</td>
</tr>
<tr>
<td>Qrr (100A/μs, 25°C)</td>
<td>49 nC</td>
<td>6,400 nC</td>
</tr>
<tr>
<td>Coss (400V)</td>
<td>47 pF</td>
<td>53 - 579 pF</td>
</tr>
<tr>
<td>Rθ J-C (°C/W)</td>
<td>1.65</td>
<td>1.22</td>
</tr>
</tbody>
</table>
Turn-on waveform, 135 mΩ (typ) cascode

- Hard-switching $R_g = 2\Omega$. $\sim 9 \mu J \, E_{ON}$
GaN HEMT Safe Operating Area

- Measured destruct current >2x higher than calculated thermal limit

Lines represent calculated thermal limit – points are measured failures

Experimental data from 190 mΩ max cascode prototype
GaN performance interdependent on package

- Two key factors for minimizing losses:
  - Minimize GaN – Si interconnect inductance
  - Eliminate common-source inductance with Kelvin connection

Die-on-die cascode construction

- Minimizes parasitic impedance between HEMT and FET
  - Faster switching transitions, less ringing and overshoot
E-mode GaN HEMT Structures

a) P-gate enhancement-mode
b) P-gate enhancement-mode (gate injection)

Enhancement-Mode HEMT (Gate Injection)

Gate Characteristics (Enhancement Mode)

- Typical non-insulated gate characteristic
  - Gate injection uses small DC current (e.g. 10 mA)

Output Characteristics (Enhancement Mode)

- HEMT turns back ON when drain goes below G, S

Reverse Bias Diode-Like Behavior

Equivalent Circuit when $V_g = 0$

$S' = \text{drain acting as source in reverse bias}$

$D' = \text{source acting as drain in reverse bias}$

$V_{GS'} = V_{D'S'}$
Forward and Reverse I-V Characteristics

- HEMT eventually saturates at very high current

GaN, superjunction, (& SiC) transfer curves

- Cascode superjunction and SiC ~135 mΩ typical
- E-mode GaN (non GIT) ~50mΩ (135 mΩ @ 150 ºC)
Comparing GaN vs SJ Qoss

Fig. 5, Comparison of the charge stored in the output capacitance $Q_{oss}$ for different CoolMOS devices and potential SiC and GaN devices.

Comparing Coss, Qoss, Eoss GaN vs SJ

Blue = superjunction
Red = e-mode HEMT
Both ~70 mΩ max Rds(on)
Comparing GaN vs superjunction turn-off

- LLC topology looking at low-side switch
  - 400 V bus, 2 A
  - Same Rds(on)
Avalanche and overvoltage

- Superjunction has junction with avalanche capability
  - Useful in circuits with unclamped inductive energy (flyback)
- GaN has no junction, no avalanche behavior
  - GaN ultimately breaks down destructively at ~2x rating
  - Overvoltage spikes are allowed depending on supplier
- GaN is best suited for half-bridge topology
  - Fast body diode helps to mitigate overvoltage spikes
  - Overvoltage spikes are clamped to bus
  - With proper design, no risk of breakdown
GaN Device Summary

- Both cascode and enhancement mode – compared to superjunction:
  - Provides MUCH lower Qrr (zero for e-mode)
    - Enables use of efficient half-bridge topologies
  - Provide smaller, more linear Qoss
    - Reduces deadtime in resonant and ZVS circuits
  - Provide lower gate charge Qg
    - Lower gate drive power and faster switching speed
  - Eoss not much difference
  - Does not have avalanche behavior
    - Does have overvoltage capability
Applications of GaN
Gate Drive

- Cascode – standard Si gate drivers work
  - $V_{gs(th)}$ is potential issue
  - Common Source Inductance is a concern as always
  - $C \frac{dv}{dt}$ induced gate currents
  - Kelvin gate-source connections
  - Advantages of floating gate drive
Gate drive challenges for low threshold devices

- Common Source Inductance distorts \( V_{gs} \)
- Kelvin source connection eliminates CSI
- ...BUT can cause system grounding problems for driver
Isolated gate drive + Kelvin source connection

- Isolating both high and low-side drivers solves system ground bounce issues which can affect current sense and logic ground.
Gate drive for gate injection

A: high current for fast turn-on
B: low steady state current to remain in ON state
C: high negative current for fast turn-off

A: high voltage overdrive
B: steady state
C: negative voltage to avoid re-turn on

Gate drive summary

- **Cascode GaN:**
  - Standard FET gate driver compatibility
  - Lower $Q_g$ for given current-handling capability
  - ZVS turn-off easier to achieve

- **Enhancement-mode GaN**
  - Low threshold, noise sensitivity, negative drive can help
  - Tighter limits on $V_{gs}$
  - *Very* low $Q_g$
  - Kelvin source connection mandatory
  - Floating driver helpful especially at higher power
This half-bridge is GaN cascode

This half-bridge is superjunction
Totem-Pole PFC Full-Bridge

- 2.5 kW all SMD power stage proof-of-concept
- GaN boost stage 70 mΩ max enhancement-mode
- superjunction sync line rectifiers

Bottom View of PCB
Totem-Pole PFC Full-Bridge

- Input $230 \, V_{AC}$
- Output $400 \, V_{DC}, \, 6.25 \, A$
- CCM 45 to 65 kHz
Totem-Pole PFC full-bridge performance

- >99% efficiency from 18-70% load

Graph showing measured efficiency for PFC with $V_{in}=230VAC$, $P_{out}$ vs. efficiency.

Complete Power Stage. $V_{in}=230V$, $T_{amb}=25^\circ C$
Totem Pole PFC

- No diode drops – only switch conduction voltage
- Very high efficiency possible >99%
- Lower component count than other bridgeless topologies
- Topology is enabled by GaN HEMT
  - Traditional Si FETs have too much body-diode Qrr
  - Large recovery currents and high losses
- Topology is Intrinsically bi-directional power flow
  - Can also be used in inverter/UPS applications
Totem Pole PFC Future

- MHz ZVS – still achieving 99% efficiency
- Multiphase architectures to minimize ripple
- Digital control to optimize performance & efficiency

LLC Resonant DC-DC

- Popular topology today using superjunction
- Frequency range <200 kHz typically
- Caution required to prevent hard-switching
LLC typical waveforms and circuit
GaN enables shorter deadtime vs SJ @ 1MHz

- Shorter deadtime lowers rms current

<table>
<thead>
<tr>
<th></th>
<th>I² Primary</th>
<th>I² Secondary</th>
<th>Gate Drive</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN</td>
<td>3.84A²</td>
<td>48.0A²</td>
<td>0.24W</td>
</tr>
<tr>
<td>Superjunction</td>
<td>4.93A²</td>
<td>64.6A²</td>
<td>1.88W</td>
</tr>
<tr>
<td>Difference</td>
<td>+28.3%</td>
<td>+34.6%</td>
<td>+685%</td>
</tr>
</tbody>
</table>
Nonlinear Qoss Charge Affects Deadtime

3.3X longer charge-up time

Qoss Measurement Circuit

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Cascode Charge Balance During ZVS Turn-ON

Improper charge balance results in loss of ZVS

- Significant energy loss

Properly balanced Cascode achieves full ZVS

- No energy loss


Measured Results: IR-Infineon Cascode
Cascode Charge Balance During ZVS Turn-OFF

Improper charge balance results in Si avalanche

- Significant energy loss

Properly balanced Cascode no avalanche, full ZVS

- No energy loss

ZVS phase-shifted full-bridge

- ZVS over most of power range except light-load
- Current-doubler output effective for 12 V and below
ZVS phase-shifted full-bridge

- 1 kW 380 V to 12 V
- 350 kHz
- 120 W/in$^3$
ZVS phase-shifted full-bridge

- Waveforms at 50% load
ZVS phase-shifted full-bridge efficiency

Efficiency vs Percentage Load

380V to 12V
fsw = 350 kHz

<table>
<thead>
<tr>
<th>Load</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>10%</td>
<td>89.5%</td>
</tr>
<tr>
<td>20%</td>
<td>94%</td>
</tr>
<tr>
<td>40%</td>
<td>96.1%</td>
</tr>
<tr>
<td>50%</td>
<td>96.4%</td>
</tr>
<tr>
<td>80%</td>
<td>96.3%</td>
</tr>
<tr>
<td>100%</td>
<td>95.7%</td>
</tr>
</tbody>
</table>
Efficiency vs Frequency at half-load

- Comparing GaN cascode vs superjunction

<table>
<thead>
<tr>
<th>Freq [Khz]</th>
<th>Efficiency_GaN [%]</th>
<th>Efficiency_SJ [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>96.7</td>
<td>96.5</td>
</tr>
<tr>
<td>200</td>
<td>96.5</td>
<td>96.2</td>
</tr>
<tr>
<td>300</td>
<td>96.4</td>
<td>95.4</td>
</tr>
<tr>
<td>350</td>
<td>96.3</td>
<td>95.0</td>
</tr>
<tr>
<td>400</td>
<td>95.9</td>
<td>94.0</td>
</tr>
<tr>
<td>450</td>
<td>95.6</td>
<td></td>
</tr>
<tr>
<td>500</td>
<td>95.4</td>
<td></td>
</tr>
</tbody>
</table>

![Graph showing efficiency vs frequency](image-url)
Why GaN for Motor Drive Applications?

- Switching speed is not necessarily a key issue for drives:
  - Typically want $dv/dt < 6V/ns$ (GaN can switch $>10x$ faster)
    - $I=C\ dv/dt$ currents in motor windings can result in failures
    - Corona and partial-discharge creates ozone and erodes insulation
    - Common-mode currents forced through bearings, eroding races
- Yet customers still want higher efficiency, increased density
- Compressor drives have even more constraints:
  - Very low leakage current mandates small $Y$-cap values (EMI)
  - Newer “green” refrigerants have very high permittivity
- Goal is to improve light-load efficiency ($<25\%$ of full power)
- EU2013 directive for Energy Saving A+++ Class
- Reducing losses also improves packaging density
Typical Compressor Drive Today

![Diagram of a typical compressor drive system]

- **EMI FILTER**
- **LINE INPUT**
- **INPUT RECTIFIER**
- **DC BUS CAP**
- **BIAS POWER SUPPLY**
- **CONTROL & PWM**
- **GATE DRIVERS**
- **OUTPUT INVERTER**
- **AC MOTOR**
Comparing Conduction voltage of IGBT vs FET (measured data)

- IRGR4045D
- 0.8Ω Si
- 0.16Ω GaN

Conduction Voltage for Same Footprint Size
Total Power Loss Summary (per switch)

- **Si FET**
  - Conduction: 0.60
  - Turn-off: 0.20
  - Turn-on: 0.20
  - Fixed: 0.00

- **IGBT**
  - Conduction: 1.00
  - Turn-off: 0.40
  - Turn-on: 0.20
  - Fixed: 0.40

- **GaN cascode**
  - Conduction: 0.10
  - Turn-off: 0.10
  - Turn-on: 0.10
  - Fixed: 0.10

Watts loss @ Iout = 1A rms
Cascode GaN $dv/dt$ control via Gate Modulation

- $dv/dt$ control possible by modulating cascode gate-drive current
- This places HEMT in linear region increasing switching times and losses
- Unknown if this affects long-term reliability – further study needed
GaN HEMT Short-Circuit Capability

- Initial devices are high-gain – limited SC SOA
  - Typically ~ 1 µs @ 300V
- Likely tradeoff between gain and SC SOA similar to IGBTs

Ref: Xing Huang; Dong Young Lee; Bondarenko, V.; Baker, A.; Sheridan, D.C.; Huang, A.Q.; Baliga, B.J., "Experimental study of 650V AlGaN/GaN HEMT short-circuit safe operating area (SC SOA)," Proc. ISPSD pp.273,276, 15-19 June 2014
Summary

- GaN HEMTs offer performance improvements for power electronic applications
  - Benefits are strongly topology-dependent
  - Just dropping GaN into existing circuit may show little benefit

- Half-bridge topology is good match for GaN
  - Half-bridge requires good dynamic reverse conduction
  - Both cascode and e-mode GaN devices benefit half-bridge

- Higher efficiency at same frequency
  - By use of better topologies i.e. totem-pole PFC

- Higher frequency at high efficiency
  - Lower charge of GaN helps HF performance
  - E.g. LLC example and ZVS full-bridge example
Questions?
References


9) Xing Huang; Dong Young Lee; Bondarenko, V.; Baker, A.; Sheridan, D.C.; Huang, A.Q.; Baliga, B.J., "Experimental study of 650V AlGaN/GaN HEMT short-circuit safe operating area (SCSOA)," Proc. ISPSD pp.273,276, 15-19 June 2014