Professional Education Seminar **S17**

Practical Application of 600 V GaN HEMTs in Power Electronics

Monday March 16, 2015 8:30 – 12:00

Eric Persson, GaN Applications

IOR infineon

Seminar Outline

- Limitations of today's 600 V Silicon
- Topologies where superjunction performs well
- Topologies where superjunction application is limited
- GaN HEMT characteristics
  - Depletion-mode, cascode, enhancement-mode
  - GaN applied to hard and soft-switching topologies
- Gate drive considerations for GaN
- PFC Application examples
  - Standard boost, dual boost, totem-pole bridgeless
- LLC converter example
- ZVS phase-shifted full-bridge example
- Motor drive example

What needs improvement?

For same Rds(on), improve all the charge parameters:

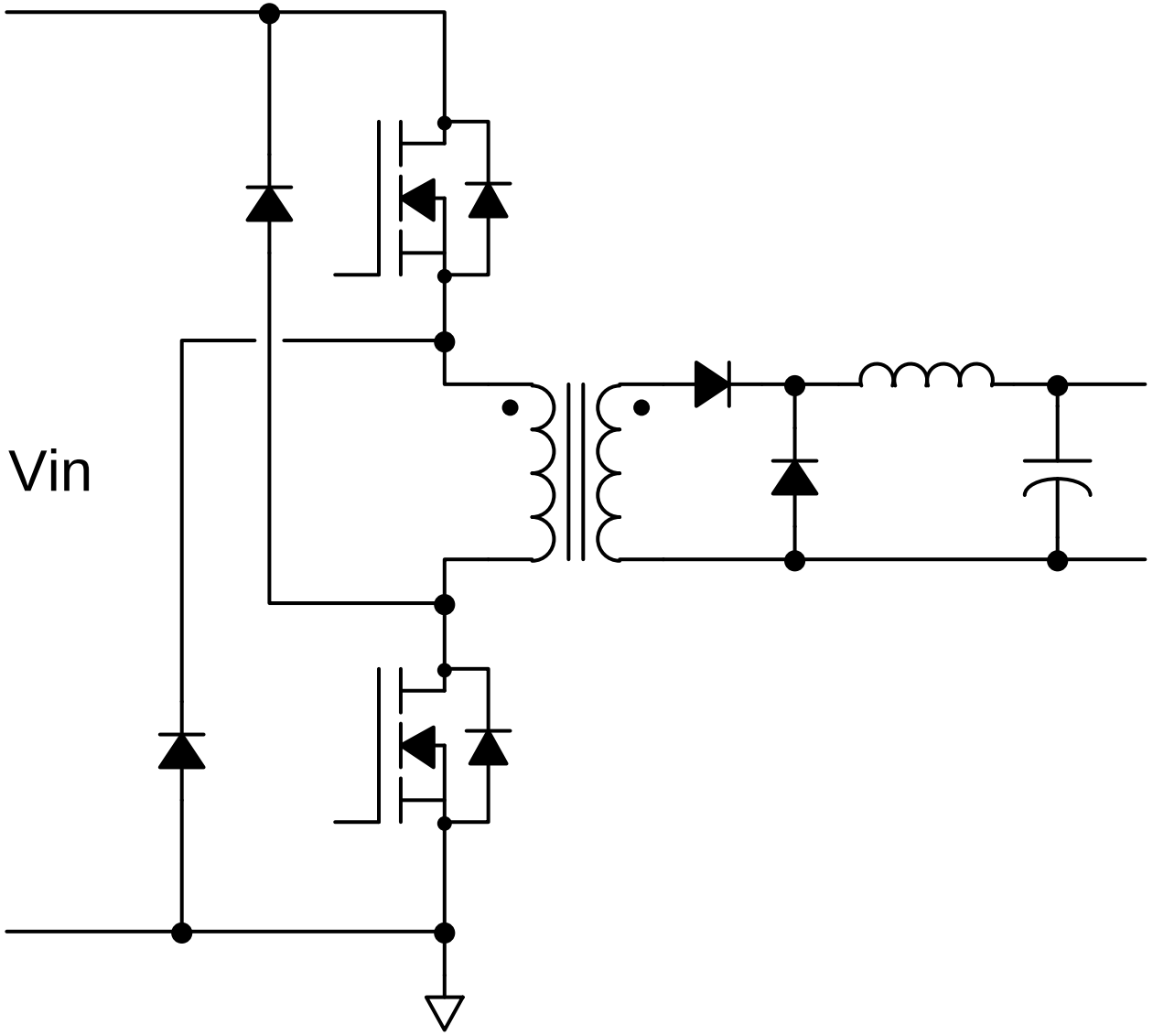
- Reduce Coss nonlinearity
  - Nonlinearity makes timing and dv/dt control challenging
- Reduce Qoss (and therefore Eoss) magnitude
- Reduce Coss dissipation factor
- Improve body diode dynamic performance
  - Reduce/eliminate Qrr
- Reduce gate charge
- All of the above at affordable cost

Topologies where superjunction works well

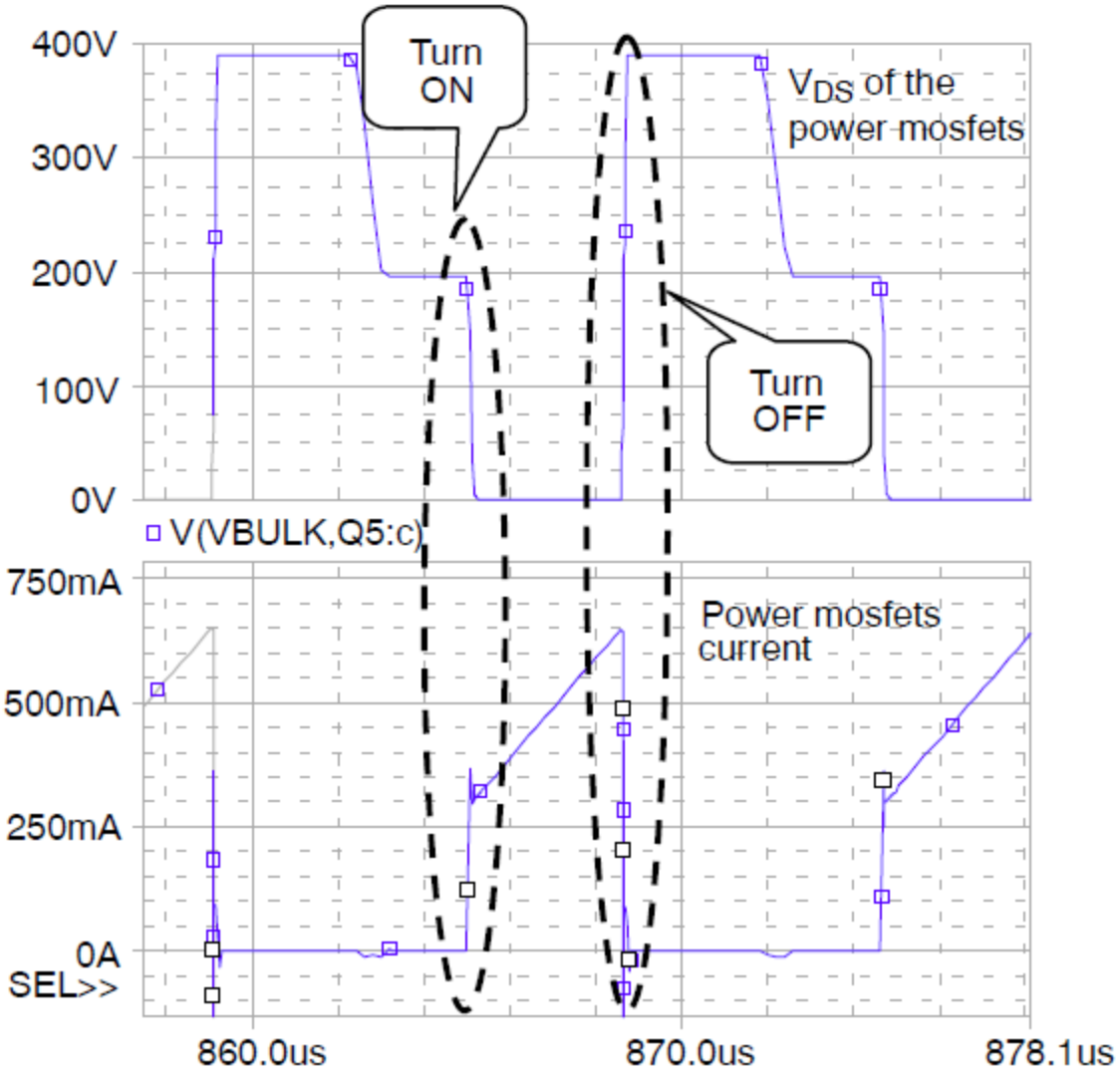
- Unipolar current flow, hard or soft-switched
- Two-transistor forward
  - Hard switched, partial valley switched
- Boost PFC
  - CCM or CrCM
- Flyback
  - Hard switched, partial valley switched

- Why?
  - Superjunction has low Rds(on)*Eoss figure of merit
  - Body diode performance is not important

2-Transistor Forward Converter (2TF)

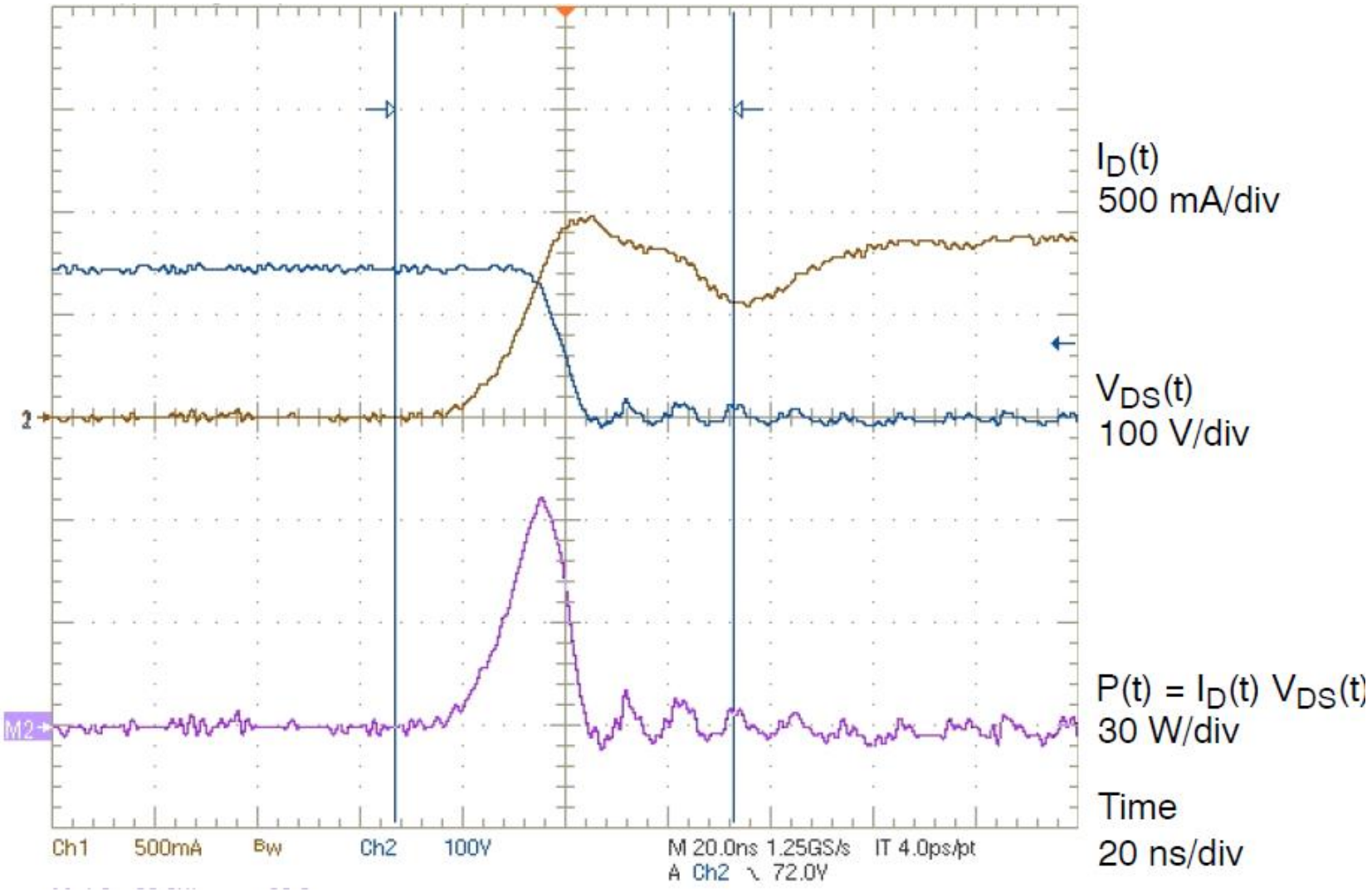


2TF voltage and current waveforms



Ref: Thierry Sutto, "2 switch forward current mode converter," ON semi app note AND8373/D

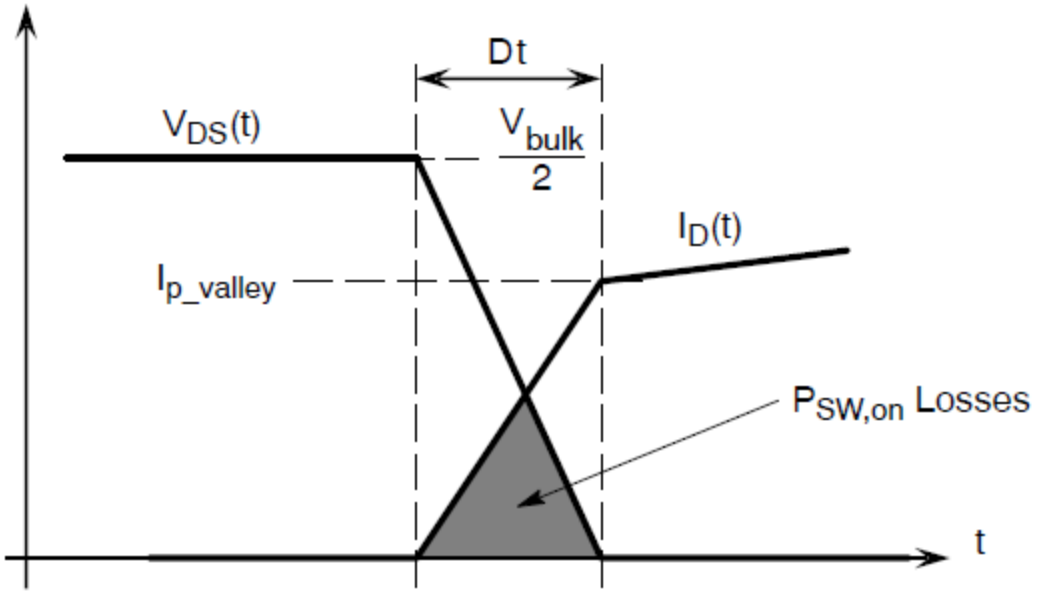
2TF FET turn-on loss measurement



Ref: Thierry Sutto, "2 switch forward current mode converter," ON semi app note AND8373/D

2TF FET turn-on loss analysis

- This accounts for the "crossover" loss
  - Where the transistor is supporting simultaneous V and I



$$P_{SW,on} = F_{sw} \int_0^{\Delta t} I_D(t) V_{DS}(t) dt$$

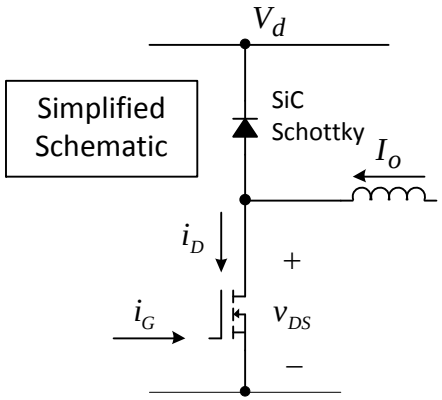
$$= \frac{I_{p\_valley} \frac{V_{bulk}}{2} \Delta t}{6} F_{sw}$$

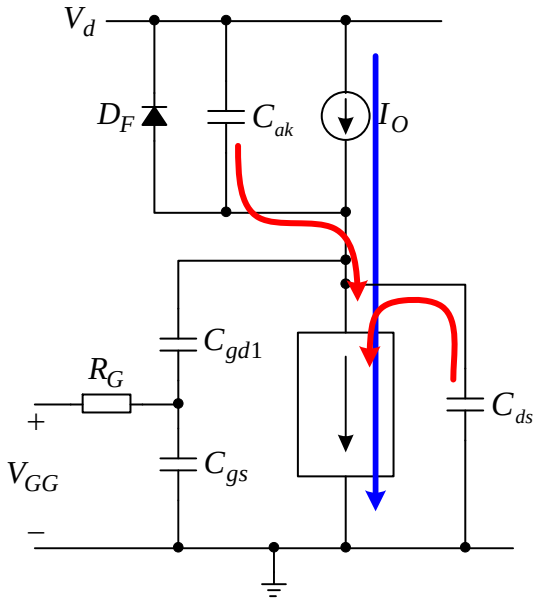
$$P_{SW,on} = \frac{I_{p\_valley} V_{bulk} \Delta t}{12} F_{sw}$$

- What is missing?
- This suggests that if Δt goes to 0, Turn-on loss = 0

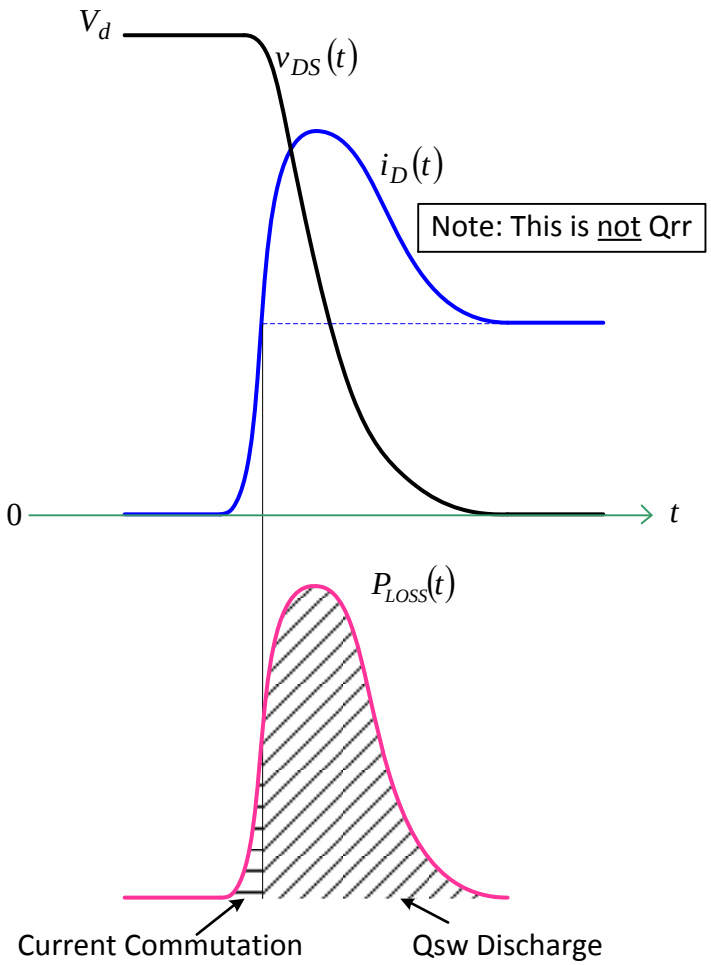
Ref: Thierry Sutto, "2 switch forward current mode converter," ON semi app note AND8373/D

What about the Eoss of the FET itself?



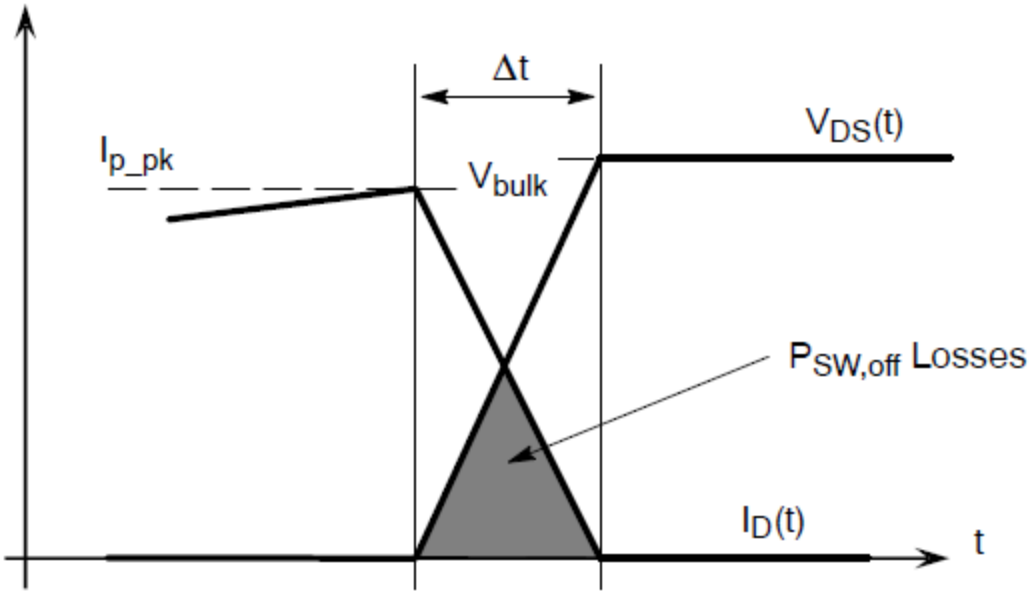


Equivalent Circuit



2TF FET turn-off loss

- Turn-off losses limited entirely by gate drive
  - If you can turn-off the gate extremely fast, get ZVS

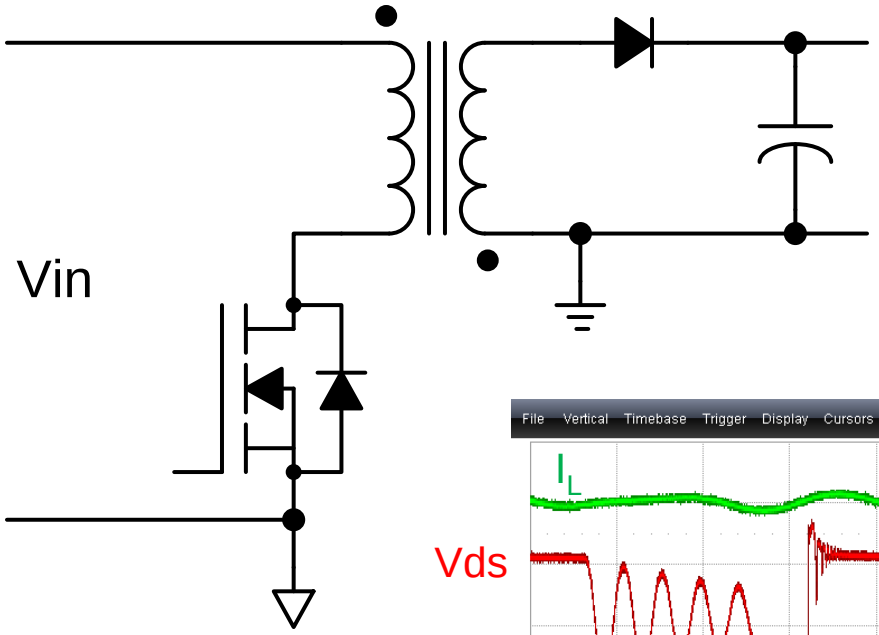


Ref: Thierry Sutto, "2 switch forward current mode converter," ON semi app note AND8373/D

2 Transistor Forward Summary

- This is a unipolar topology
  - Superjunction already works well
  - Body diode performance is unimportant
- Switch losses are dominated by:
  - Conduction
  - Turn-on speed
  - Eoss
  - Turn-off speed
- Possible switch improvements
  - For a given Rds(on):
  - Reduced Eoss (stored energy in device Coss)
  - Reduced Qg to enable faster switching

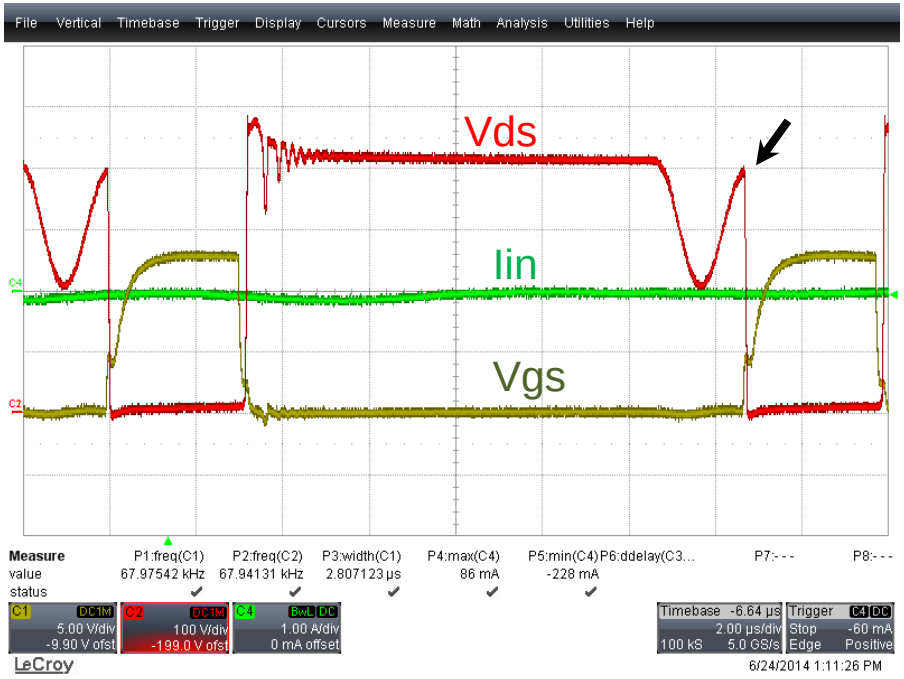
Flyback Converter

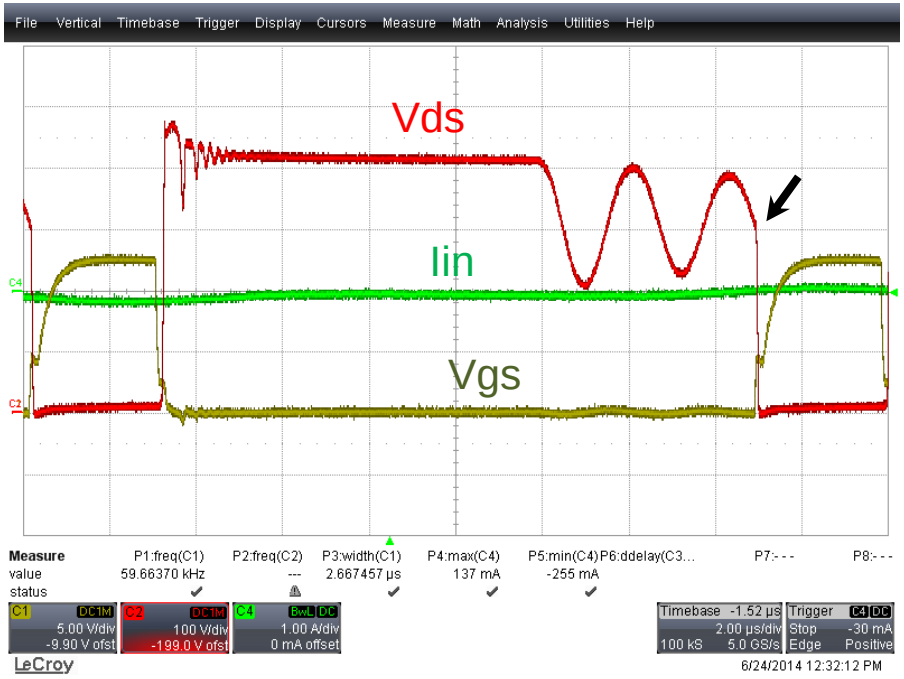


- Avalanche risk

Flyback turn-on timing is critical

- Eoss dissipated proportional to Vds^2
- Strong dependence on timing turn-on to waveform
  - Turning on at peak versus valley – big difference in Eoss



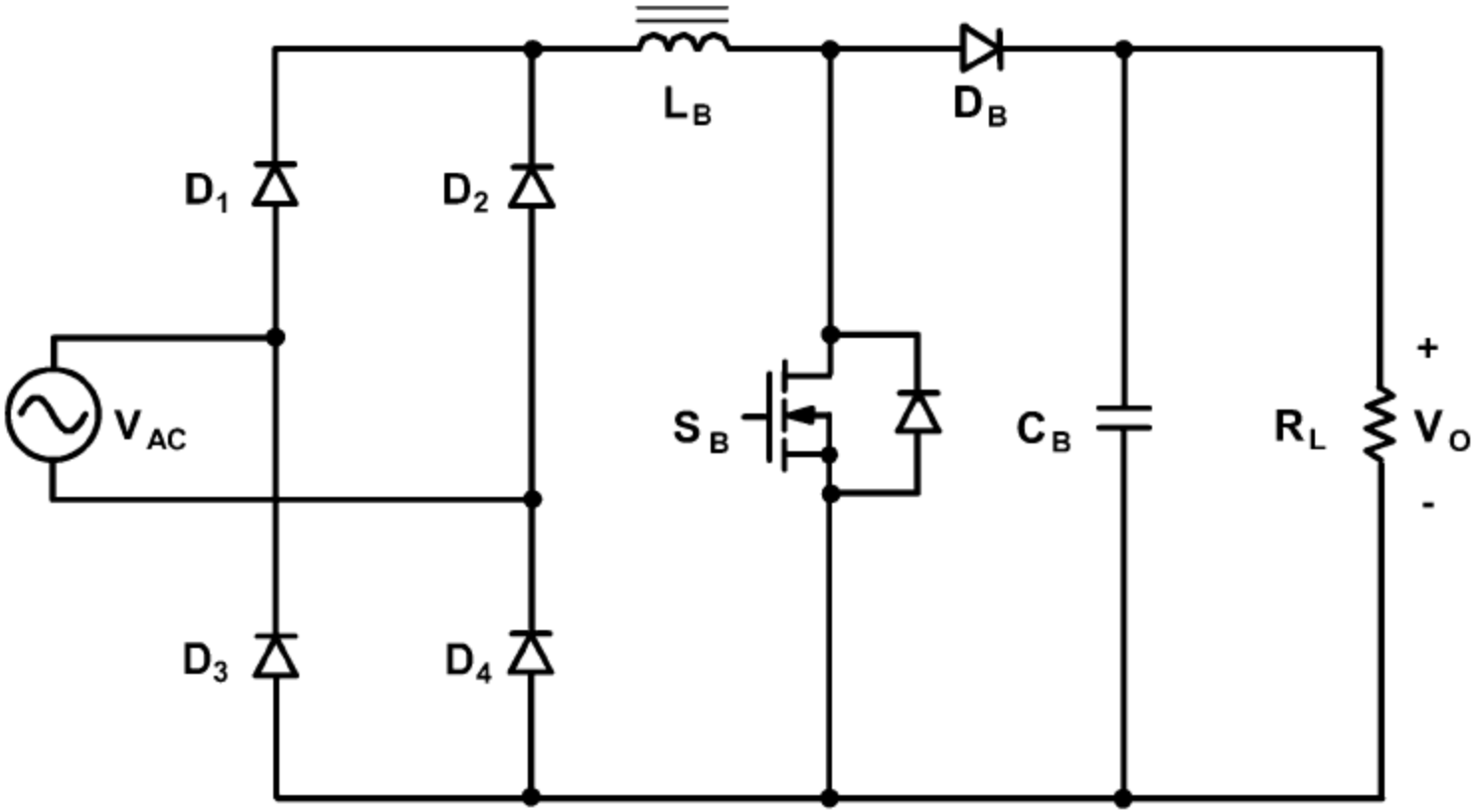


Flyback Summary

- This is a unipolar topology
  - Superjunction already works well
  - Body diode performance is unimportant
  - Avalanche or overvoltage capability likely necessary
- Switch losses are dominated by:
  - Conduction
  - Turn-on speed
  - Eoss (valley switching can minimize loss)
  - Turn-off speed
- Possible switch improvements
  - For a given Rds(on):
  - Reduced Eoss (stored energy in device Coss)
  - Reduced Qg to enable faster switching

Standard boost PFC

- S_B typically superjunction
- D_B SiC Schottky for lowest loss
- Can achieve >96% efficiency



REF: L. Huber, Y. Jang, M. Jovanovic, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 23, NO. 3, MAY 2008

Standard boost PFC

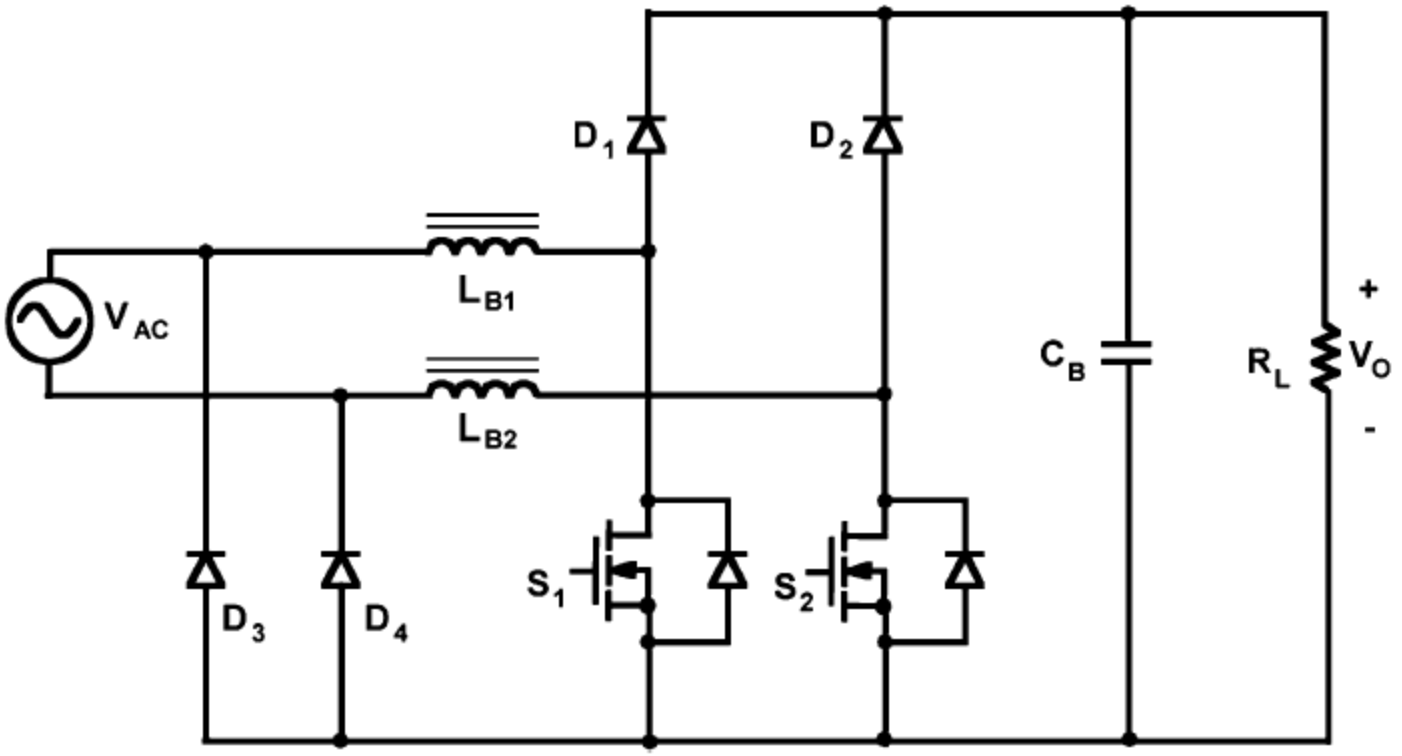
- Typical operating frequency <70 kHz
  - Keep fundamental and 2nd harmonic below 150 kHz EMI
  - Increasing frequency increases switching loss
- Control mode typically Continuous Conduction Mode
  - CCM balances ripple current losses and switching loss
- Can be operated Discontinuous or Critical mode
  - Much higher ripple current
  - But ZVS or near ZVS possible, much lower switching loss
- Either way, dominant loss is input bridge rectifier
  - 1-2% total efficiency loss due to input bridge
  - Even a "perfect" zero loss switch can't make-up for bridge

Standard boost PFC summary

- This is a unipolar topology
  - Superjunction already works well
  - Body diode performance is unimportant
- Switch losses are dominated by:
  - Conduction (especially severe for high ripple CrCM and DCM)
  - Turn-on speed
  - Eoss (only for CCM)
  - Turn-off speed
- Possible switch improvements
  - For a given Rds(on):
  - Reduced Eoss (stored energy in device Coss)
  - Reduced Qg to enable faster switching

What about bridgeless PFC topologies?

- Dual boost – semi bridgeless
- S1 S2 commonly superjunction, D1 D2 SiC



Ref: A. F. Souza and I. Barbi, "High power factor rectifier with reduced conduction and commutation losses," in *Proc. Int. Telecommunication Energy Conf.*, Jun. 1999, pp. 8.1.1–8.1.5.

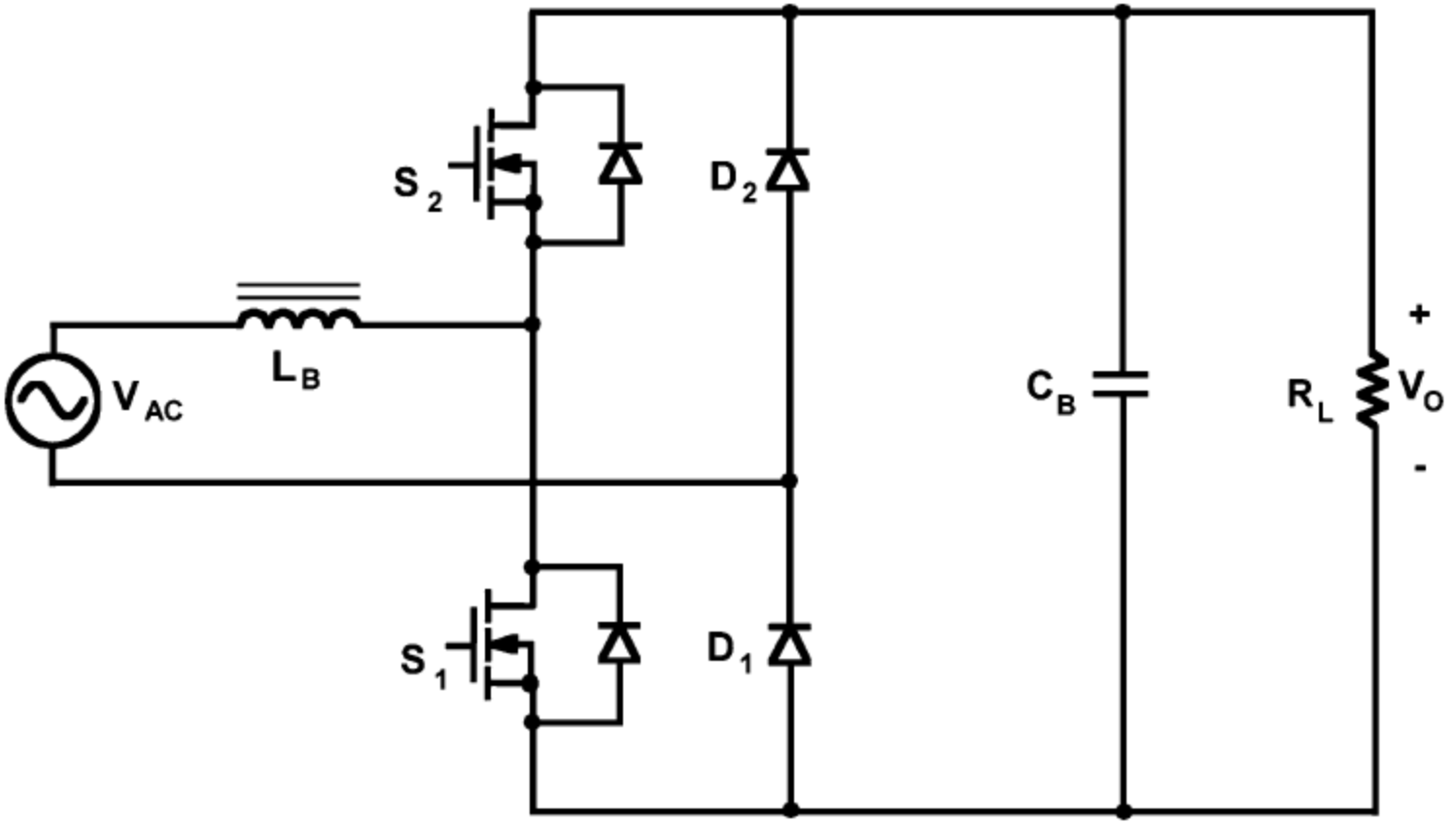
Dual boost PFC summary

- This is a unipolar topology
  - Superjunction already works well
  - Body diode performance is unimportant
- Switch losses are dominated by:
  - Conduction (especially severe for high ripple CrCM and DCM)
  - Turn-on speed
  - Eoss (only for CCM)
  - Turn-off speed
- Possible switch improvements
  - For a given Rds(on):
  - Reduced Eoss (stored energy in device Coss)
  - Reduced Qg to enable faster switching

Tradeoff: eliminate 1 diode drop, add an entire boost stage

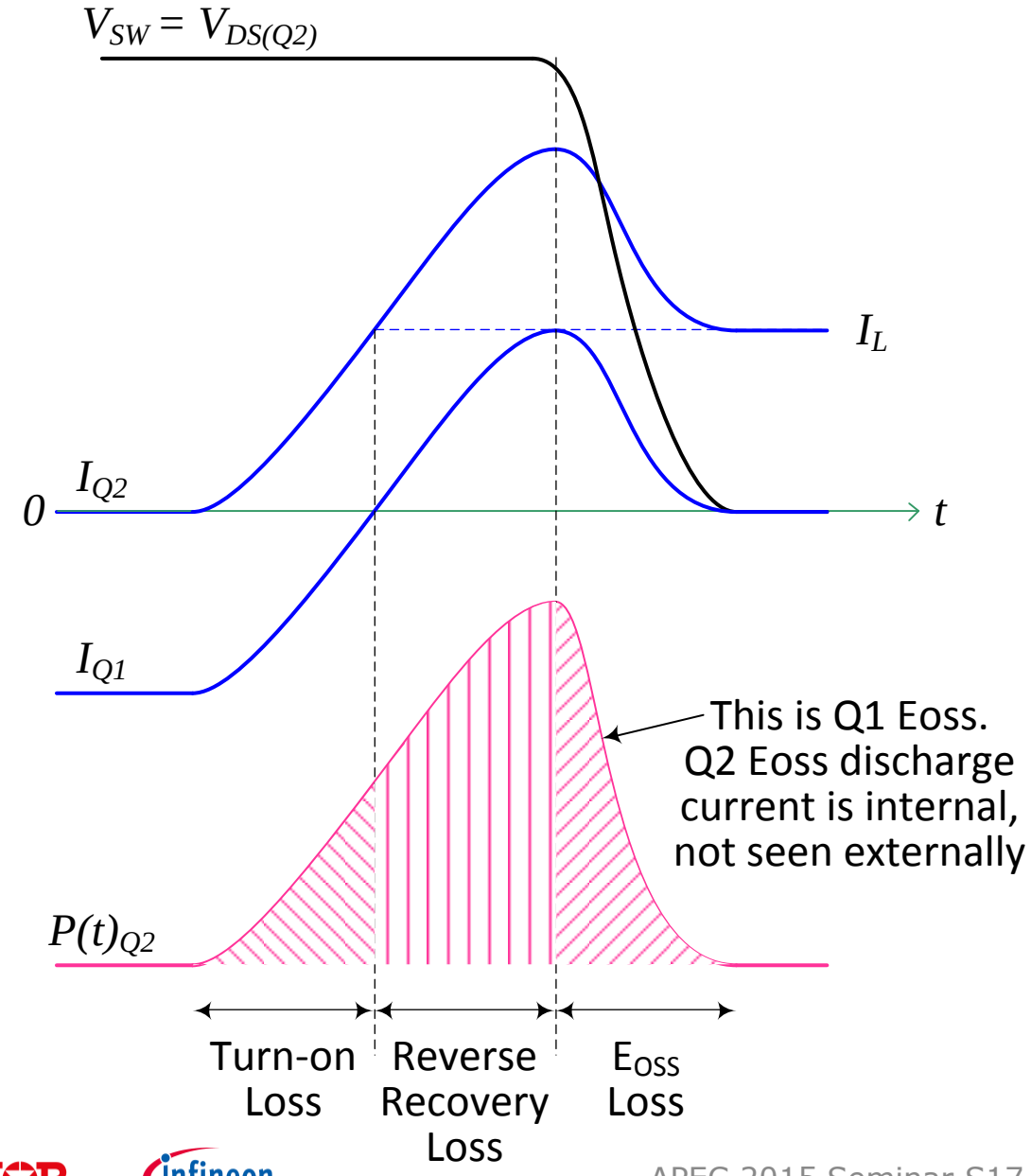
Why not totem-pole PFC with superjunction?

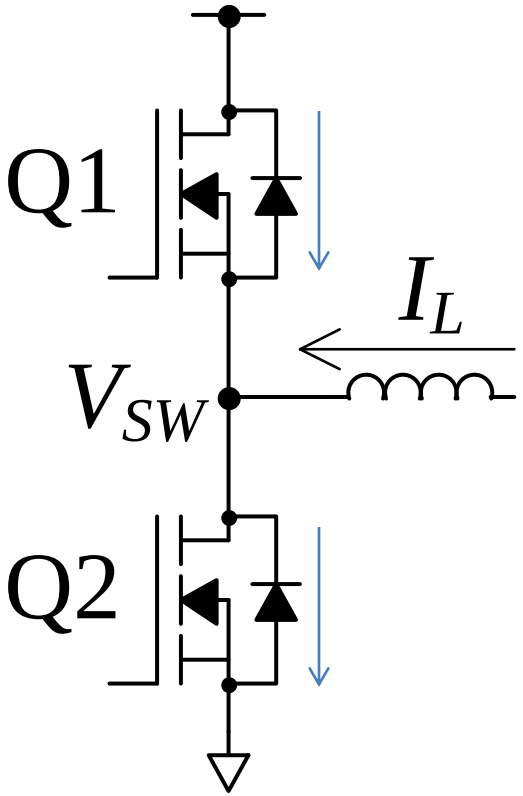
- Hard-switched half-bridge requires good body-diode



REF: J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase ac supplies and using either single or split dc rail voltage outputs," *APEC*, Mar. 1995, pp. 473–479.

Hard-switched half-bridge





Summary: topologies with limited superjunction use

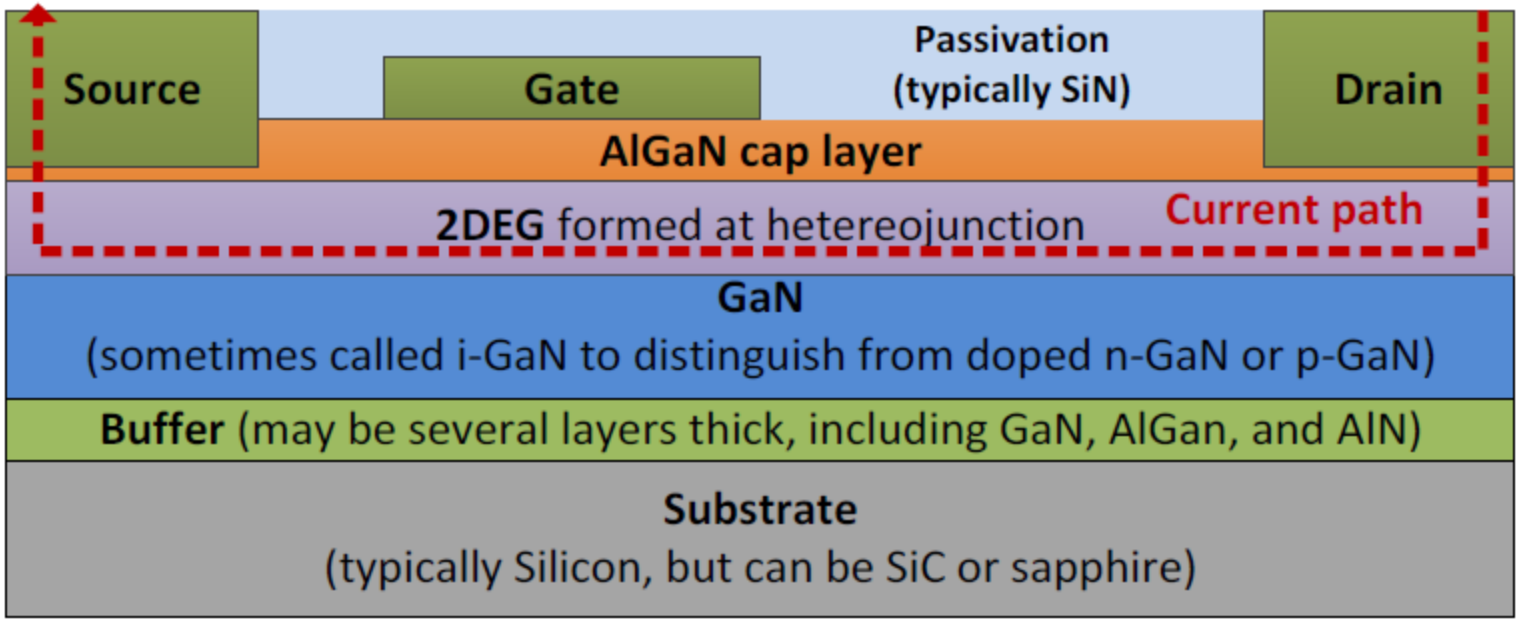
- Bipolar current flow topologies
  - Anywhere diode recovery is important
- Half-bridge hard-switching
  - Totem-pole bridgeless boost CCM (except line polarity switch)
  - Inverters, motor drives
- Half-bridge soft-switching or resonant? Depends…
  - Limited frequency range
  - Risk of hard-switching
  - Frequency dependent losses in Qoss

GaN High Electron Mobility Transistor (HEMT)

- Depletion-mode basic HEMT
  - Normally-on is a problem for power electronics
- 2 methods to achieve normally-off
  - Cascode
  - Enhancement-mode
- GaN cascode characteristics
- GaN enhancement-mode characteristics
- GaN application summary
  - Hard-switching
  - Soft-switching & resonant

GaN High Electron Mobility Transistor (HEMT)

- Depletion-mode (normally-on) HEMT
- Si substrate for low cost
- Normally-on potential problem for power electronics



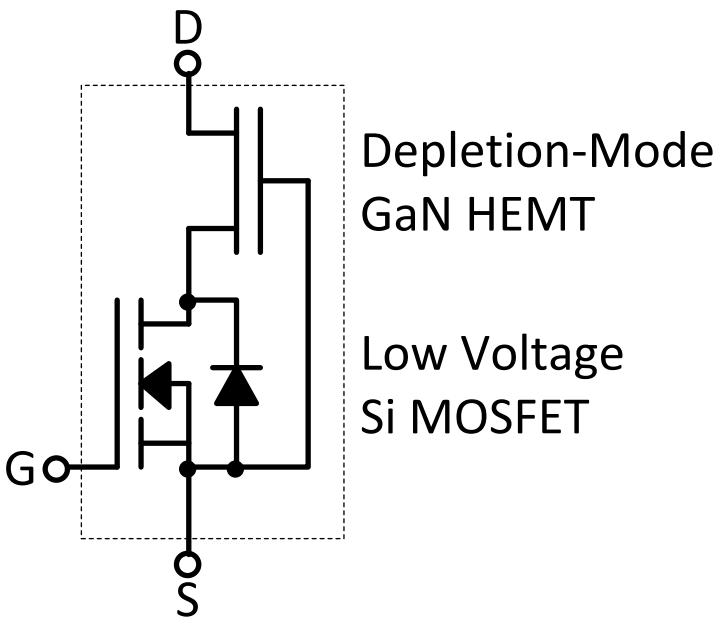
Ref: Jones, E.A.; Wang, F.; Ozpineci, B., "Application-based review of GaN HFETs," Wide Bandgap Power Devices and Applications (WiPDA) 2014, pp.24-29, 13-15 Oct. 2014

Depletion-mode HEMT

- Normally-on
  - Essentially a resistor that can be turned-off with -gate bias
  - Potential issues with power-up and power-down
  - Requires additional master enable switch
  - Requires negative gate drive
- Low area specific on-resistance
- Bi-directional conduction
  - No intrinsic body diode
- Can be made bi-directional blocking
- Lateral device – monolithic integration possibilities

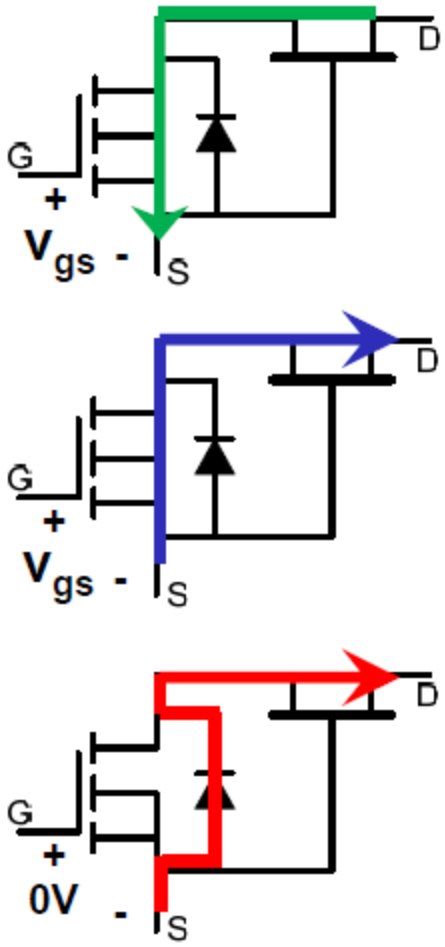
Cascode Provides Normally-OFF Function

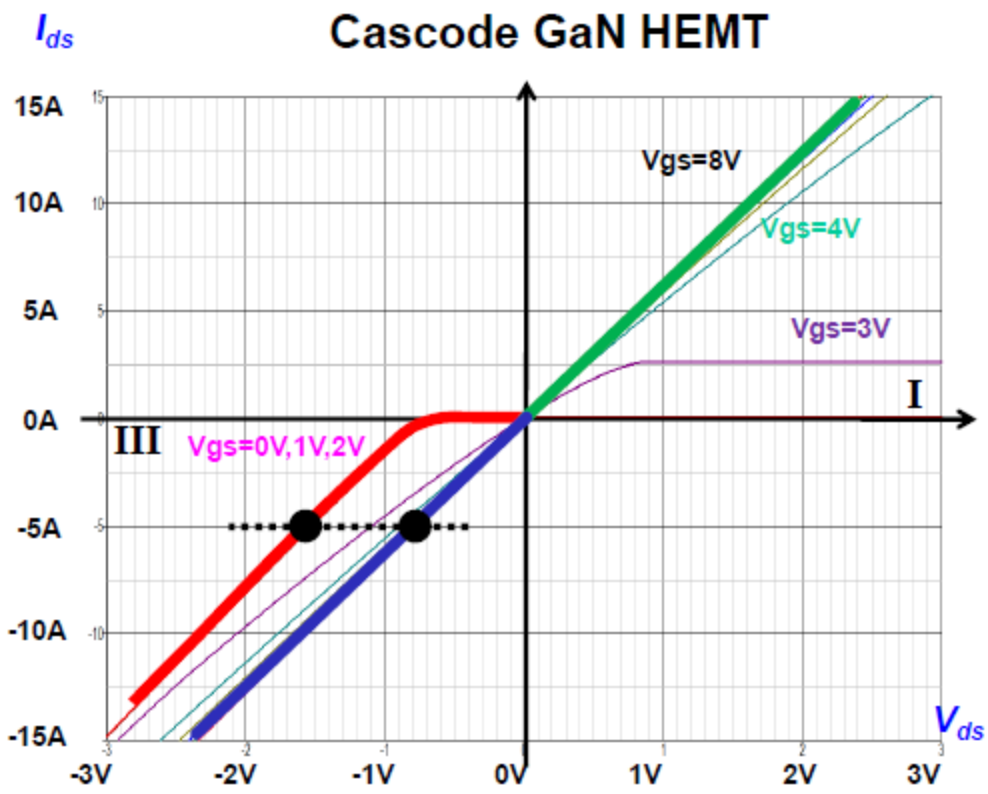
- Native d-mode GaN HEMT + LV Si FET in cascode
  - Rds(on) is compromised to shift threshold positive
- Cascode has easy gate drive
- Cascode includes excellent body diode
- 2-chip solution no more difficult than IGBT
- Almost zero "Miller Effect"
  - C dv/dt immunity
  - Enables turn-off ZVS in almost any topology



Hybrid Semiconductor Device, US Pat. 8,017,978
Hybrid semiconductor device having a GaN transistor and a Silicon MOSFET, US Pat. 8,368,120

Cascode Conduction Modes

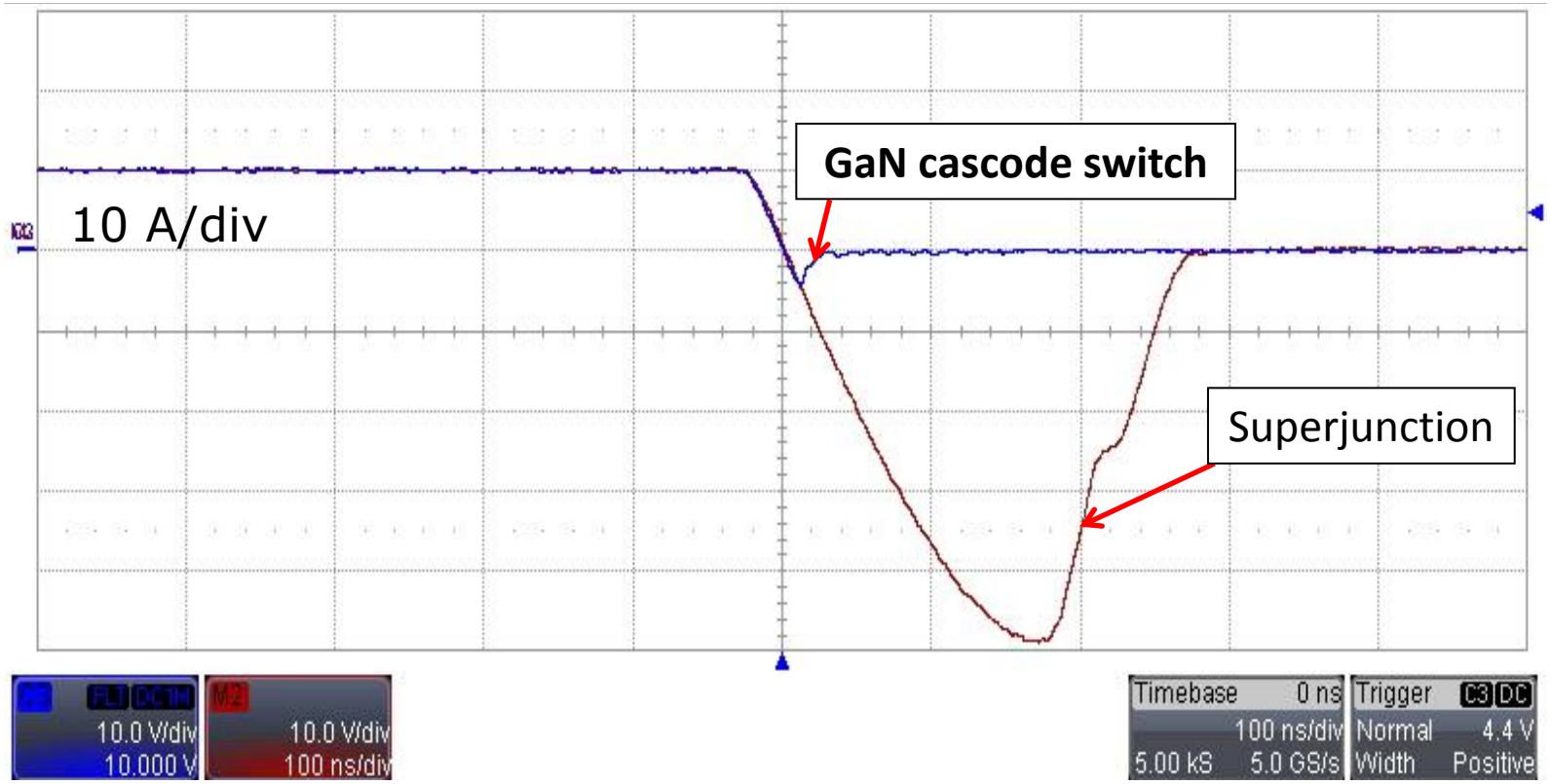




Ref: Xiucheng Huang, Fred C. Lee, Qiang Li, "Characterization and Enhancement of 600V Cascode GaN Device," CPES PMC Review, March 11, 2015

Body diode reverse-recovery

- >100x lower Qrr for GaN cascode



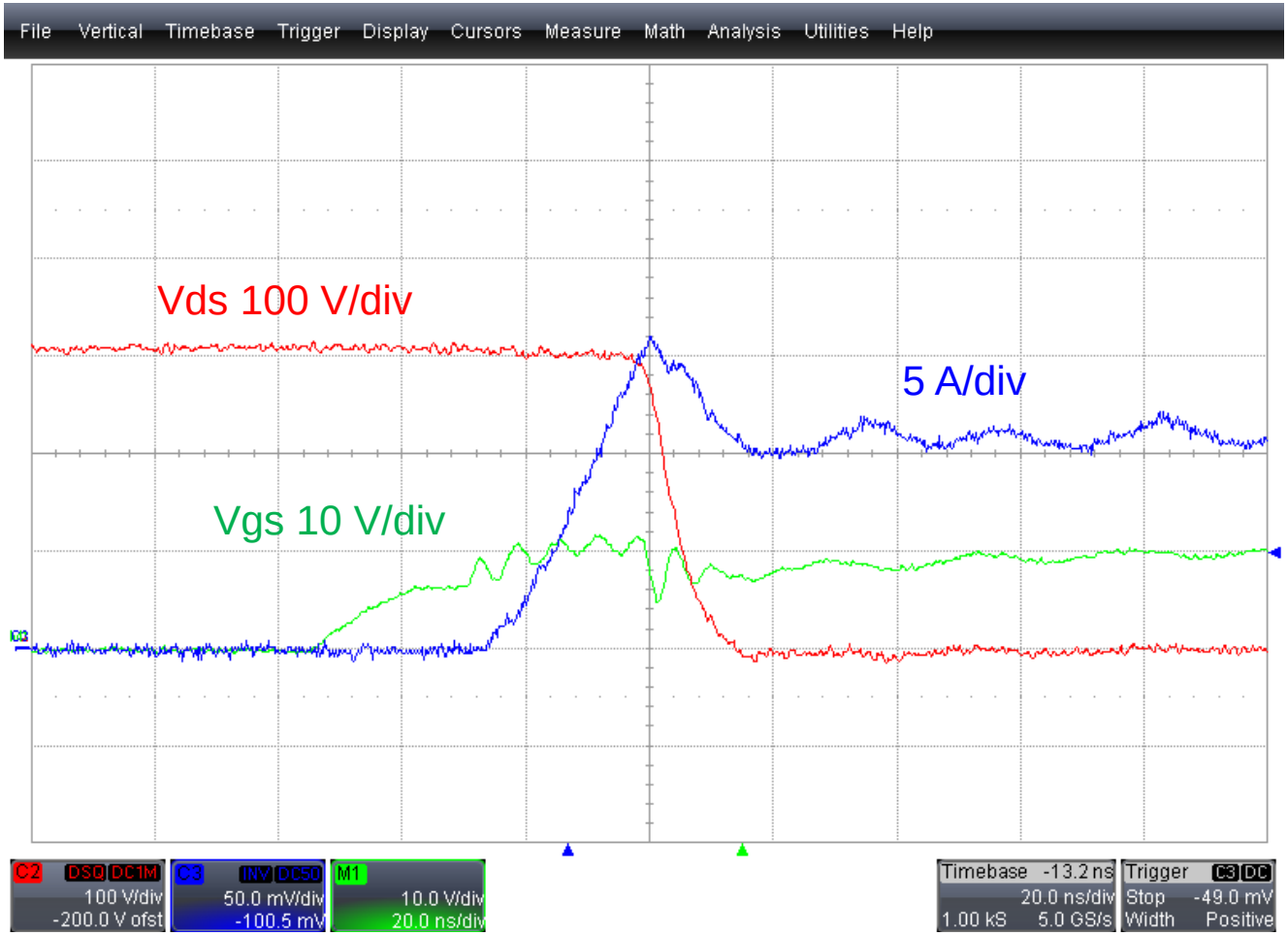
Comparing GaN cascode to superjunction

- 1st Generation GaN cascode

Parameter	GaN cascode	Equivalent SJ	
Package	6x8 mm PQFN	8x8 mm PQFN	GaN 25% smaller package
Vdss	600 V	650 V	
Rdson typ 25°C	135 mΩ	115 mΩ	
Rdson typ 125°C	225 mΩ	230 mΩ	GaN 1.67x; SJ 2x
Qg (10V Vgs, 480V Vds)	8.8 nC	35 nC	GaN ~4X lower than SJ
Qrr (100A/µs, 25°C)	49 nC	6,400 nC	GaN >100X lower than SJ
Coss (400V)	47 pF	53 - 579 pF	Energy vs time equivalent
Rθ J-C (°C/W)	1.65	1.22	Consistent with package

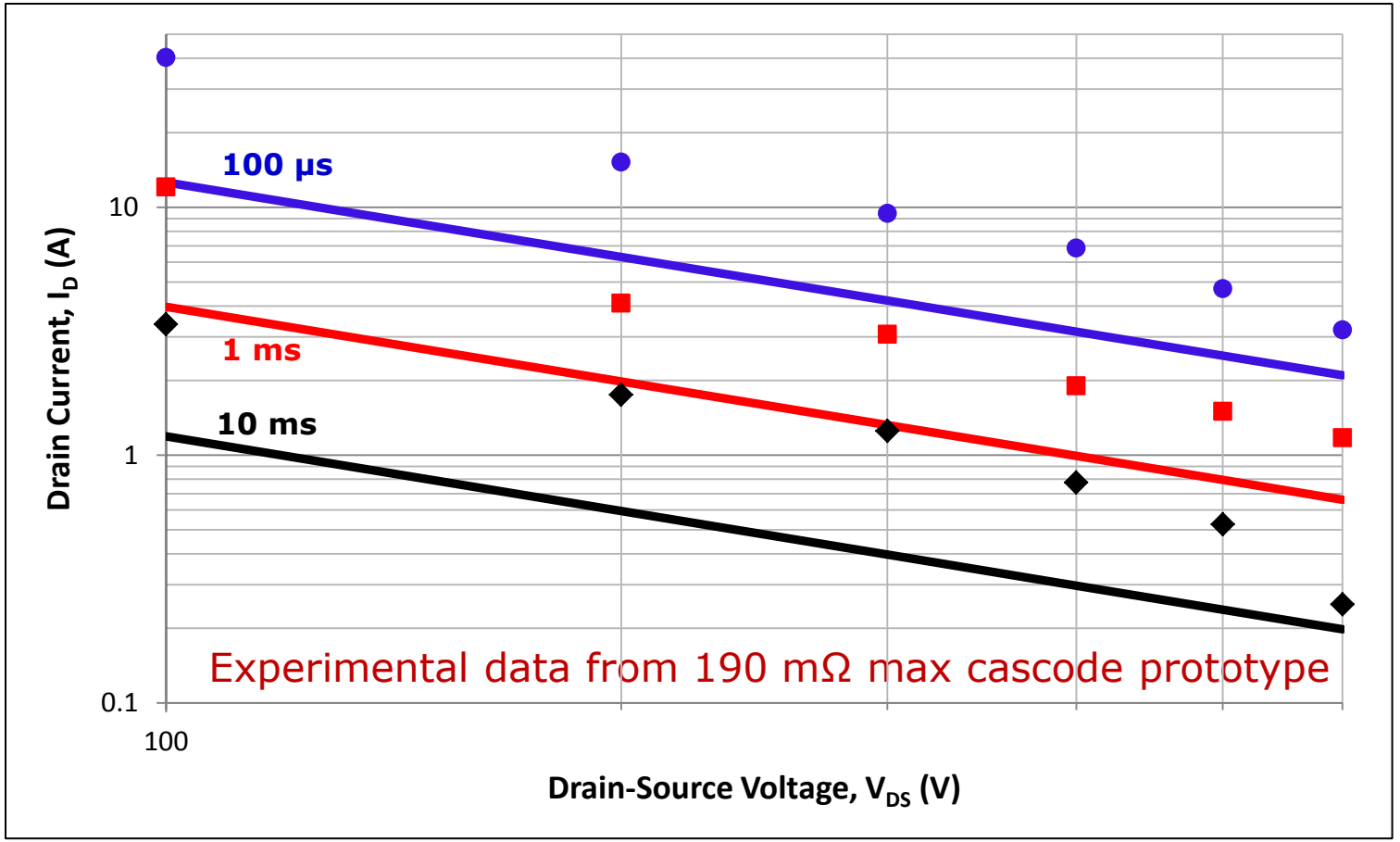
Turn-on waveform, 135 mΩ (typ) cascode

- Hard-switching Rg = 2Ω. ~9 µJ E_{ON}



GaN HEMT Safe Operating Area

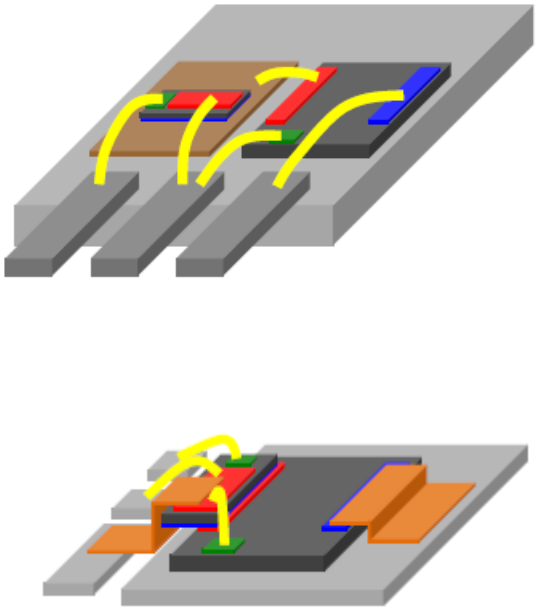
- Measured destruct current >2x higher than calculated thermal limit

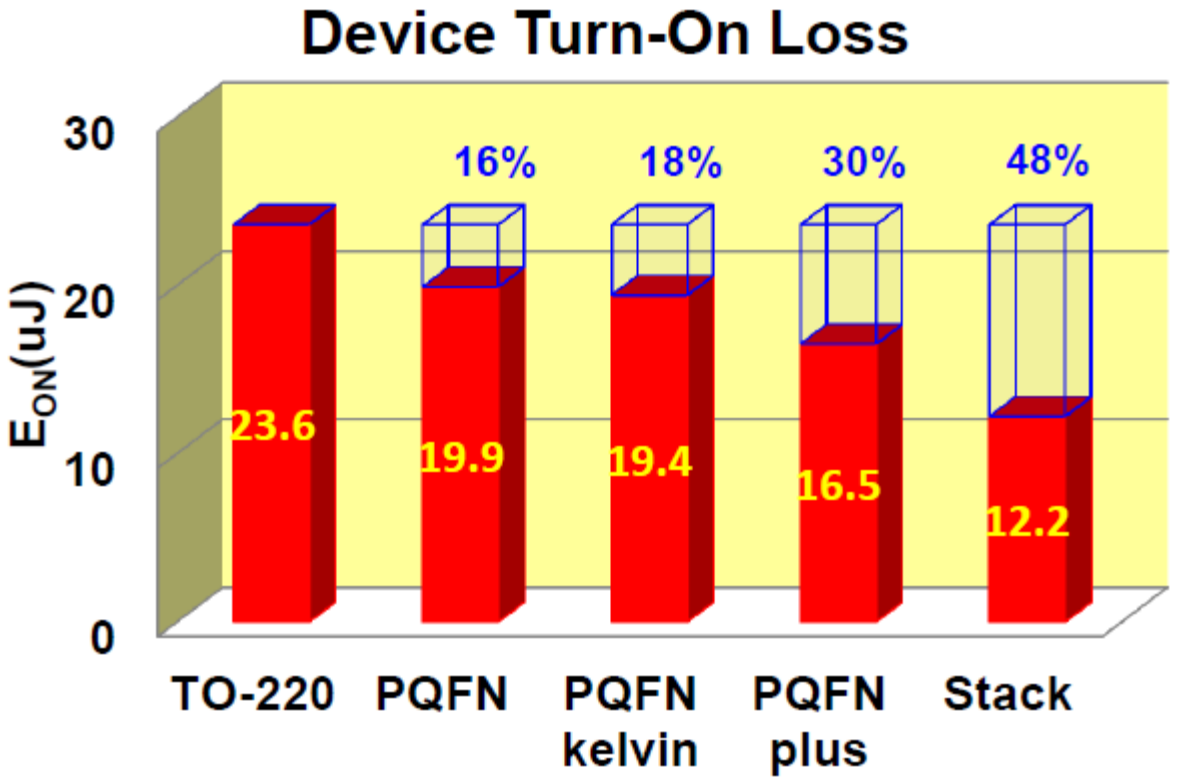


- Lines represent calculated thermal limit – points are measured failures

GaN performance interdependent on package

- Two key factors for minimizing losses:
  - Minimize GaN – Si interconnect inductance
  - Eliminate common-source inductance with Kelvin connection

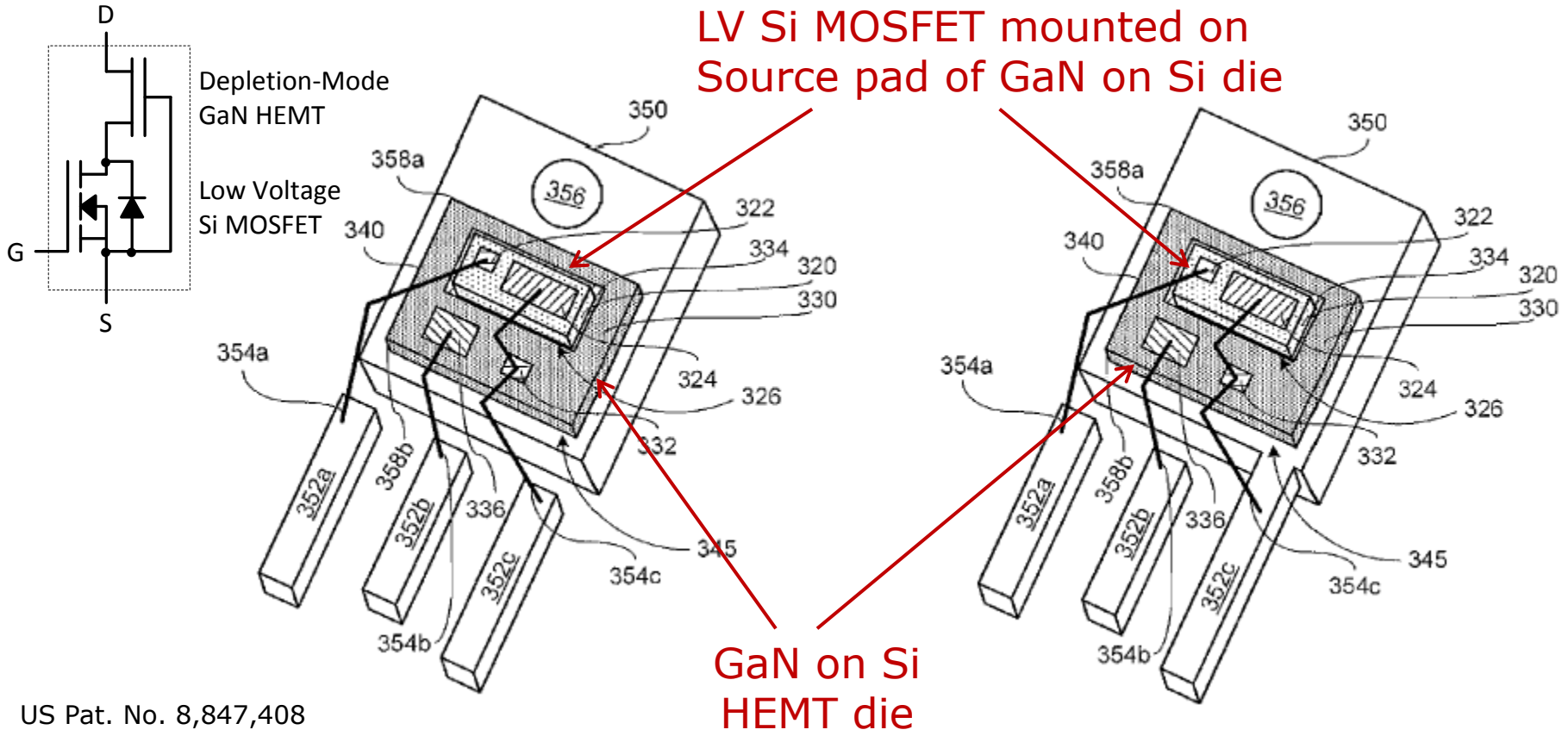




REF: Z. Liu, X. Huang, FC Lee, Q. Li, "Investigation of Package Influence on High Voltage Cascode GaN HEMT with Simulation Model," CPES review 2-13-2013, Milpitas, CA

Die-on-die cascode construction

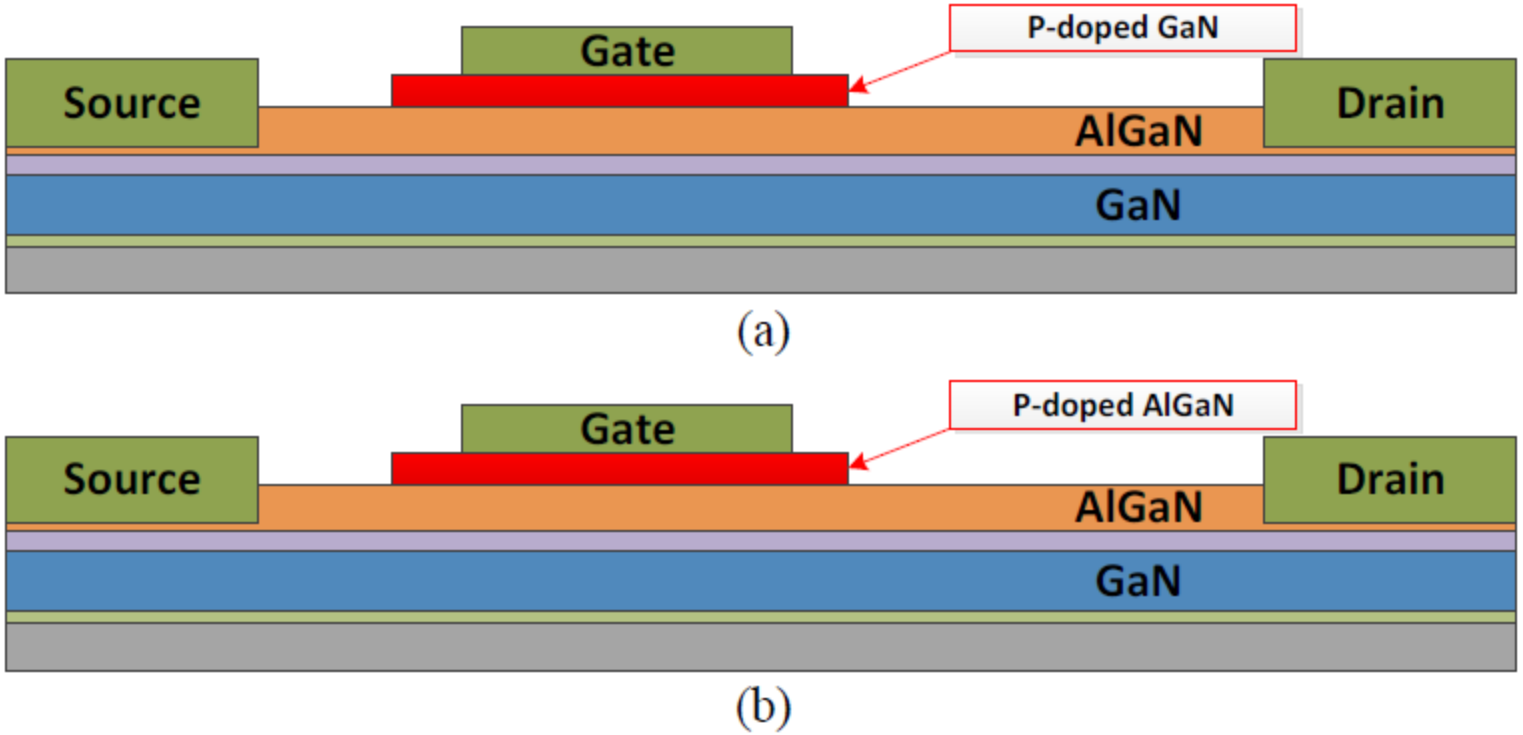
- Minimizes parasitic impedance between HEMT and FET
  - Faster switching transitions, less ringing and overshoot



US Pat. No. 8,847,408

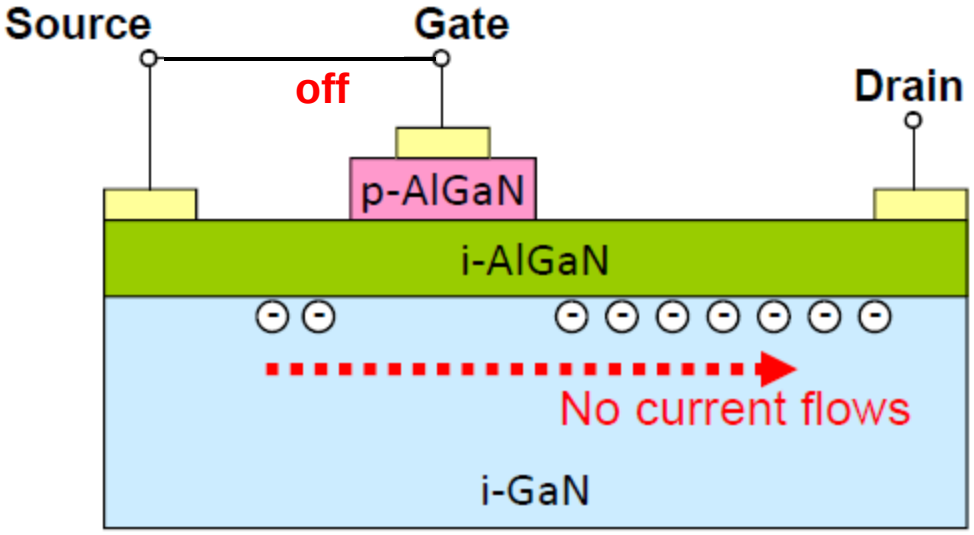
E-mode GaN HEMT Structures

a) P-gate enhancement-mode
b) P-gate enhancement-mode (gate injection)



Ref: Jones, E.A.; Wang, F.; Ozpineci, B., "Application-based review of GaN HFETs," Wide Bandgap Power Devices and Applications (WiPDA) 2014, pp.24-29, 13-15 Oct. 2014

Enhancement-Mode HEMT (Gate Injection)

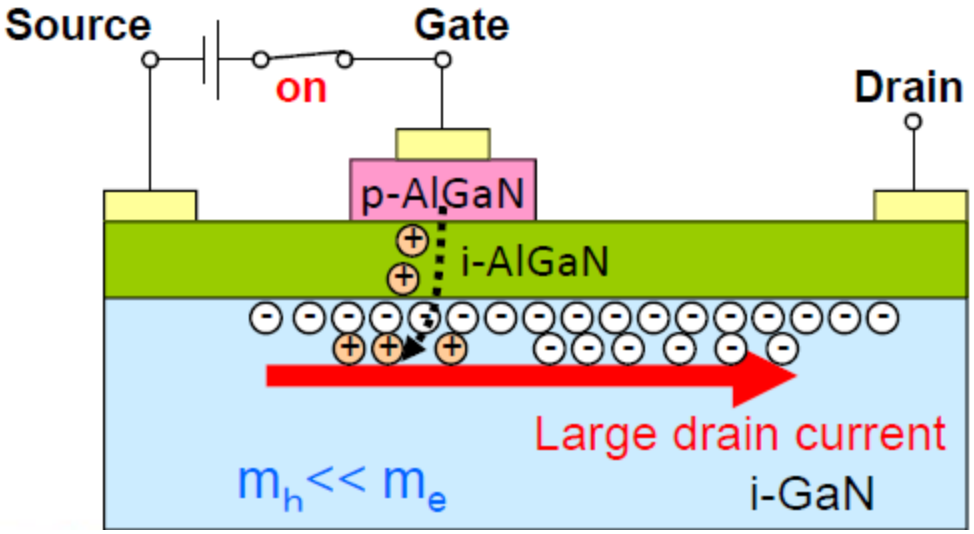


Vg = 0V

p-gate potential depletes the channel under the gate

↓

No drain current



Vg > Vf of GaN-PN junction

Hole injection

↓

Electron generation

↓

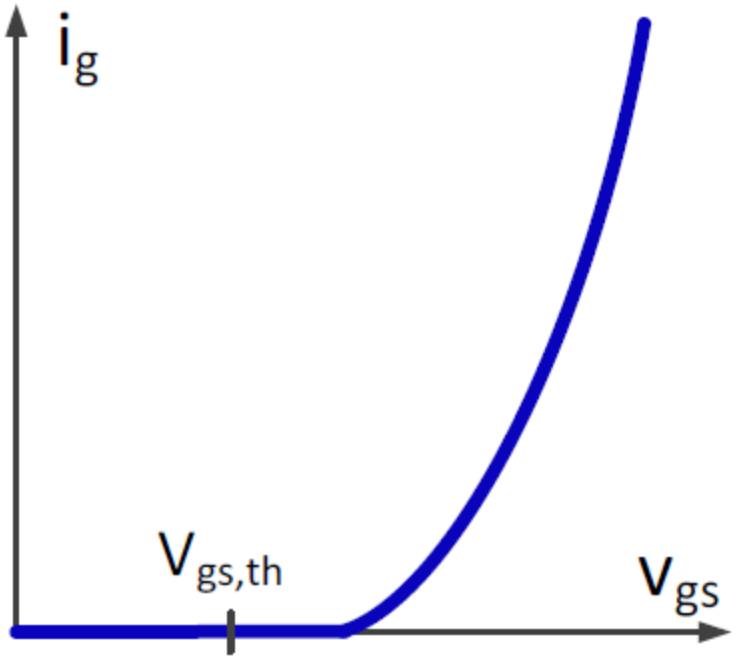
Large drain current

(conductivity modulation)

Ref: http://www.semicon.panasonic.co.jp/en/news/contents/2013/apec/panel/APEC2013_GaN_FPD_WEB.pdf

Gate Characteristics (Enhancement Mode)

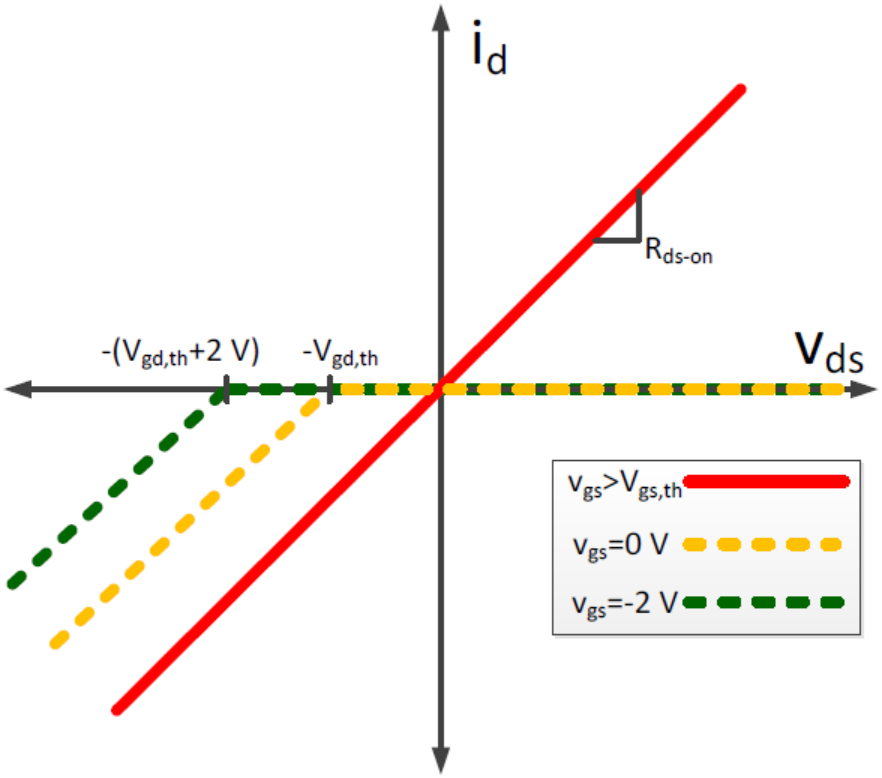
- Typical non-insulated gate characteristic
  - Gate injection uses small DC current (e.g. 10 mA)



Ref: Jones, E.A.; Wang, F.; Ozpineci, B., "Application-based review of GaN HFETs," Wide Bandgap Power Devices and Applications (WiPDA) 2014, pp.24-29, 13-15 Oct. 2014

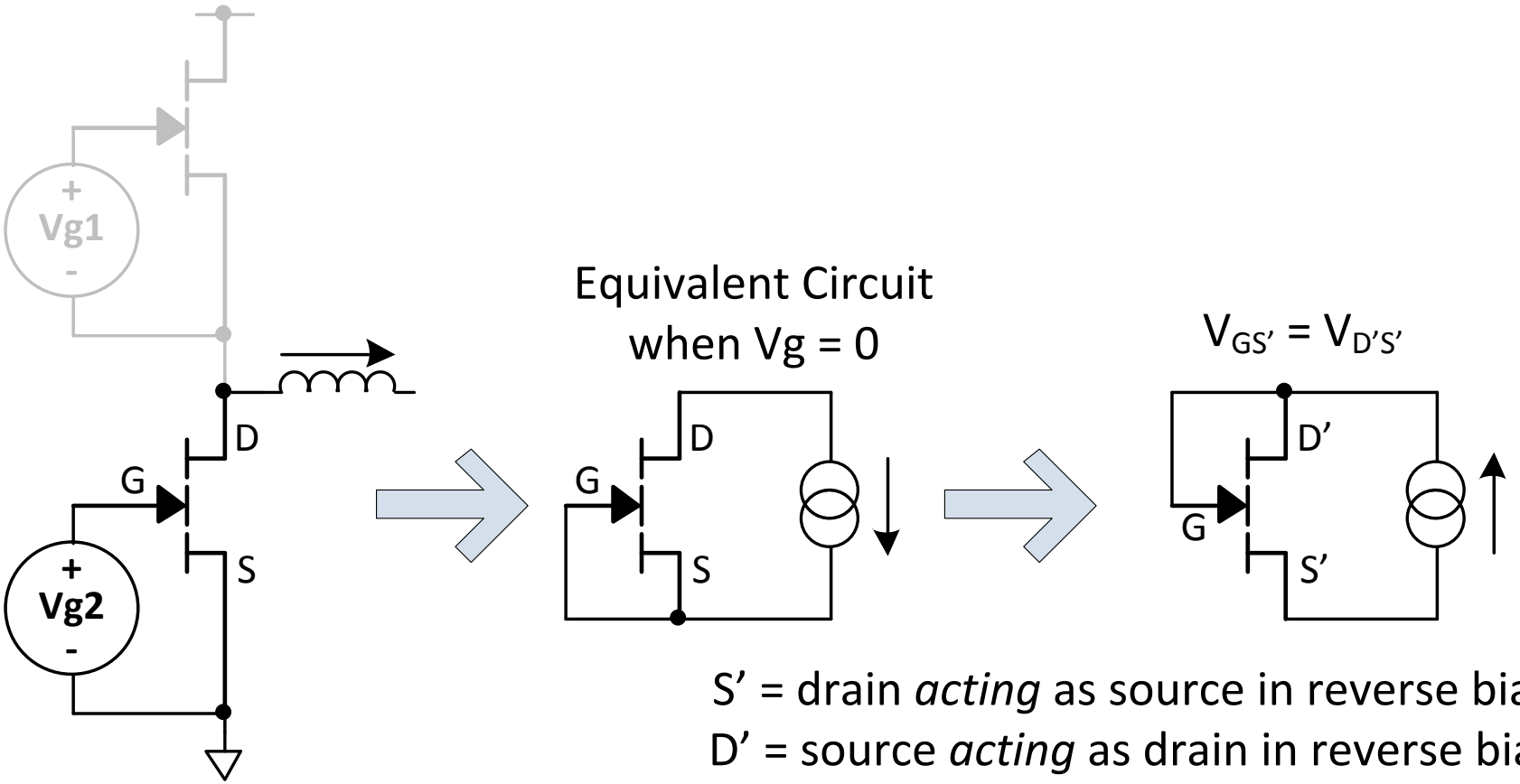
Output Characteristics (Enhancement Mode)

- HEMT turns back ON when drain goes below G, S



Ref: Jones, E.A.; Wang, F.; Ozpineci, B., "Application-based review of GaN HFETs," Wide Bandgap Power Devices and Applications (WiPDA) 2014, pp.24-29, 13-15 Oct. 2014

Reverse Bias Diode-Like Behavior

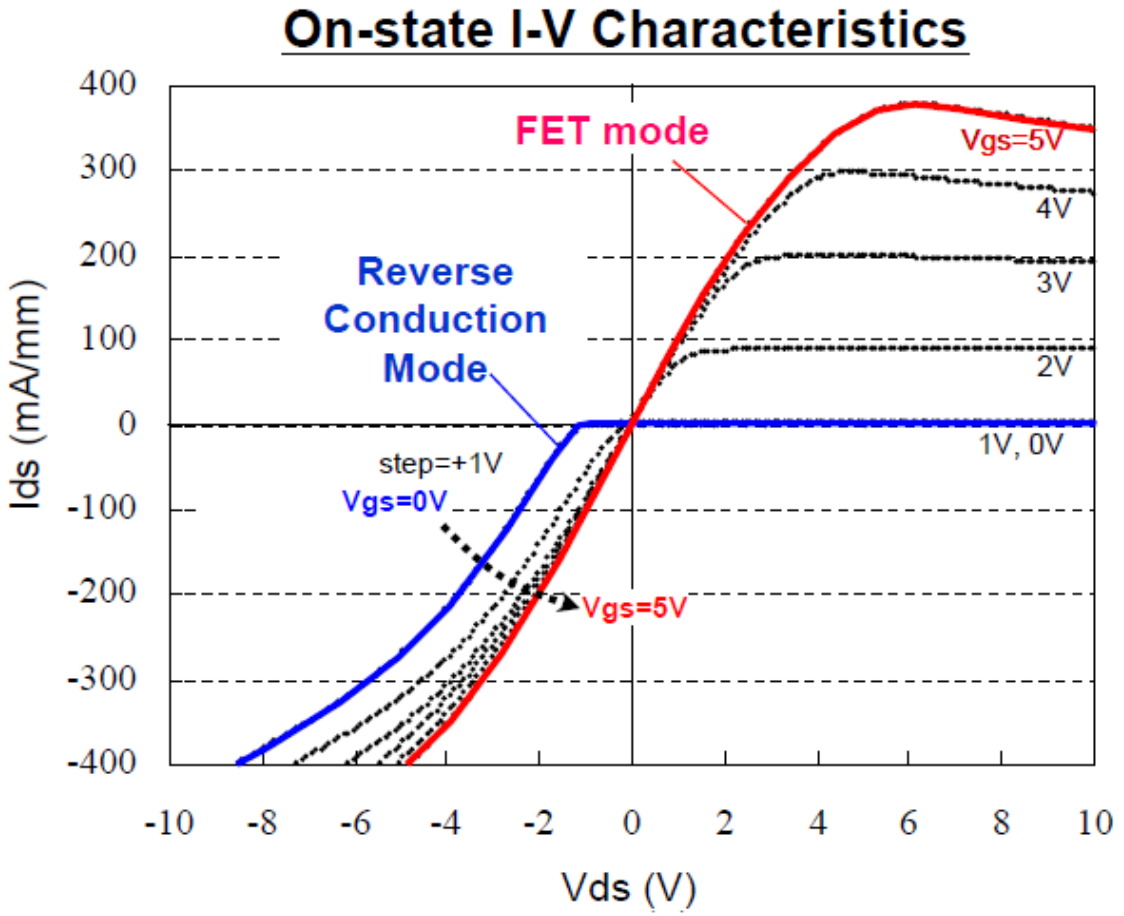


S' = drain *acting* as source in reverse bias

D' = source *acting* as drain in reverse bias

Forward and Reverse I-V Characteristics

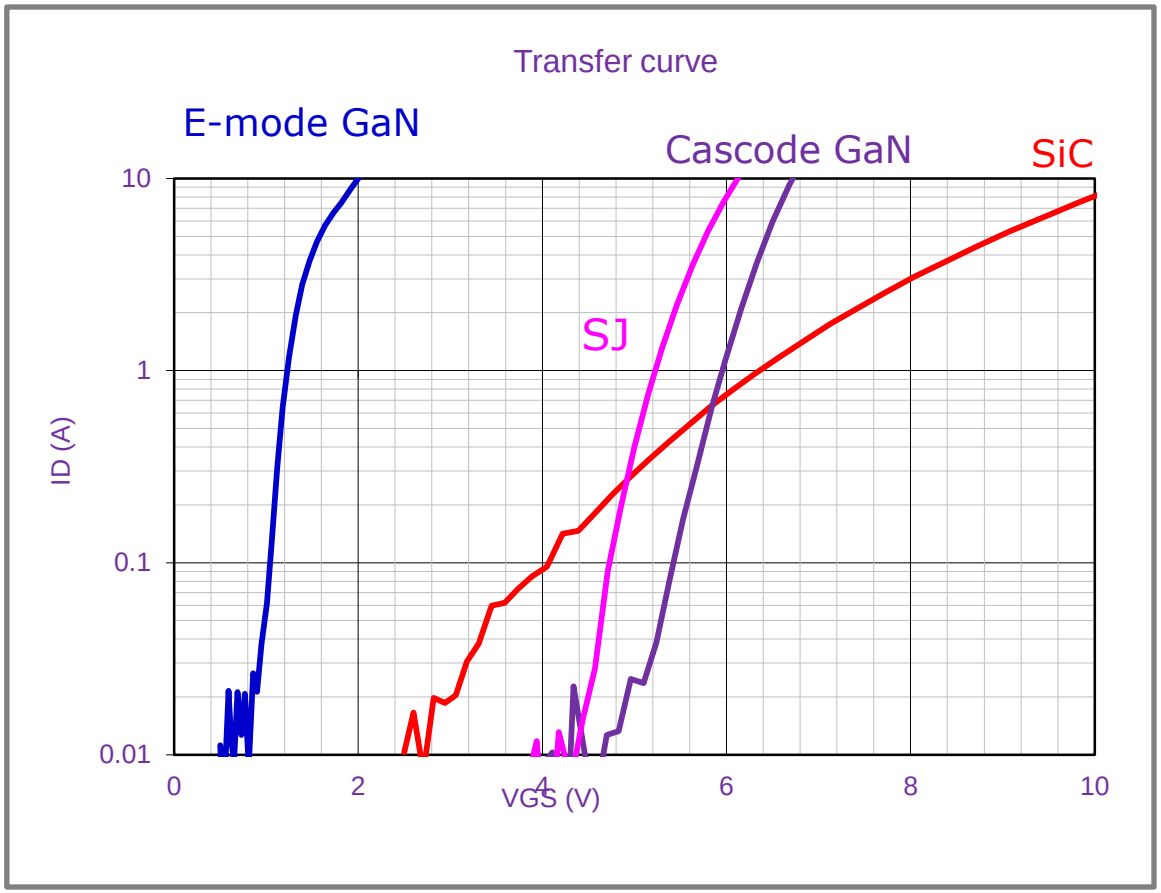
- HEMT eventually saturates at very high current



Ref: http://www.semicon.panasonic.co.jp/en/news/contents/2013/apec/panel/APEC2013_GaN_FPD_WEB.pdf

GaN, superjunction, (& SiC) transfer curves

- Cascode superjunction and SiC ~135 mΩ typical
- E-mode GaN (non GIT) ~50mΩ (135 mΩ @ 150°C)



Comparing GaN vs SJ Qoss

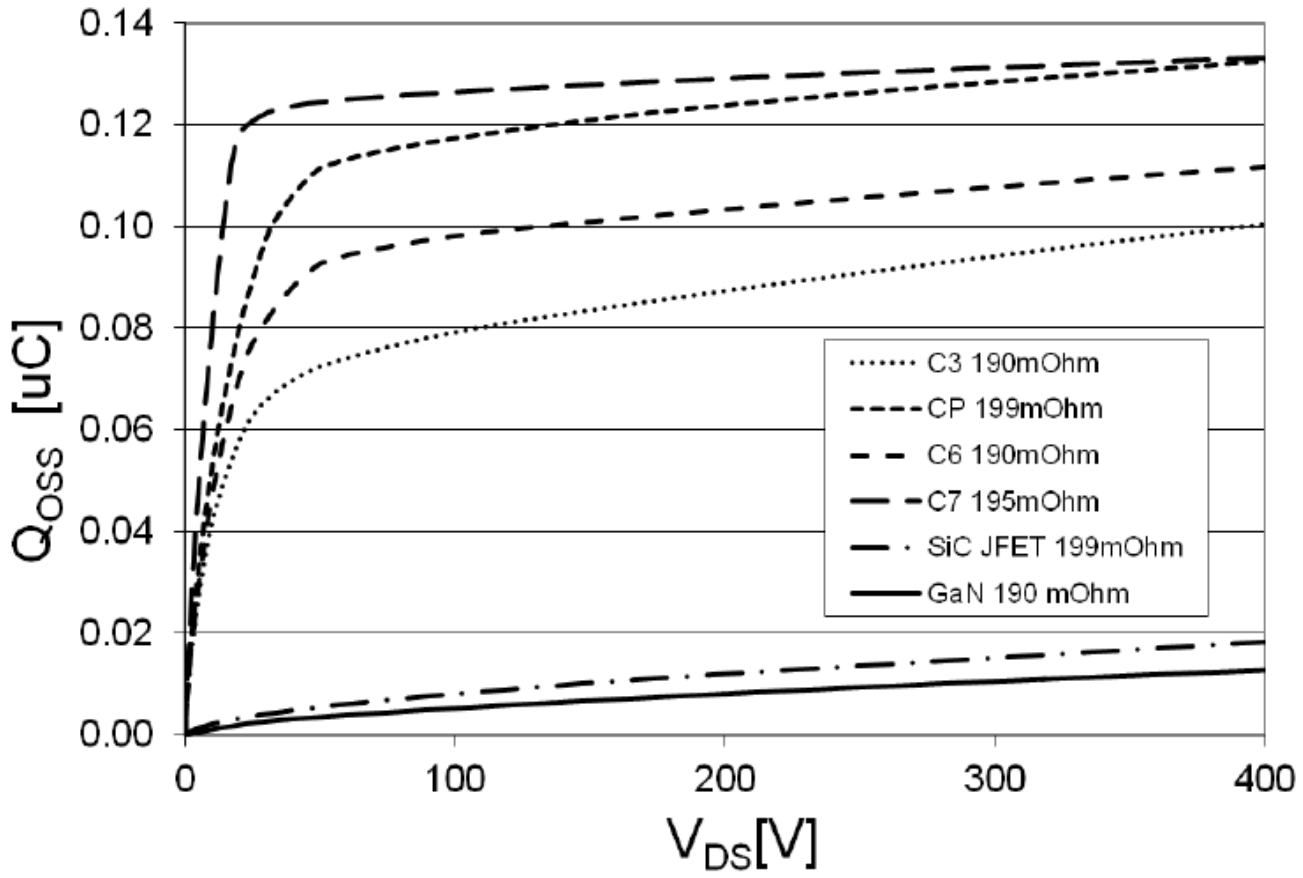
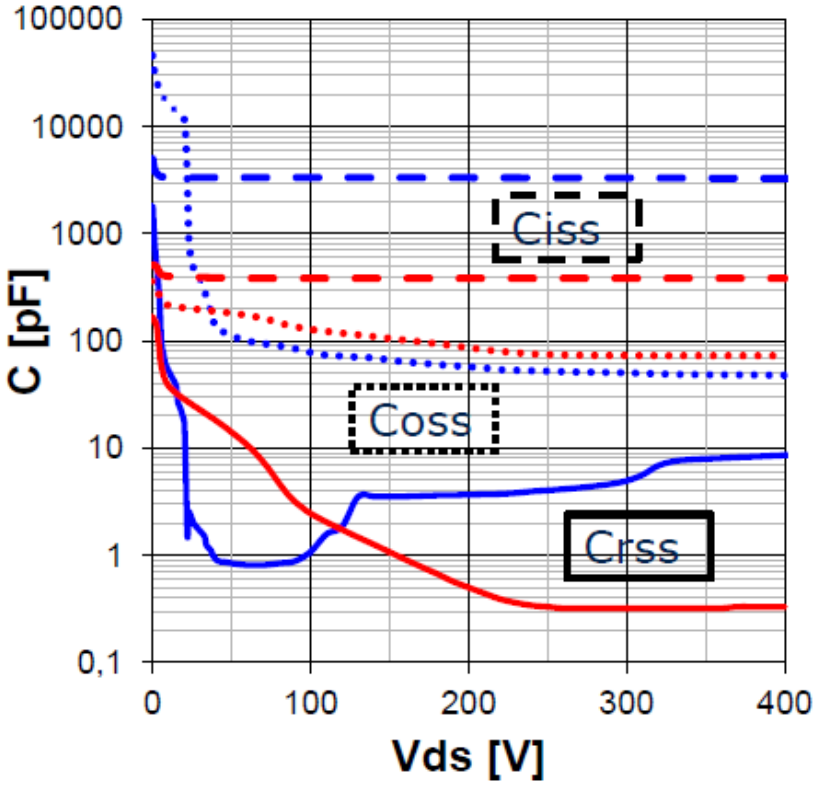


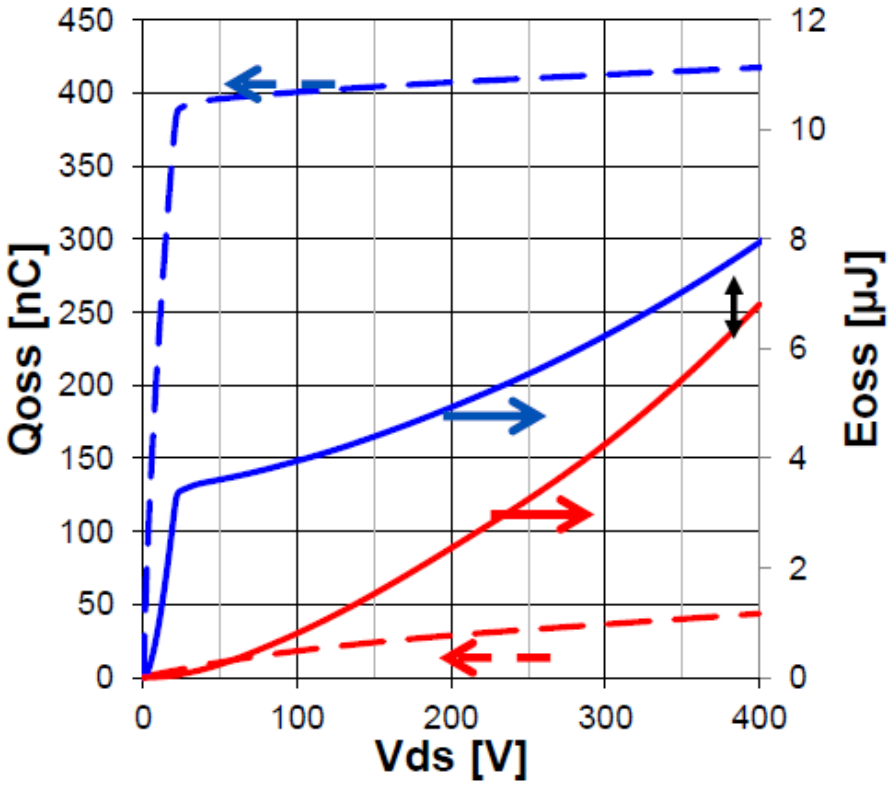
Fig. 5, Comparison of the charge stored in the output capacitance Q_{OSS} for different CoolMOS devices and potential SiC and GaN devices.

REF: M. Treu, E. Vecino, M. Pippan, O. Häberlen, G. Curatola, G. Deboy, M. Kutschak, U. Kirchner," The role of silicon, silicon carbide and gallium nitride in power electronics," IEEE International Electron Devices Meeting, December, 2012

Comparing Coss, Qoss, Eoss GaN vs SJ

Blue = superjunction
Red = e-mode HEMT
Both ~70 mΩ max Rds(on)

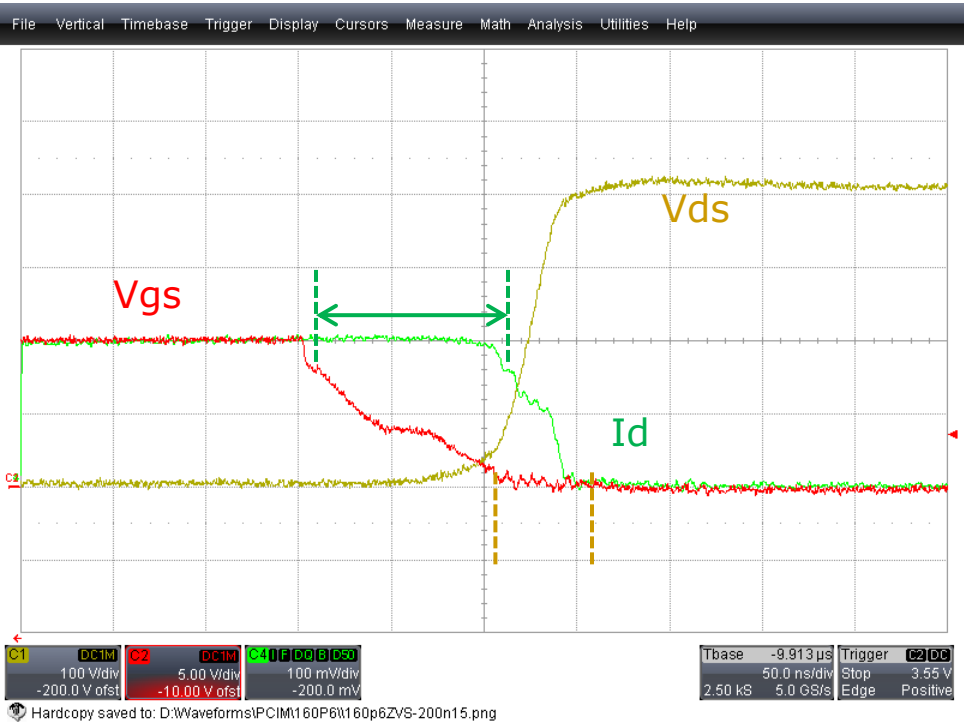




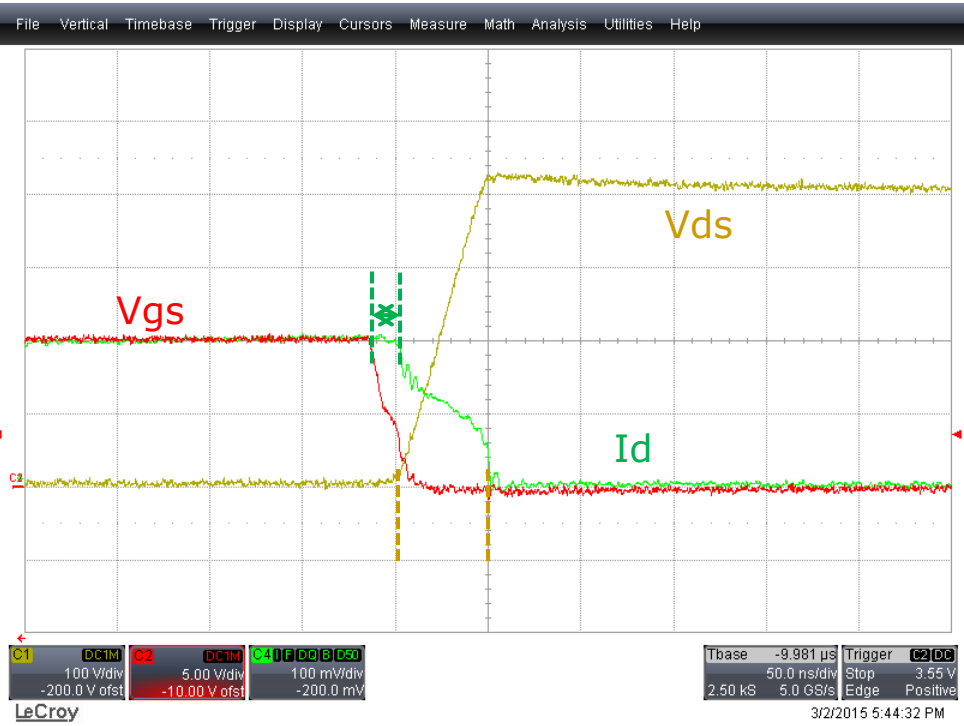
Comparing GaN vs superjunction turn-off

- LLC topology looking at low-side switch
  - 400 V bus, 2 A
  - Same Rds(on)

Superjunction



Cascode GaN



Avalanche and overvoltage

- Superjunction has junction with avalanche capability
  - Useful in circuits with unclamped inductive energy (flyback)
- GaN has no junction, no avalanche behavior
  - GaN ultimately breaks down destructively at ~2x rating
  - Overvoltage spikes are allowed depending on supplier
- GaN is best suited for half-bridge topology
  - Fast body diode helps to mitigate overvoltage spikes
  - Overvoltage spikes are clamped to bus
  - With proper design, no risk of breakdown

GaN Device Summary

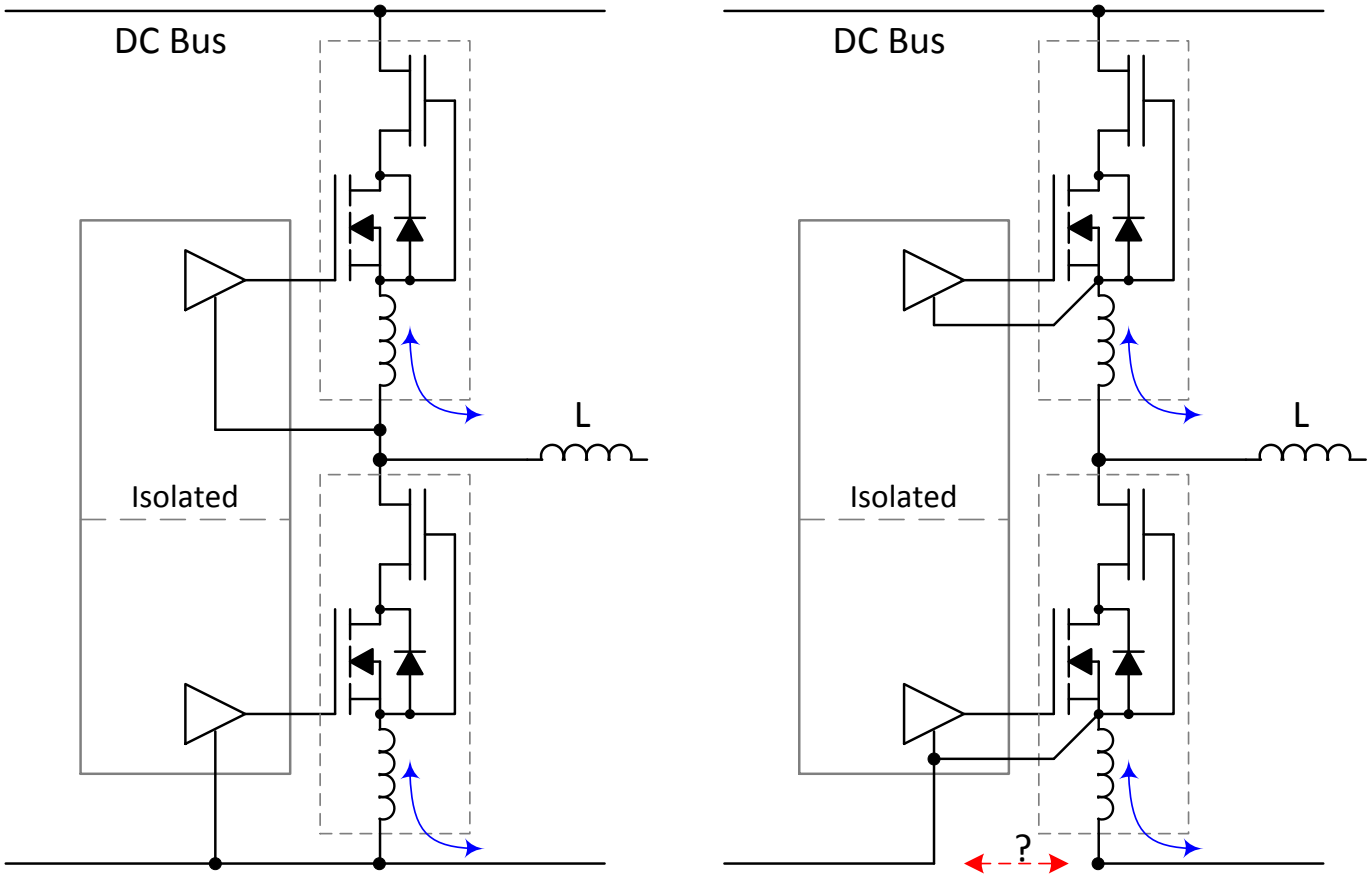
- Both cascode and enhancement mode – compared to superjunction:
- Provides MUCH lower Qrr (zero for e-mode)
  - Enables use of efficient half-bridge topologies
- Provide smaller, more linear Qoss
  - Reduces deadtime in resonant and ZVS circuits
- Provide lower gate charge Qg
  - Lower gate drive power and faster switching speed
- Eoss not much difference
- Does not have avalanche behavior
  - Does have overvoltage capability

Applications of GaN

Gate Drive

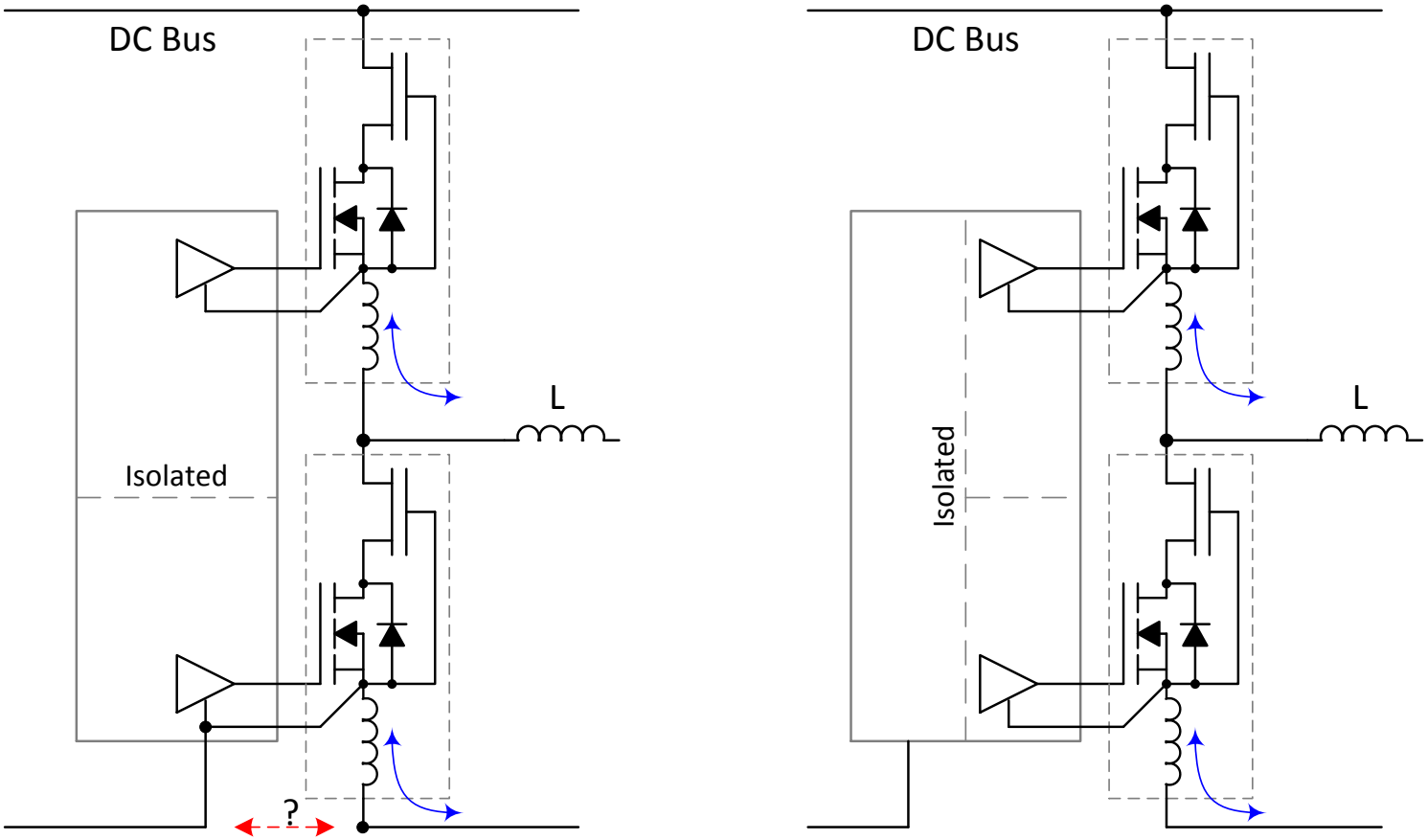
- Cascode – standard Si gate drivers work
  - Vgs(th) is potential issue
  - Common Source Inductance is a concern as always
  - C dv/dt induced gate currents
  - Kelvin gate-source connections
  - Advantages of floating gate drive

Gate drive challenges for low threshold devices



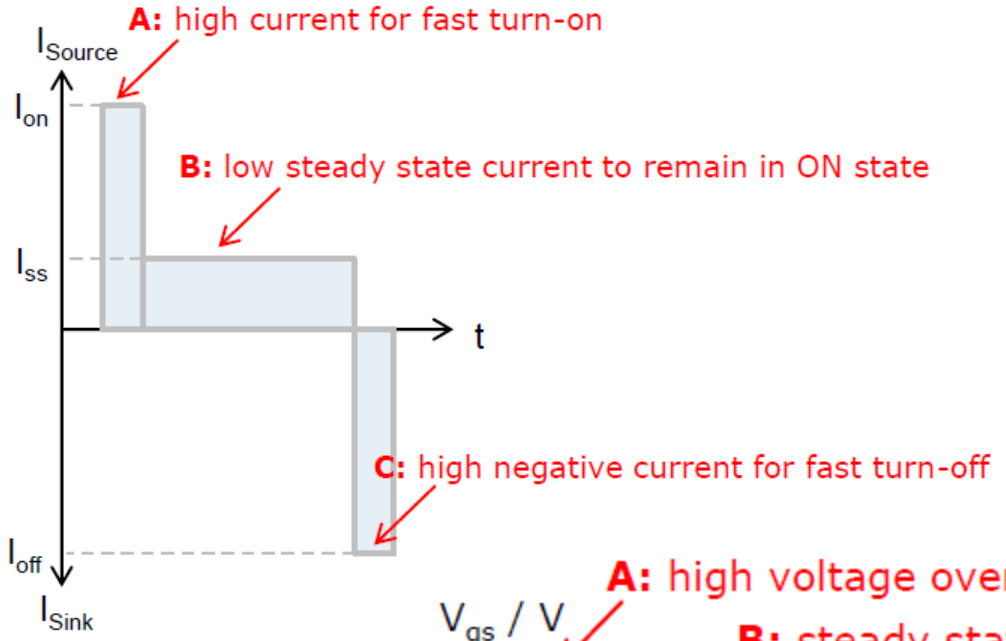
- Common Source Inductance distorts Vgs
- Kelvin source connection eliminates CSI
- …BUT can cause system grounding problems for driver

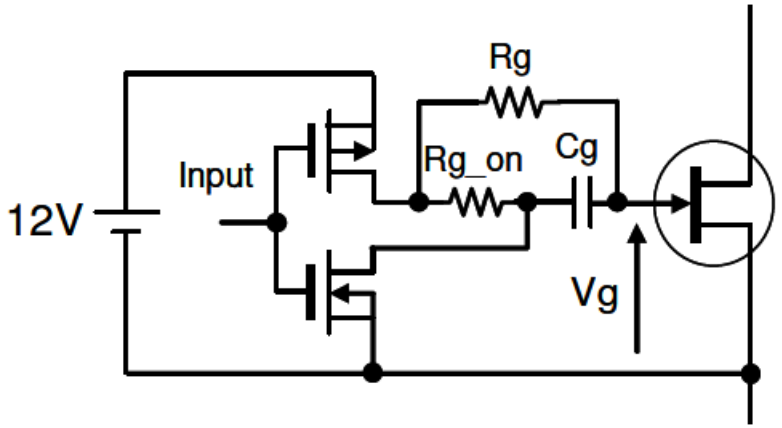
Isolated gate drive + Kelvin source connection



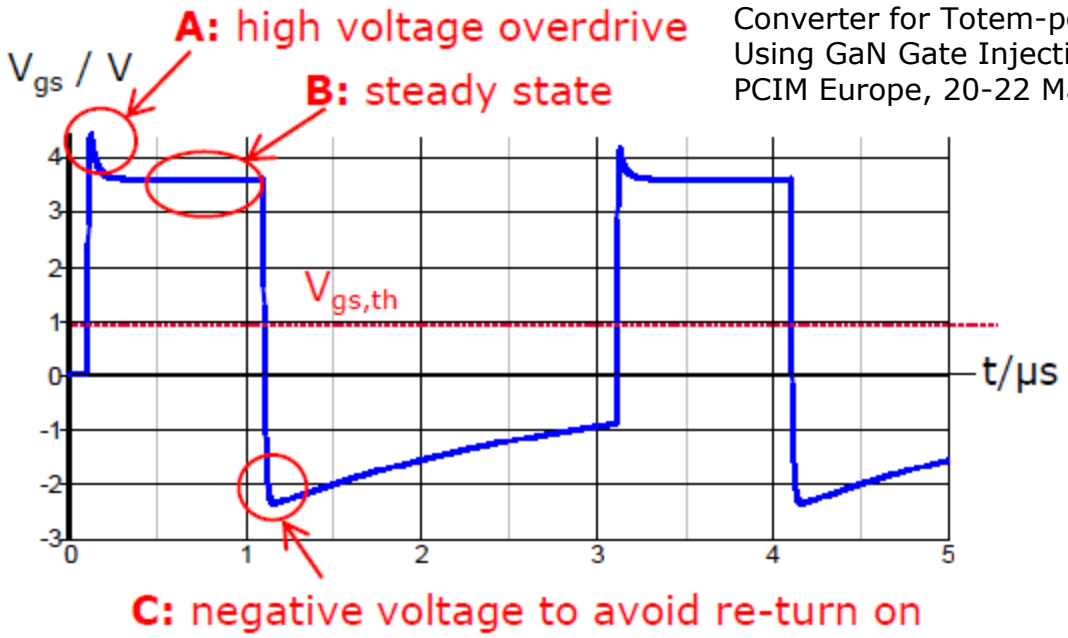
- Isolating both high and low-side drivers solves system ground bounce issues which can affect current sense and logic ground

Gate drive for gate injection





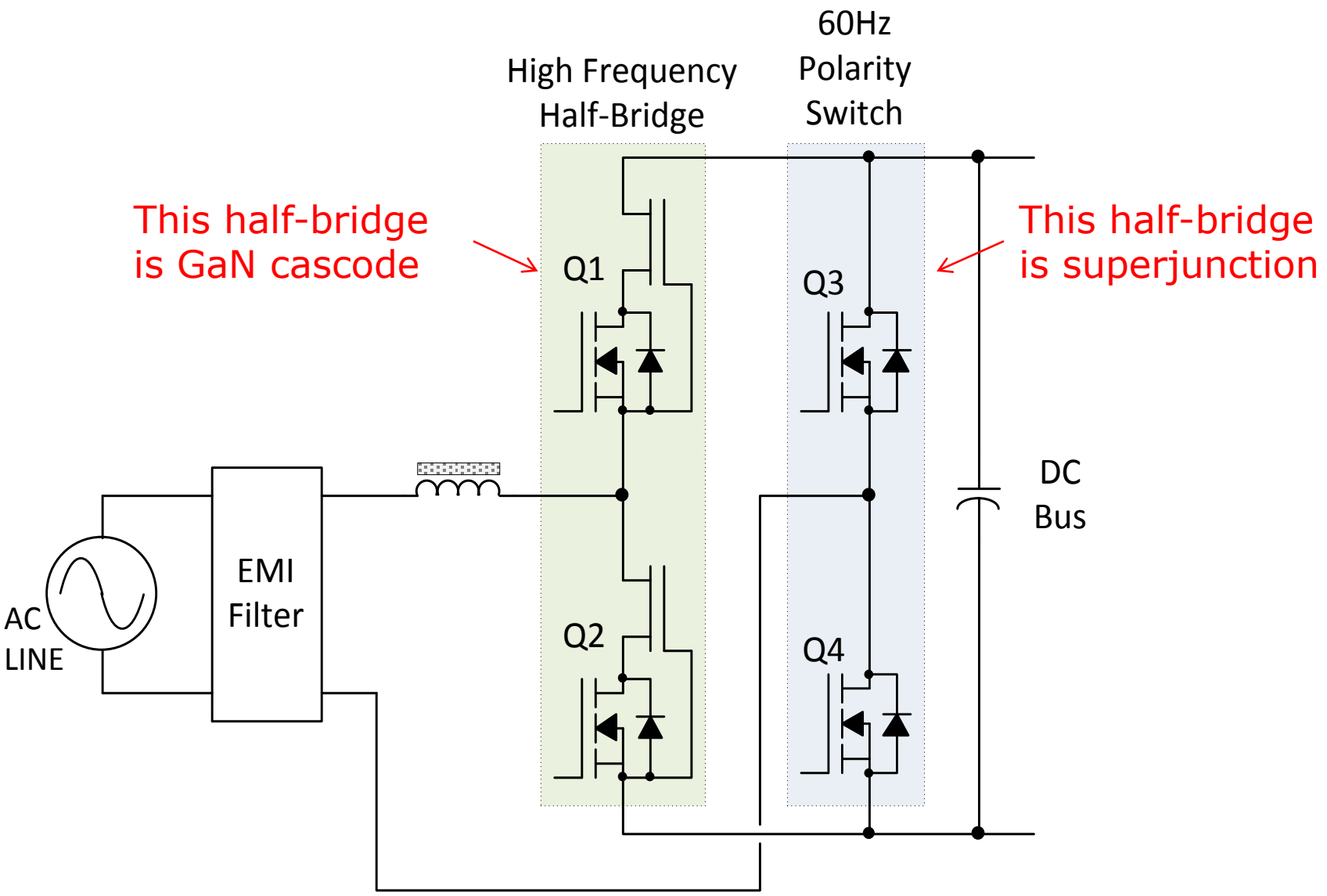
REF: T. Morita, H. Hanada, S Ujita, M Ishida, T. Ueda, "99.3% Efficiency Boost-up Converter for Totem-pole Bridgeless PFC Using GaN Gate Injection Transistors," Proc. PCIM Europe, 20-22 May 2014



Gate drive summary

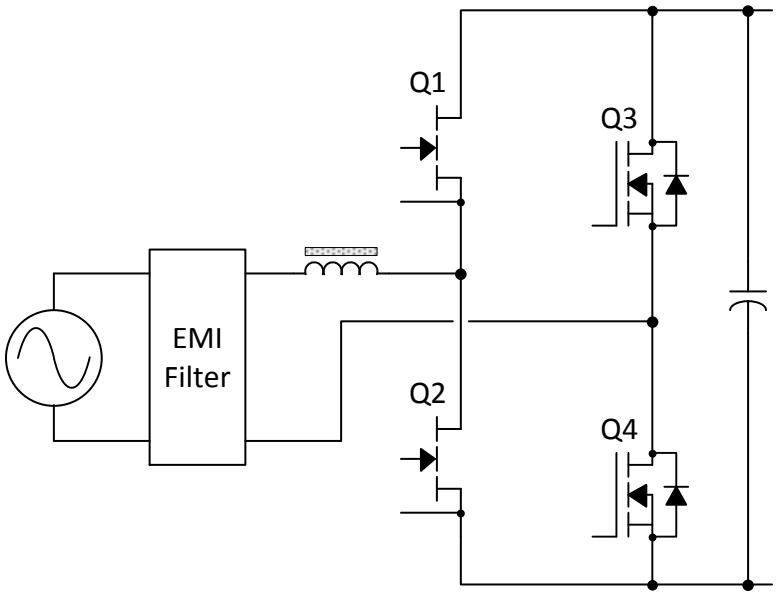
- Cascode GaN:
  - Standard FET gate driver compatibility
  - Lower Qg for given current-handling capability
  - ZVS turn-off easier to achieve
- Enhancement-mode GaN
  - Low threshold, noise sensitivity, negative drive can help
  - Tighter limits on Vgs
  - *Very* low Qg
  - Kelvin source connection mandatory
  - Floating driver helpful especially at higher power

Totem-Pole PFC Full-Bridge

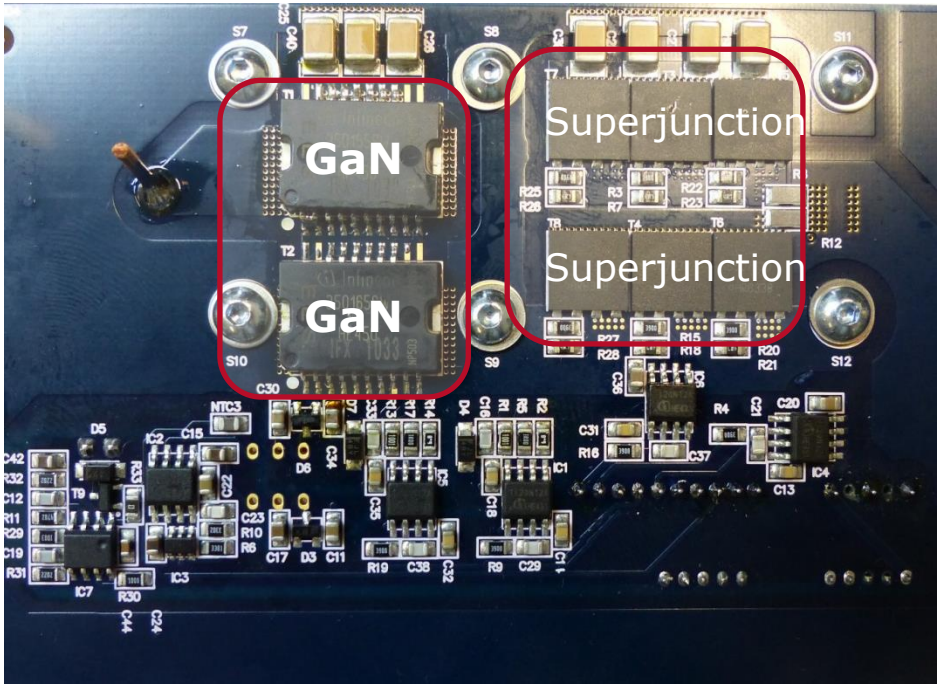


Totem-Pole PFC Full-Bridge

- 2.5 kW all SMD power stage proof-of-concept
- GaN boost stage 70 mΩ max enhancement-mode
- superjunction sync line rectifiers

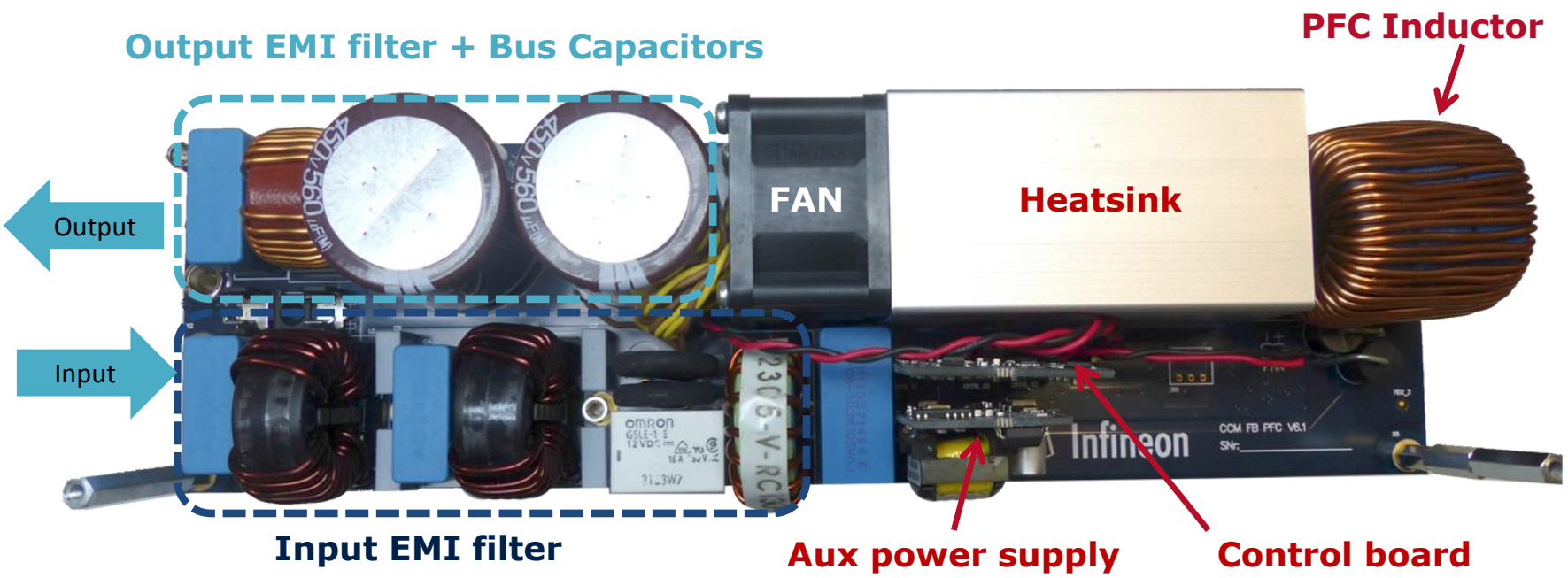


Bottom View of PCB



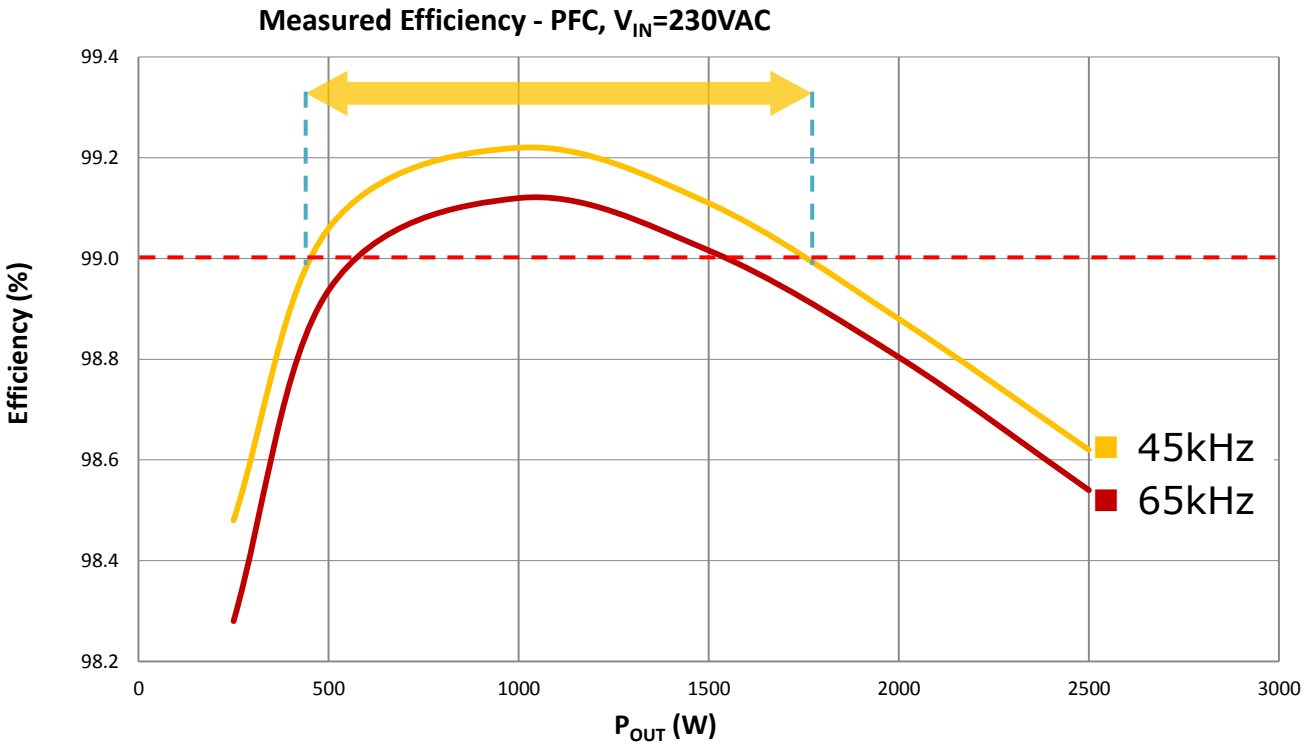
Totem-Pole PFC Full-Bridge

- Input 230 V_{AC}
- Output 400 V_{DC}, 6.25 A
- CCM 45 to 65 kHz



Totem-Pole PFC full-bridge performance

- >99% efficiency from 18-70% load



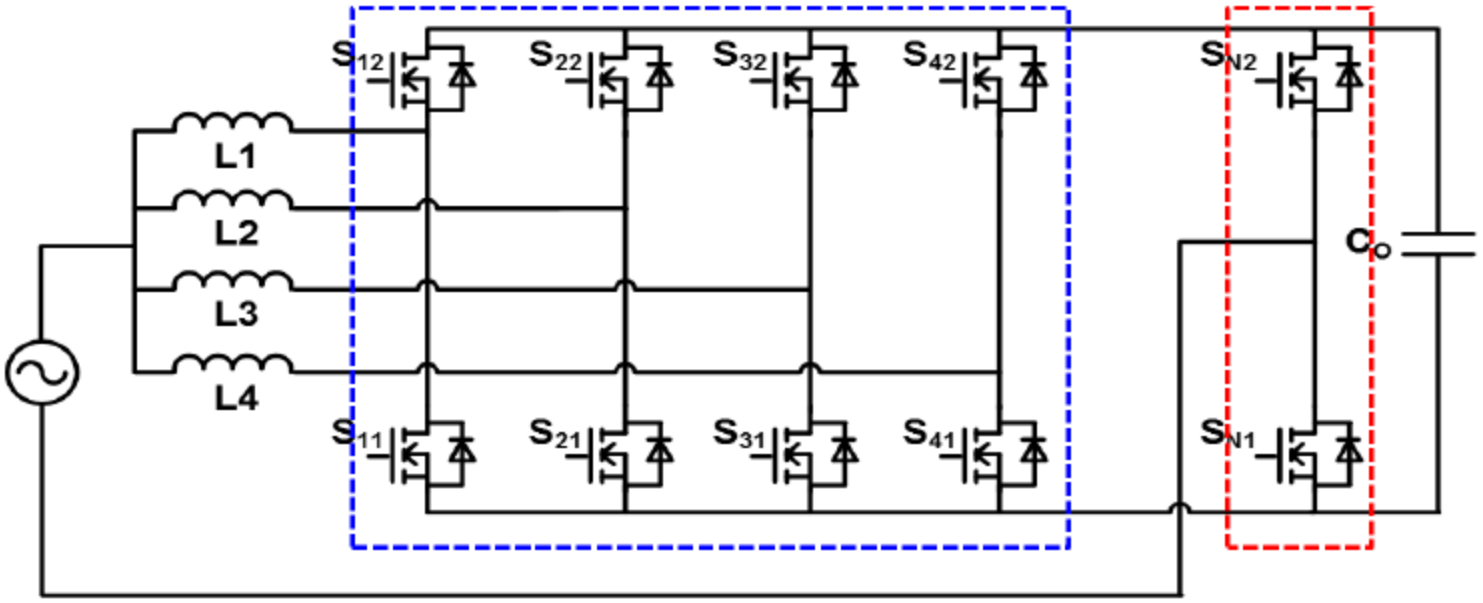
Complete Power Stage. V_{in}=230 V, T_{amb}=25° C

Totem Pole PFC

- No diode drops – only switch conduction voltage
- Very high efficiency possible >99%
- Lower component count than other bridgeless topologies
- Topology is enabled by GaN HEMT
  - Traditional Si FETs have too much body-diode Qrr
    Large recovery currents and high losses
- Topology is Intrinsically bi-directional power flow
  - Can also be used in inverter/UPS applications

Totem Pole PFC Future

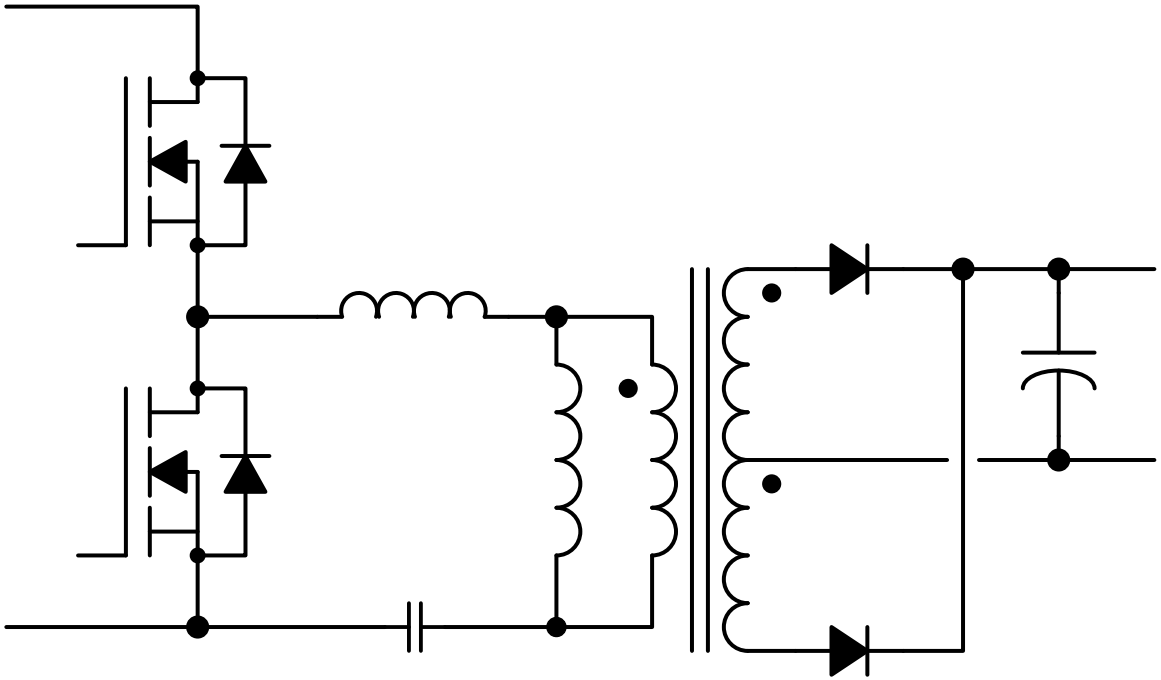
- MHz ZVS – still achieving 99% efficiency
- Multiphase architectures to minimize ripple
- Digital control to optimize performance & efficiency



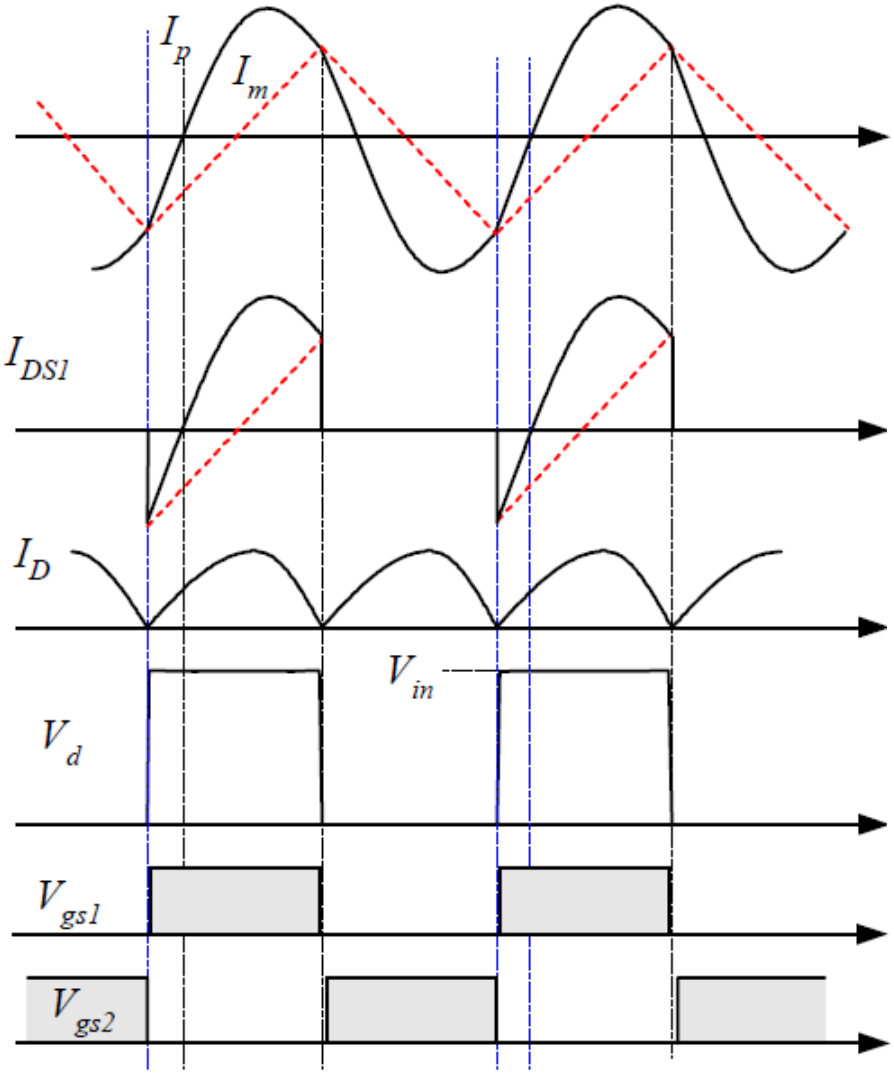
Ref: Zhengyang Liu, Fred C. Lee, QiangLi, "Digital Control for MHz Totem-pole PFC Rectifier," CPES PMC Review, Mar.11, 2015

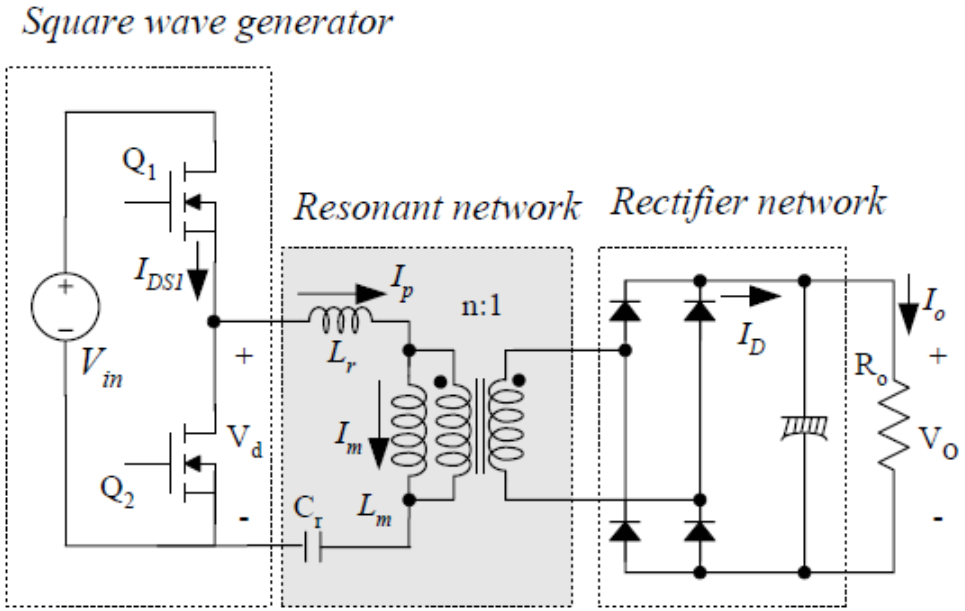
LLC Resonant DC-DC

- Popular topology today using superjunction
- Frequency range <200 kHz typically
- Caution required to prevent hard-switching



LLC typical waveforms and circuit

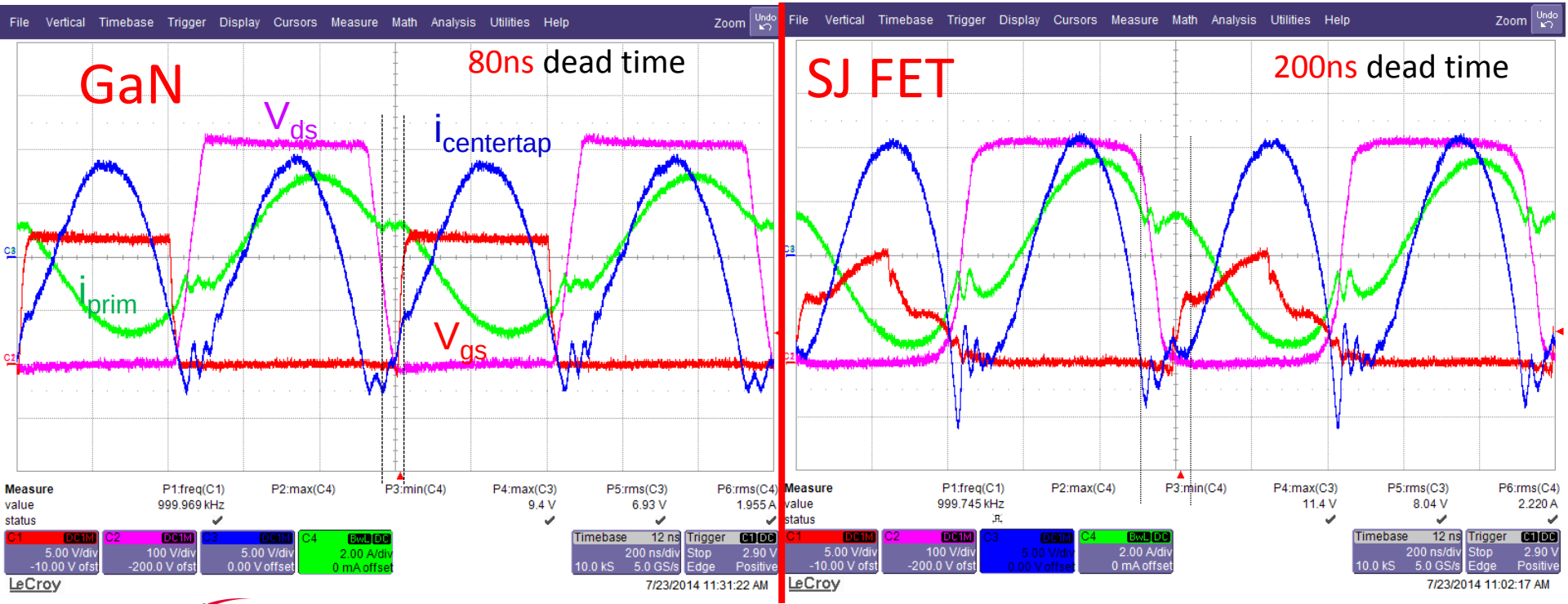




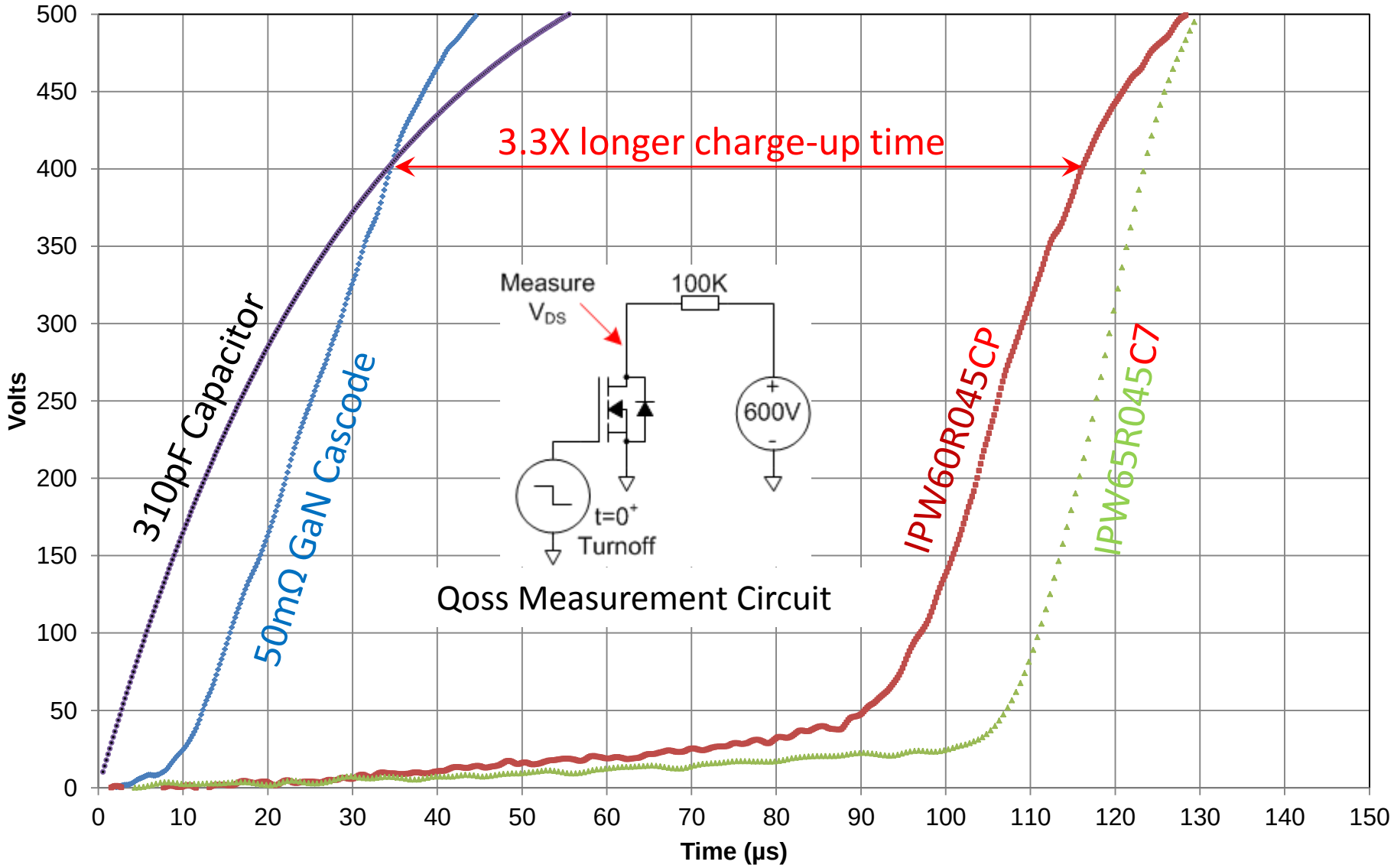
GaN enables shorter deadtime vs SJ @ 1MHz

- Shorter deadtime lowers rms current

	I^2 Primary	I^2 Secondary	Gate Drive
GaN	$3.84A^2$	$48.0A^2$	0.24W
Superjunction	$4.93A^2$	$64.6A^2$	1.88W
Difference	+28.3%	+34.6%	+685%



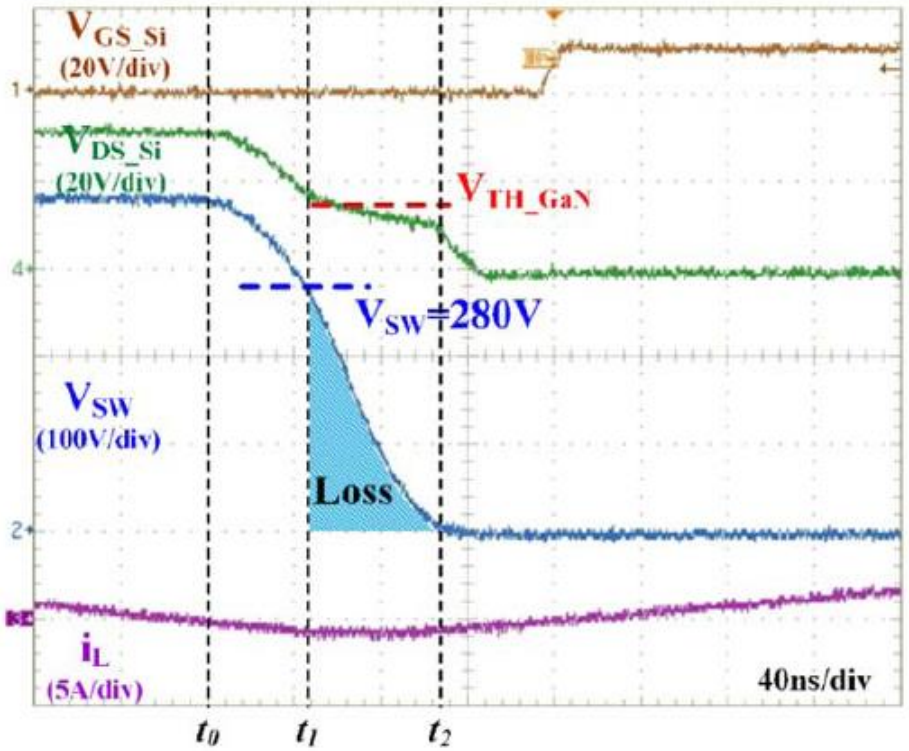
Nonlinear Qoss Charge Affects Deadtime



Cascode Charge Balance During ZVS Turn-ON

Improper charge balance results in loss of ZVS

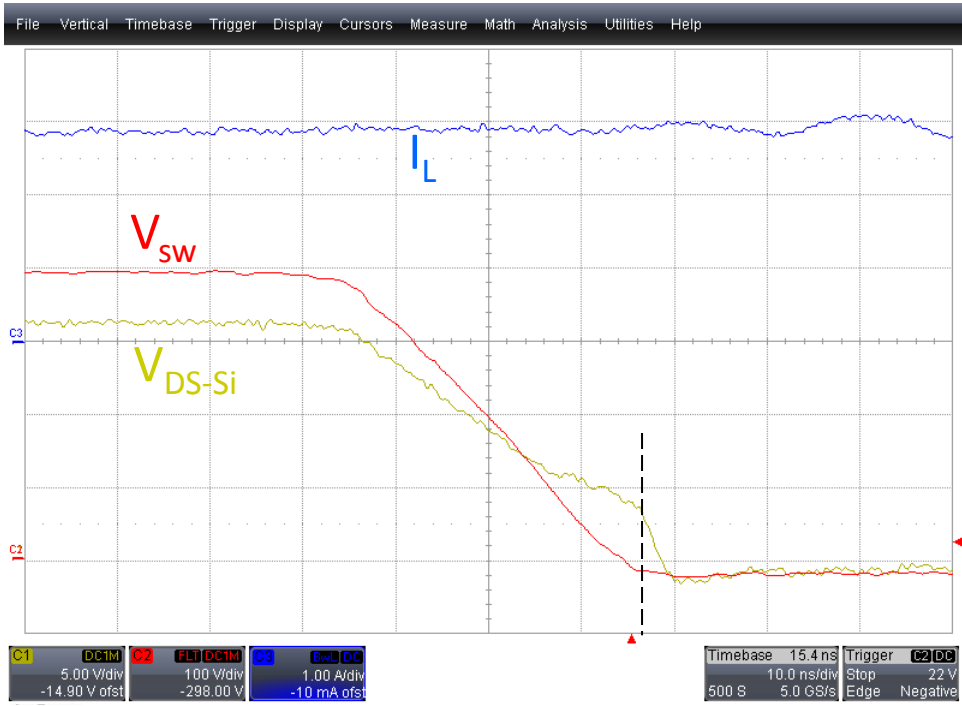
- Significant energy loss



X. Huang, W. Du, Z. Liu, F. C. Lee, and Q. Li, "Performance Analysis of Cascode GaN Device," CPES Review, Nov 18, 2013

Properly balanced Cascode achieves full ZVS

- No energy loss

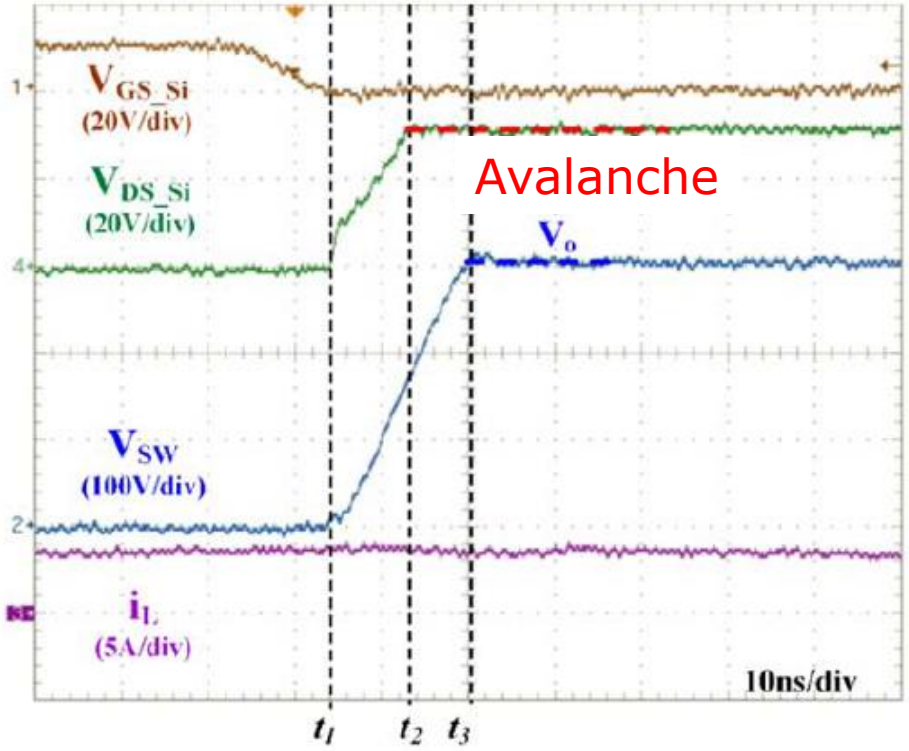


Measured Results: IR-Infineon Cascode

Cascode Charge Balance During ZVS Turn-OFF

Improper charge balance results in Si avalanche

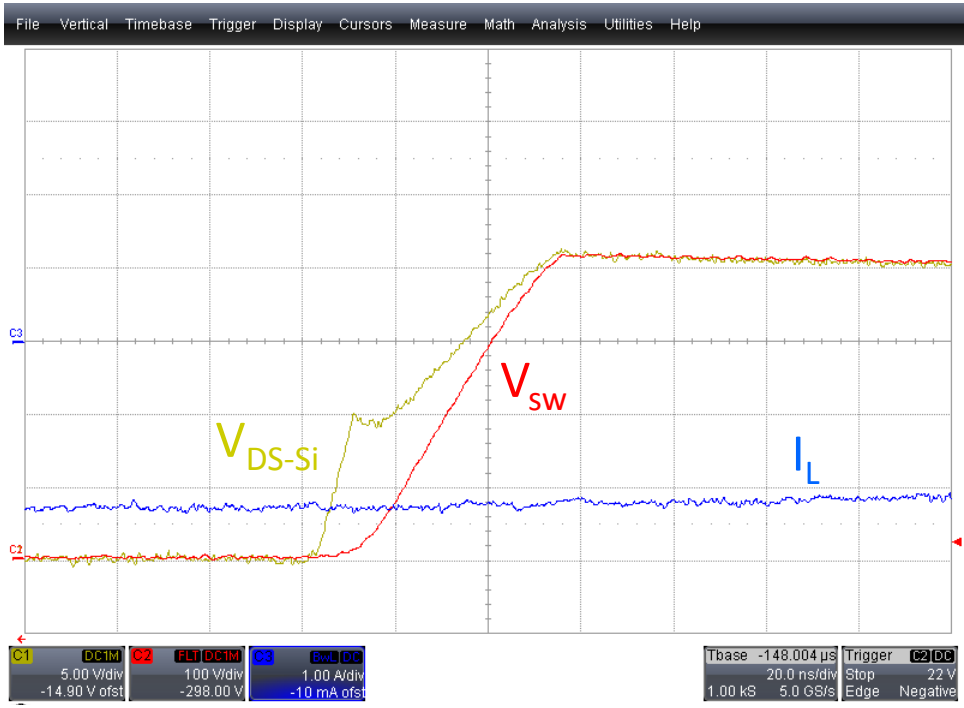
- Significant energy loss



X. Huang, W. Du, Z. Liu, F. C. Lee, and Q. Li, "Performance Analysis of Cascode GaN Device," CPES Review, Nov 18, 2013

Properly balanced Cascode no avalanche, full ZVS

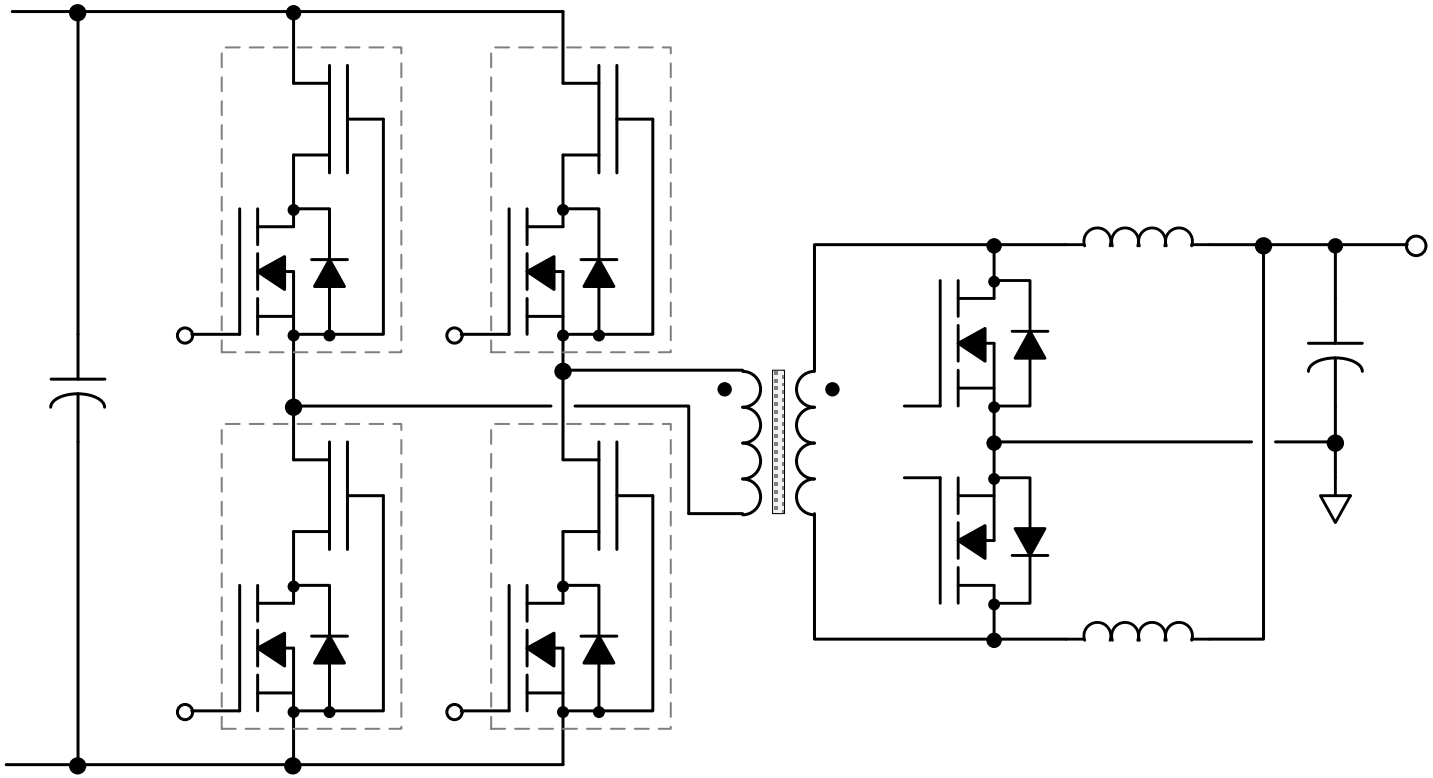
- No energy loss



Measured Results: IR-Infineon Cascode

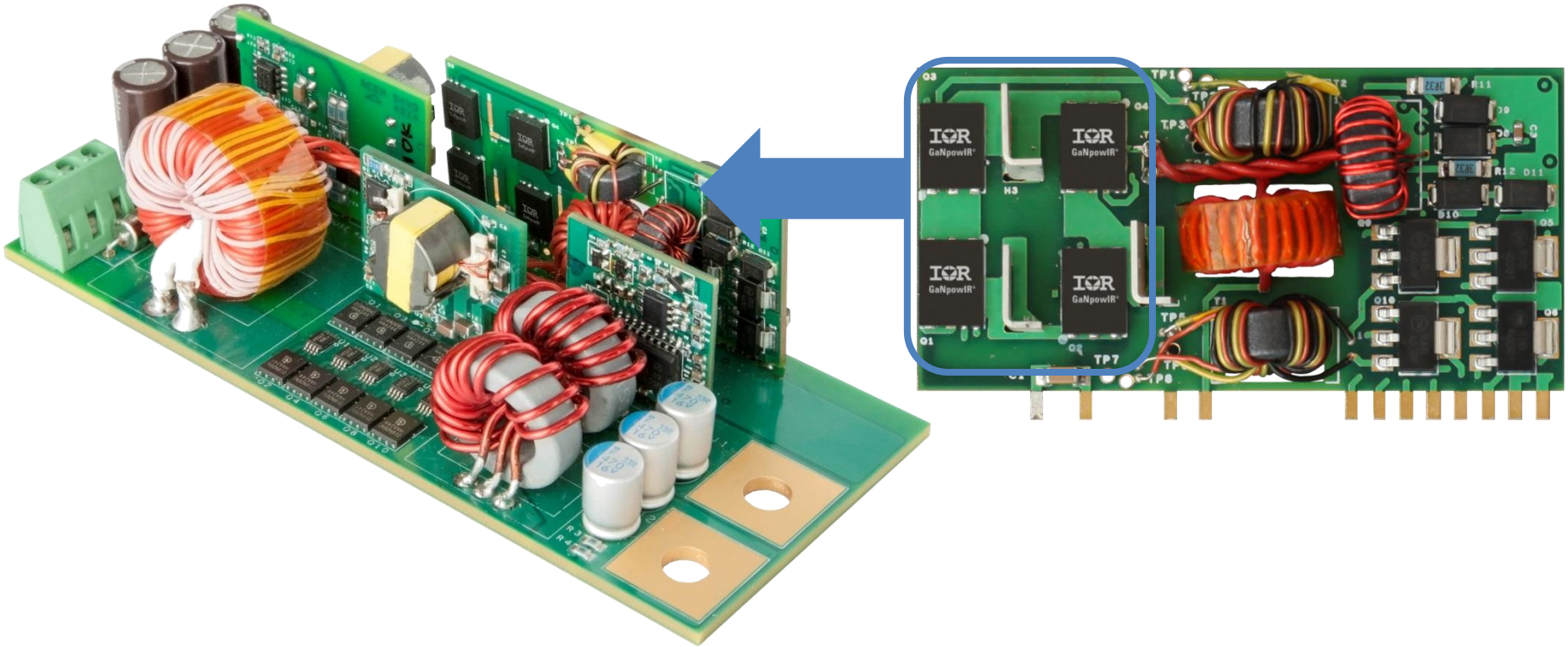
ZVS phase-shifted full-bridge

- ZVS over most of power range except light-load
- Current-doubler output effective for 12 V and below



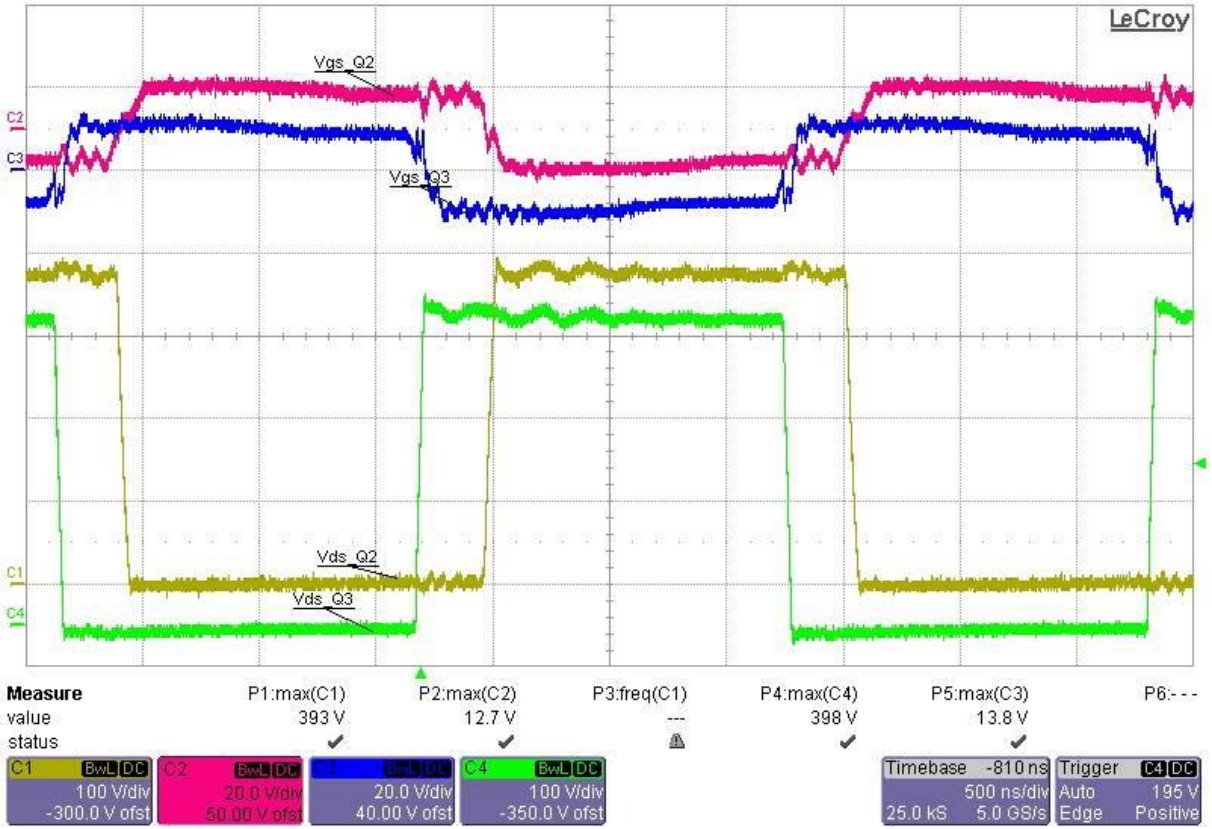
ZVS phase-shifted full-bridge

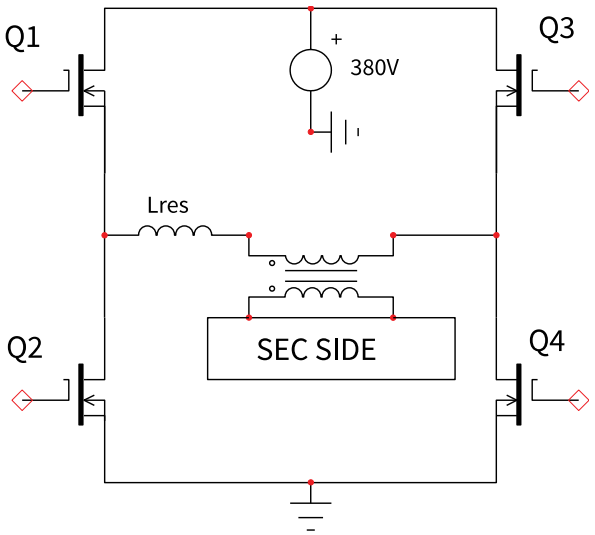
- 1 kW 380 V to 12 V
- 350 kHz
- 120 W/in^3



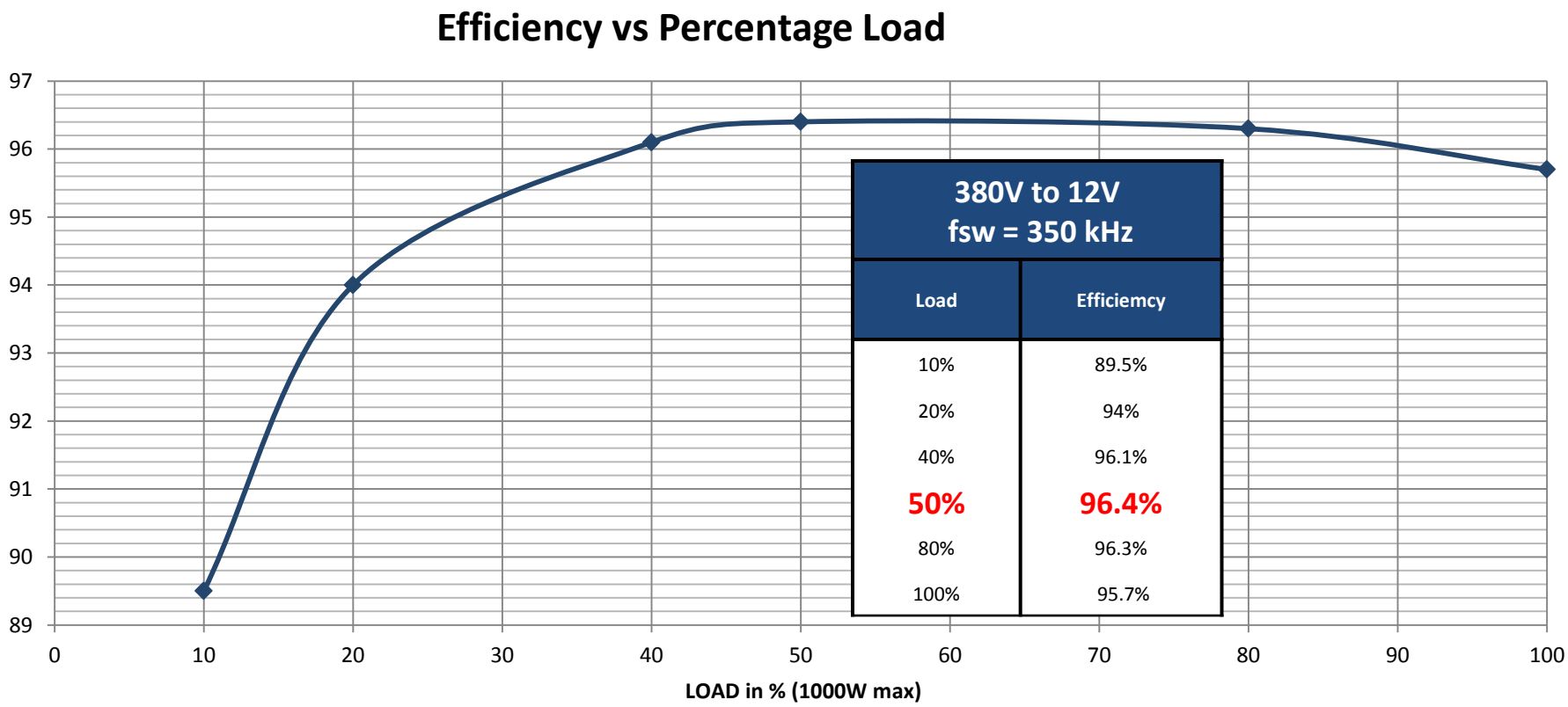
ZVS phase-shifted full-bridge

- Waveforms at 50% load



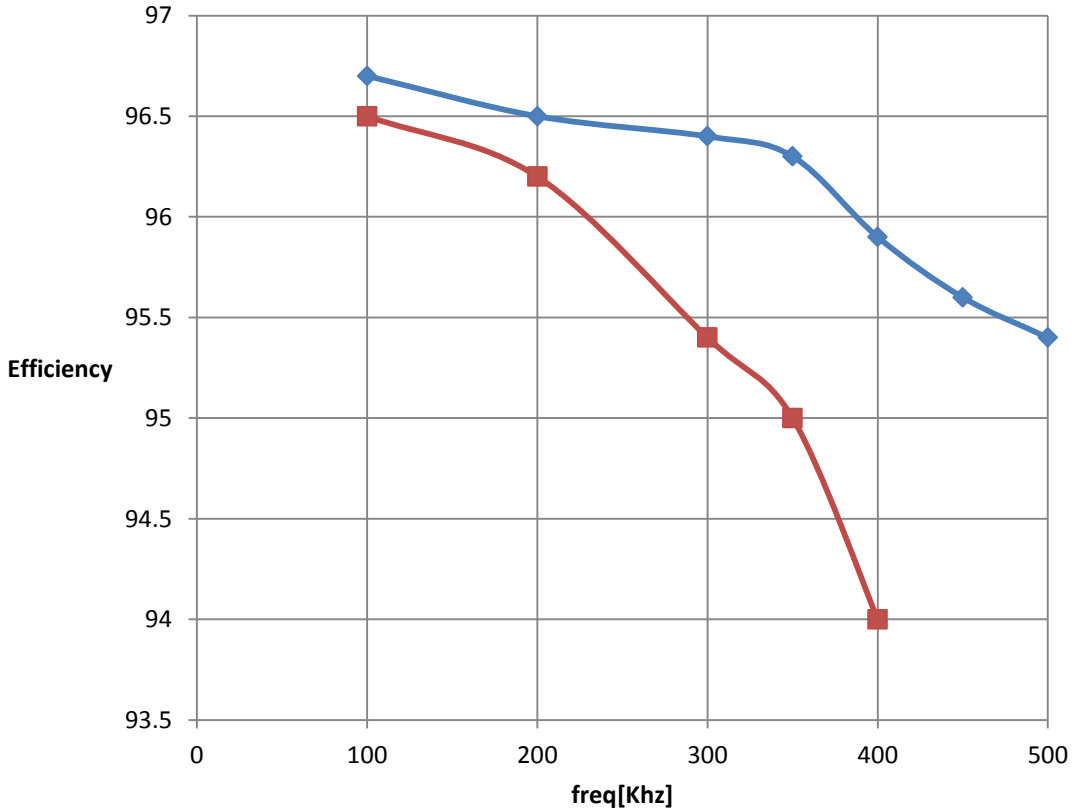


ZVS phase-shifted full-bridge efficiency



Efficiency vs Frequency at half-load

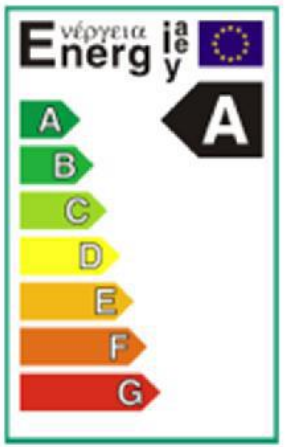
- Comparing GaN cascode vs superjunction



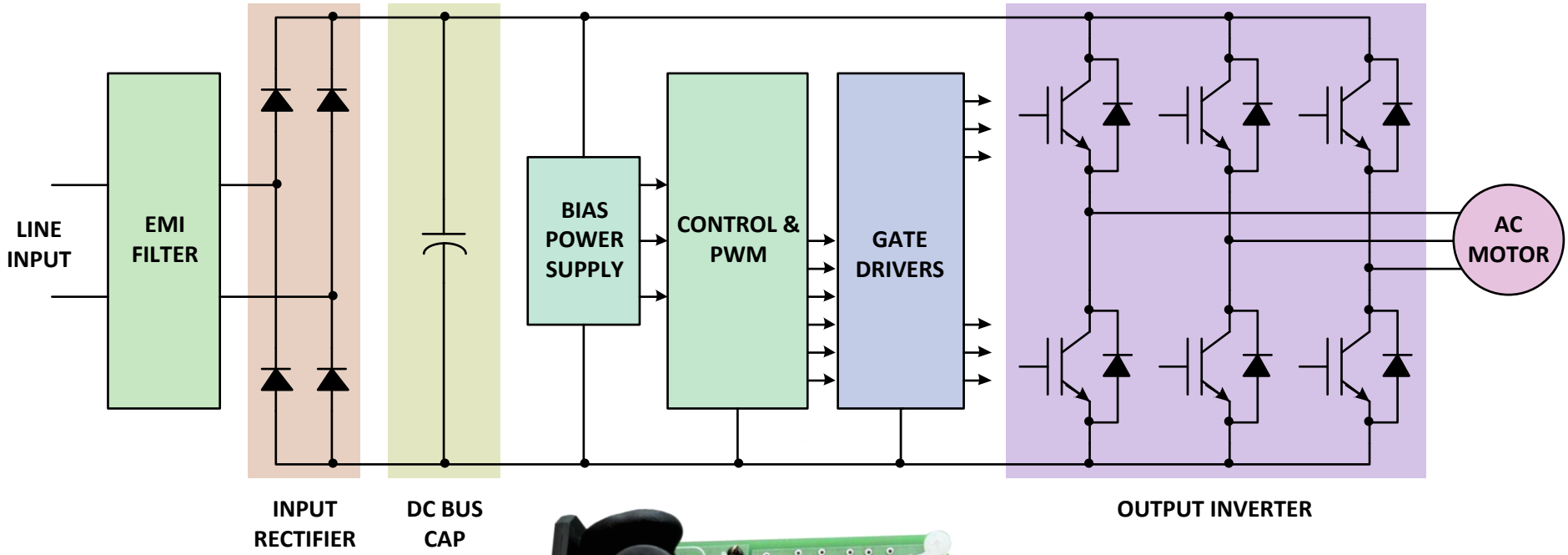
Freq [Khz]	Efficiency_GaN [%]	Efficiemcy_SJ [%]
100	96.7	96.5
200	96.5	96.2
300	96.4	95.4
350	96.3	95
400	95.9	94
450	95.6	
500	95.4	

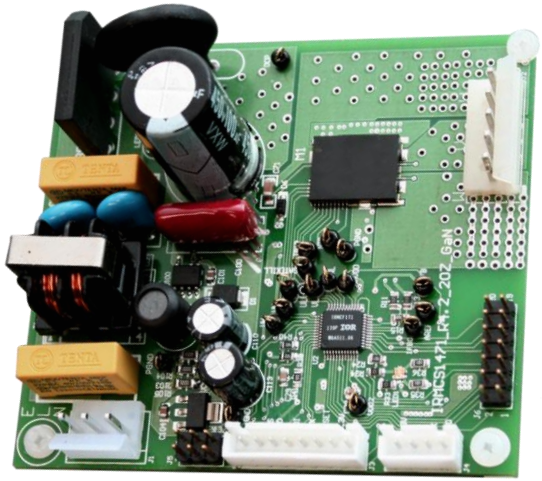
Why GaN for Motor Drive Applications?

- Switching speed is not necessarily a key issue for drives:
- Typically want dv/dt <6V/ns (GaN can switch >10x faster)
  - I=C dv/dt currents in motor windings can result in failures
  - Corona and partial-discharge creates ozone and erodes insulation
  - Common-mode currents forced through bearings, eroding races
- Yet customers still want higher efficiency, increased density
- Compressor drives have even more constraints:
  - Very low leakage current mandates small Y-cap values (EMI)
  - Newer "green" refrigerants have very high permittivity
- Goal is to improve light-load efficiency (<25% of full power)
- EU2013 directive for Energy Saving A+++ Class
- Reducing losses also improves packaging density

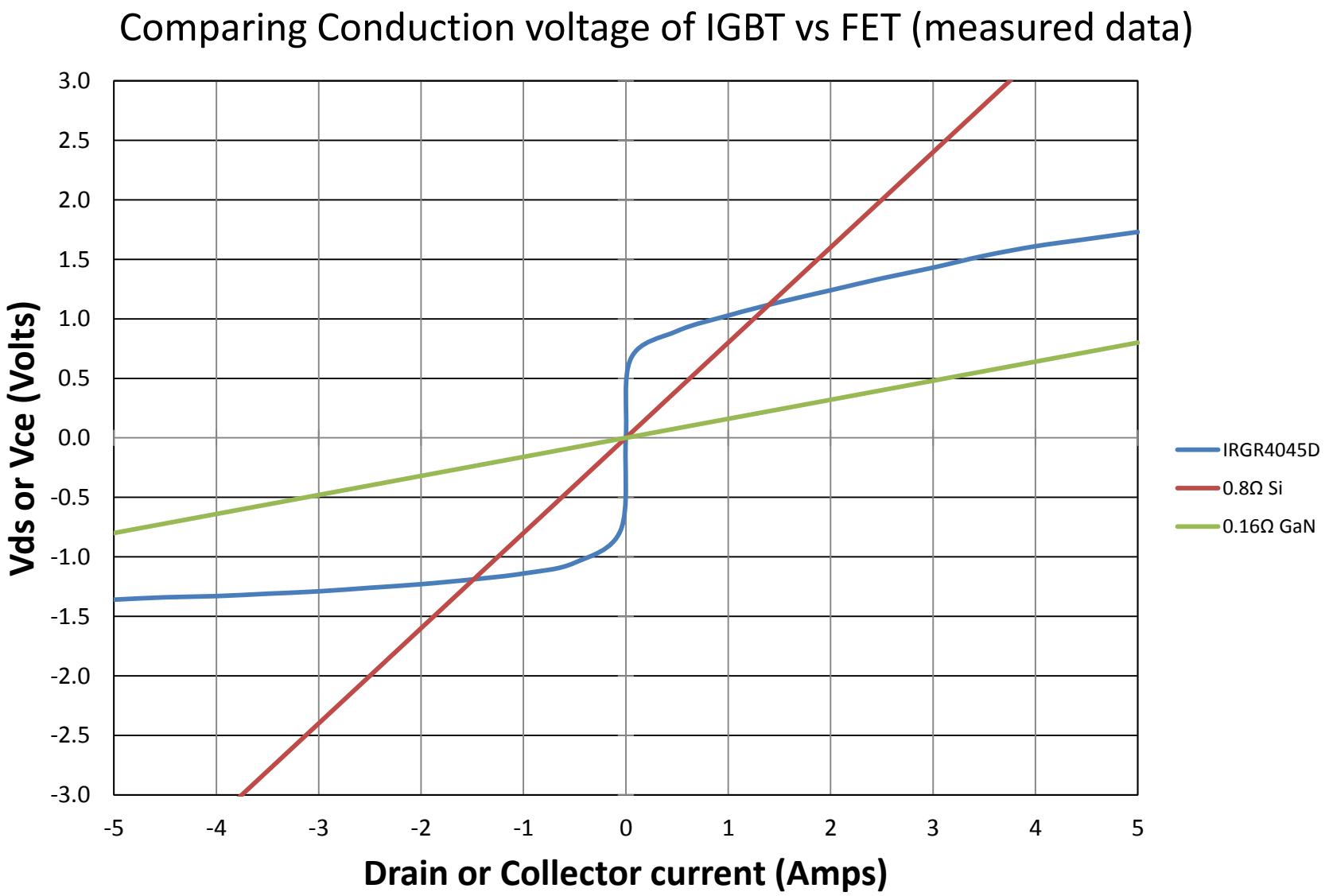


Typical Compressor Drive Today

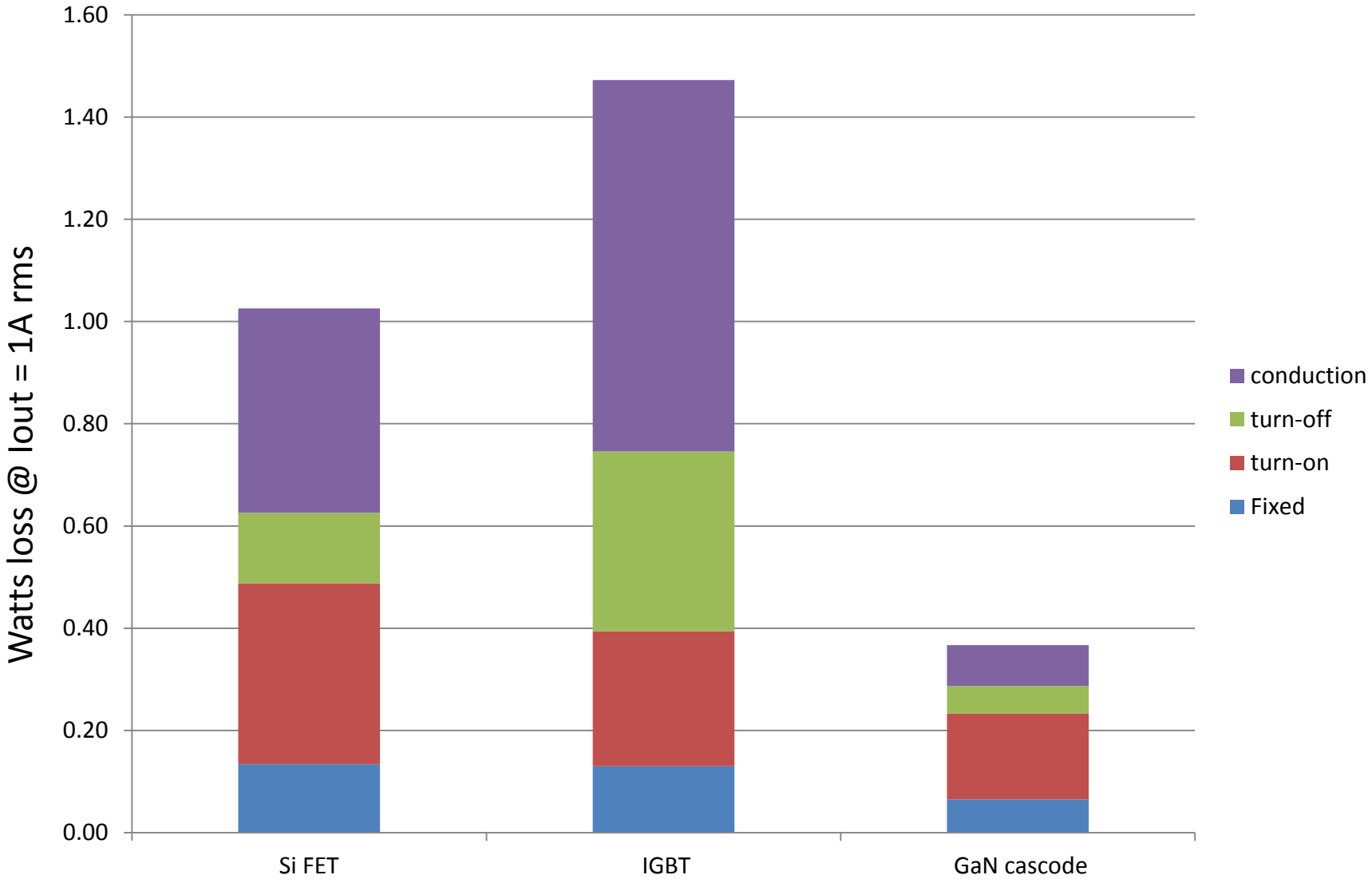




Conduction Voltage for Same Footprint Size



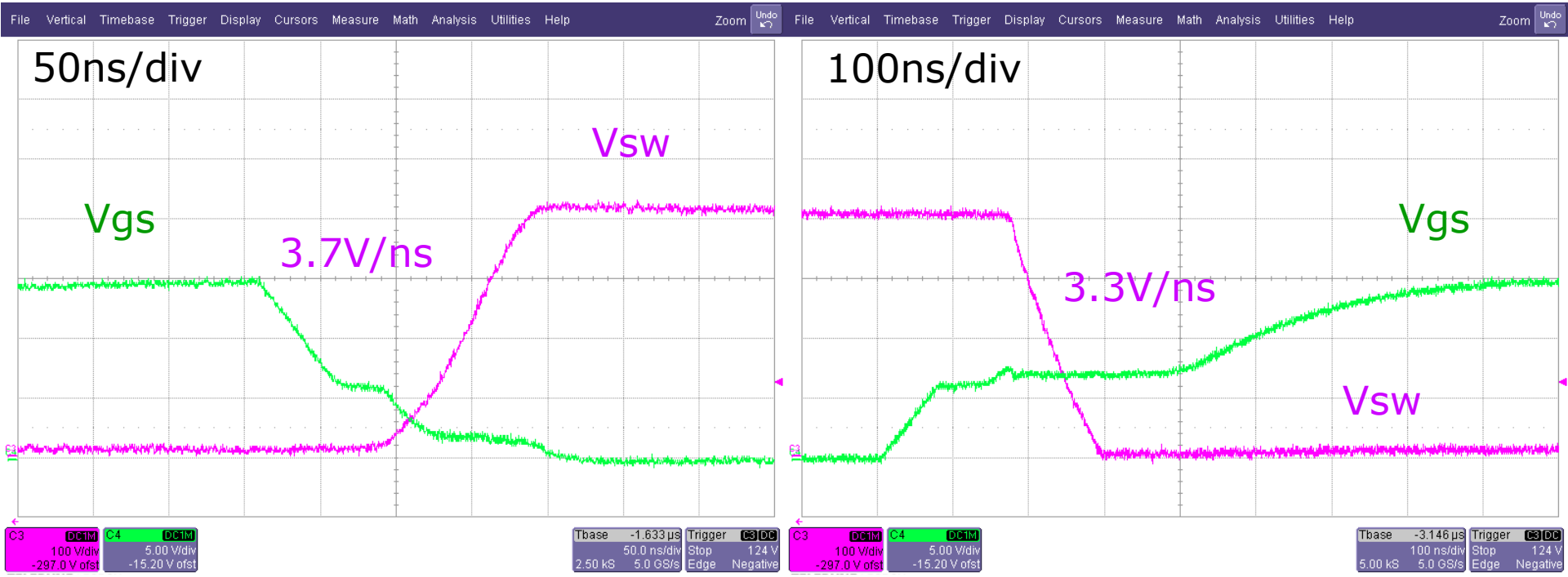
Total Power Loss Summary (per switch)



Cascode GaN dv/dt control via Gate Modulation

2A Turn off

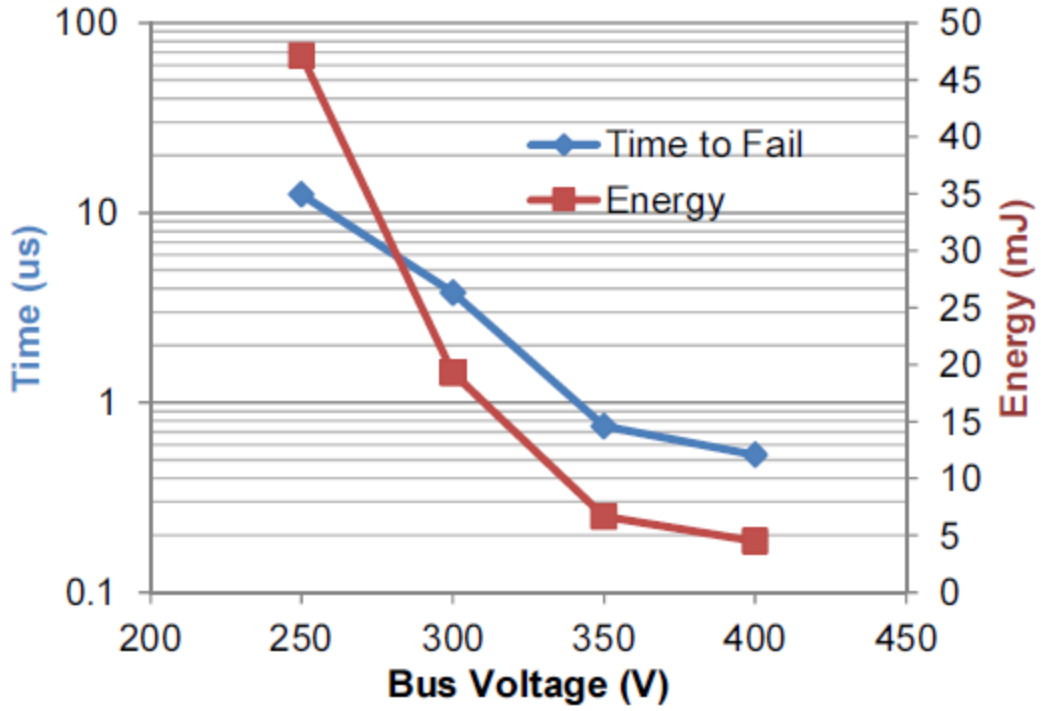
2A Turn on



- Dv/dt control possible by modulating cascode gate-drive current
- This places HEMT in linear region increasing switching times and losses
- Unknown if this affects long-term reliability – further study needed

GaN HEMT Short-Circuit Capability

- Initial devices are high-gain – limited SCSOA
  - Typically ~ 1 µs @ 300V
- Likely tradeoff between gain and SCSOA similar to IGBTs



Ref: Xing Huang; Dong Young Lee; Bondarenko, V.; Baker, A.; Sheridan, D.C.; Huang, A.Q.; Baliga, B.J., "Experimental study of 650V AlGaN/GaN HEMT short-circuit safe operating area (SCSOA)," Proc. ISPSD pp.273,276, 15-19 June 2014

Summary

- GaN HEMTs offer performance improvements for power electronic applications
  - Benefits are strongly topology-dependent
  - Just dropping GaN into existing circuit may show little benefit
- Half-bridge topology is good match for GaN
  - Half-bridge requires good dynamic reverse conduction
  - Both cascode and e-mode GaN devices benefit half-bridge
- Higher efficiency at same frequency
  - By use of better topologies i.e. totem-pole PFC
- Higher frequency at high efficiency
  - Lower charge of GaN helps HF performance
  - E.g. LLC example and ZVS full-bridge example

Questions?

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8) Xiucheng Huang, Fred C. Lee, Qiang Li, "Characterization and Enhancement of 600V Cascode GaN Device," CPES PMC Review, March 11, 2015
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