Power MOSFET avalanche design guidelines

Application note

About this document

Scope and purpose

This application note is a revised edition of AN-1005 “Power MOSFET Avalanche Design Guideline” **[1]** published by International Rectifier, now Infineon Technologies. Together with other application notes **[2][3]** available on Infineon Technologies’ website, this will help design engineers understand avalanche breakdown and read avalanche ratings on datasheets properly.

Intended audience

Electrical design engineers, technicians, and developers of electronic systems.

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1 Introduction

1.1 Overview

International Rectifier, now Infineon Technologies, has been providing rugged power MOSFET semiconductor devices since the 1980s. To better understand and utilize Infineon Technologies' IR MOSFET™, it is important to explore the theory behind avalanche breakdown and to understand the design and rating of rugged MOSFETs. Several different avalanche ratings are explained, and their usefulness and limitations in design are considered.

1.2 Avalanche mode defined

All semiconductor devices are rated for a certain maximum reserve voltage (BV_{DSS} for power MOSFETs). Operation above this threshold will cause high electric fields in reverse-biased p-n junctions. Due to impact ionization, the high electric fields create electron-hole pairs that undergo a multiplication effect leading to increased current. The reverse current flow through the device causes high power dissipation, associated temperature rise and potential device destruction.

1.3 Avalanche occurrences in industry applications

1.3.1 Flyback converter example

Some designers don't allow for avalanche operation; instead, a voltage derating is maintained between rated B_{VDSS} and V_{DD} (typically 90 percent or less). In such instances, however, there is still a possibility that greater than planned for voltage spikes can occur, so even the best designs may encounter an infrequent avalanche event. One such example, a flyback converter, is shown in **Figure 1**.

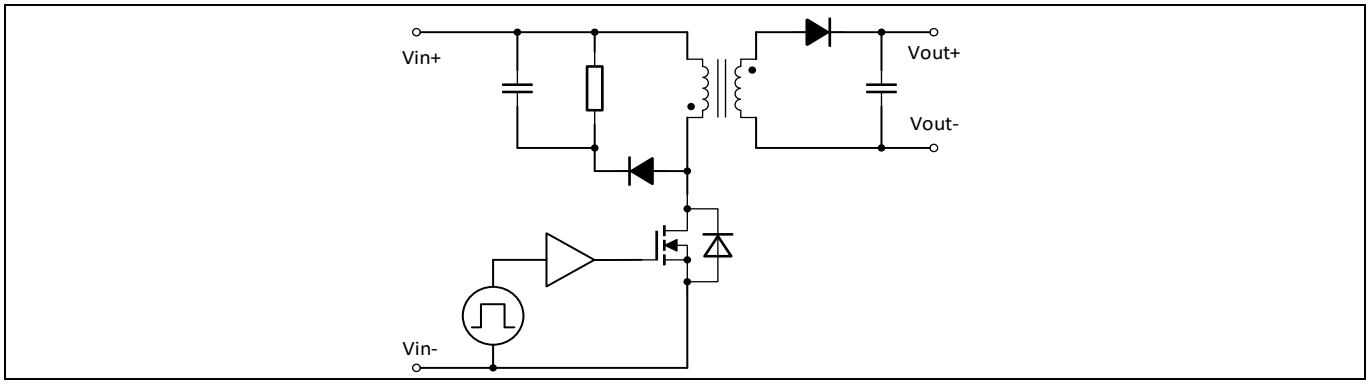

Figure 1 Simplified flyback converter circuit example

During MOSFET operation of the flyback converter, energy is stored in the leakage inductor. If the inductor is not properly clamped, during MOSFET turn-off the leakage inductance discharges through the primary switch and may cause avalanche operation, as shown in the V_{DS}, I_{DS} and V_{GS} vs. time waveforms in **Figure 2**. In this application, built-in avalanche capability is an additional power MOSFET feature and safeguards against unexpected voltage overstress that may occur at the limits of circuit operation.

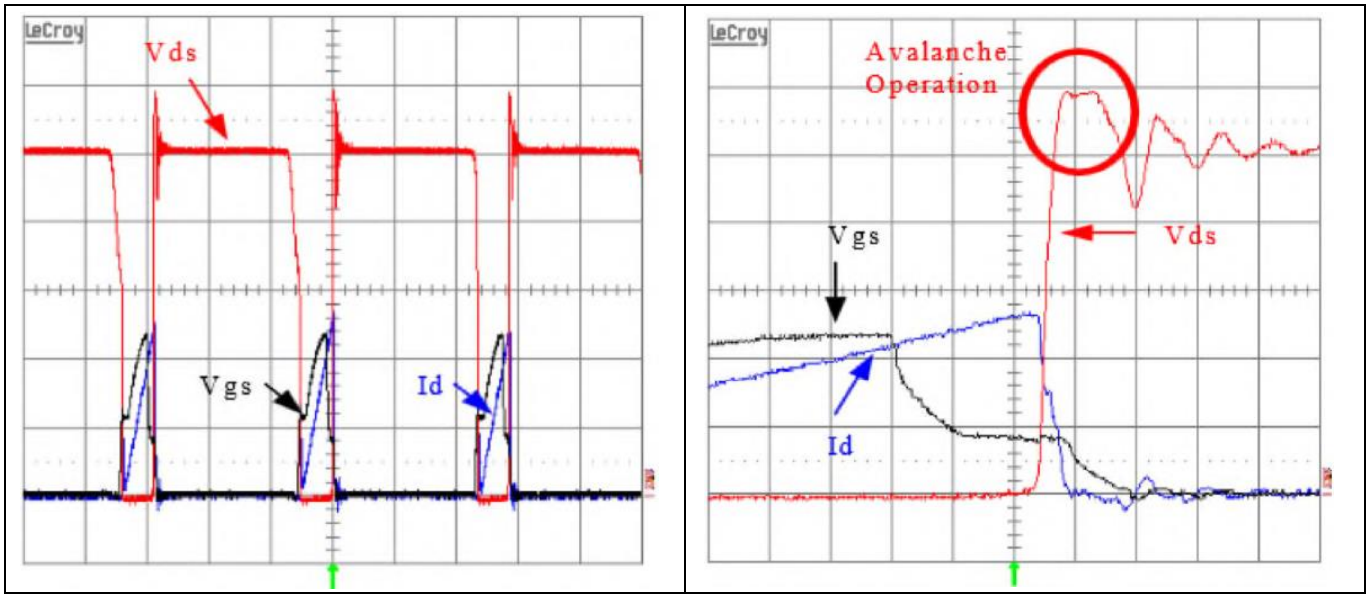

Figure 2 Flyback converter switch under avalanche waveforms (left) and detail (right)

1.3.2 Automotive fuel injector coil example

Other applications, such as automotive fuel injection, are designed to experience avalanche. See the example injector coil circuit in **Figure 3** (left). During switch operation, energy is stored in the solenoid inductance. Following switch turn-off, the inductor discharges on the primary switch, causing avalanche operation as illustrated in **Figure 3** (right). In this application, avalanche tested and rated devices are necessary for reliable circuit operation.

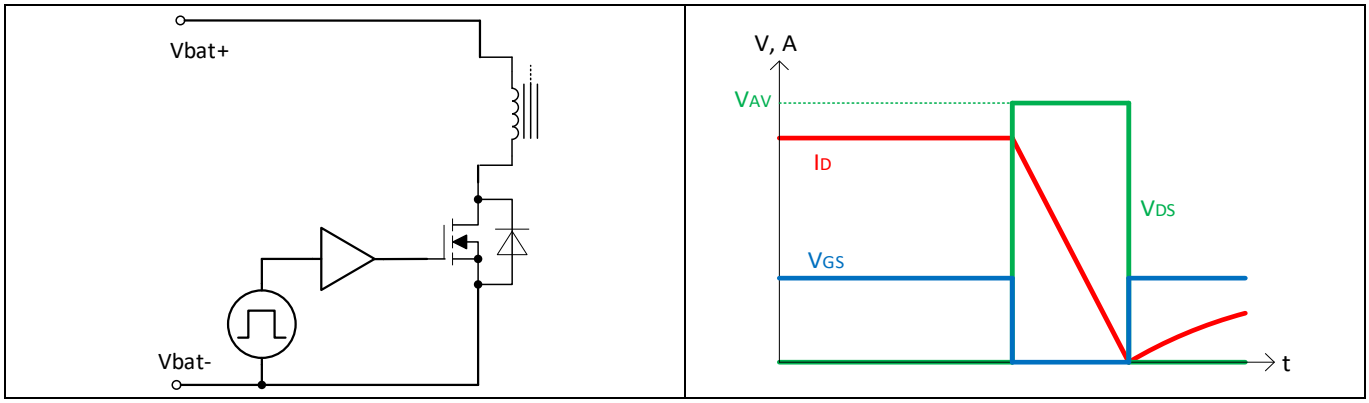

Figure 3 Simplified fuel injector coil circuit example (left) and illustrated waveforms in avalanche operation (right)

2 Avalanche failure mode

2.1 Overview

Some power semiconductor devices are designed to withstand a certain amount of avalanche current for a limited time and can, therefore, be avalanche rated. Others will fail very quickly after the onset of avalanche. The difference in performance stems from particular device physics, design and manufacturing.

2.2 Power MOSFET device physics

All semiconductor devices contain parasitic components intrinsic to the physical design of the device. In power MOSFETs, these components include capacitors due to displaced charge in the junction between p and n regions, resistors associated with material resistivity, a body diode formed where the p+ body diffusion is made into an n- epi-layer, and NPN (bi-polar junction transistor sequence, or BJT) formed where the n+ source contact is diffused. See **Figure 4** for a power MOSFET schematic that incorporates the parasitic components listed above and for a complete circuit model of the device.

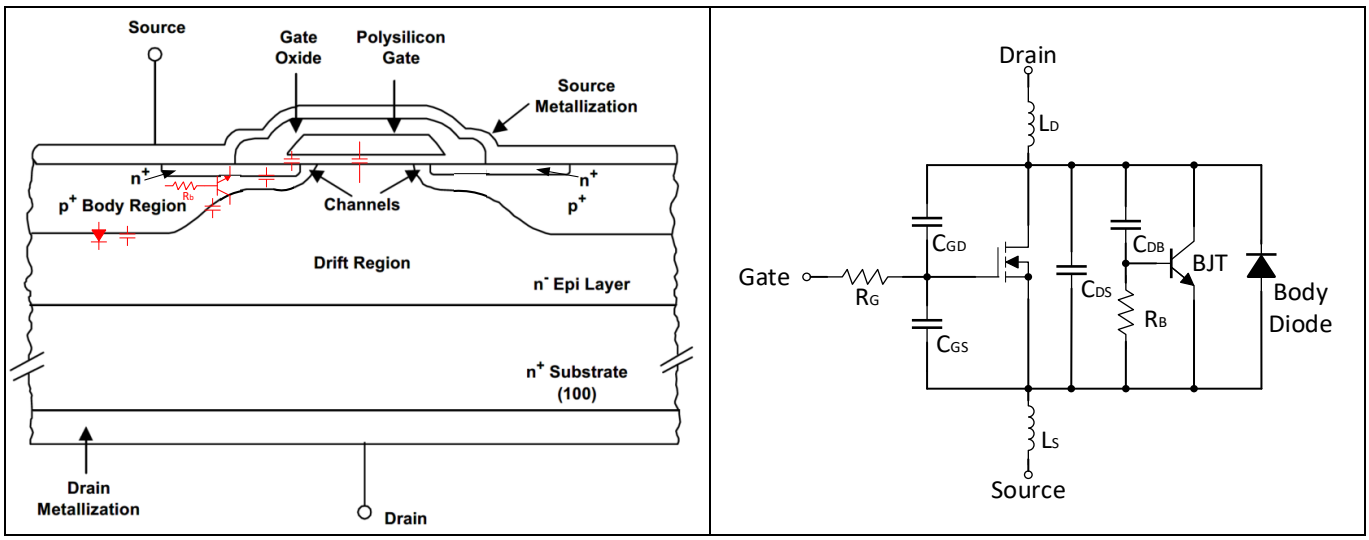

Figure 4 Power MOSFET schematic (left) and circuit model (right)

In avalanche, the p-n junction acting as a diode no longer blocks voltage. With higher applied voltage a critical field is reached where impact ionization tends to infinity and carrier concentration increases due to avalanche multiplication. Due to the radial field component, the electric field inside the device is most intense at the point where the junction bends. This strong electric field causes maximum current flow in close proximity to the parasitic BJT, as depicted in **Figure 5**. The power dissipation increases temperature, thus increasing R_b, since silicon resistivity increases temperature. From Ohm's Law we know that increasing resistance at constant current creates an increasing voltage drop across the resistor. When the voltage drop is sufficient to forward bias the parasitic BJT, it will turn on with potentially catastrophic results, as control of the switch is lost.

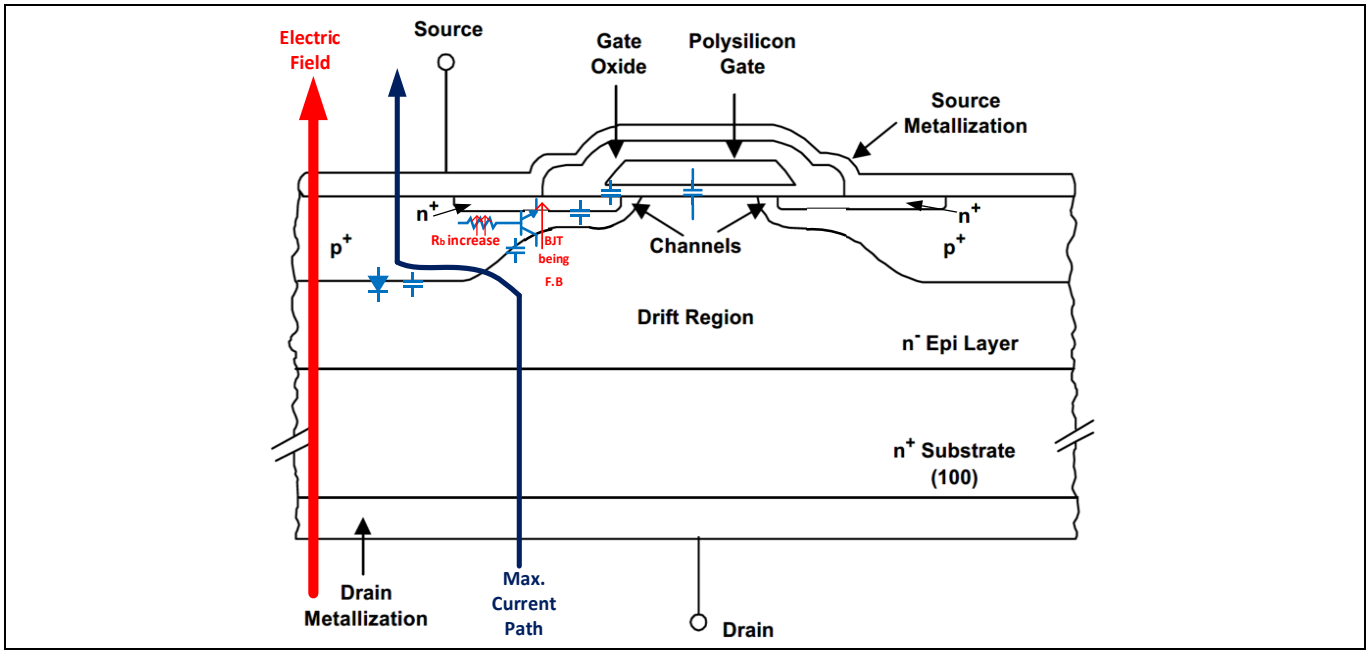

Figure 5 Power MOSFET schematic under avalanche

Typical modern power MOSEFTs have millions of identical trenches, cells, or strips in parallel to form one device, as shown in **Figure 6**. For robust designs, then, avalanche current must be shared among many cells/strips evenly. Failure will then occur randomly in a single cell, at a high temperature. In weak designs, the voltage required to reach an electric field is lower for one device region (group of cells) than for others, so critical temperature will be reached more easily, causing the device to fail in one specific area.

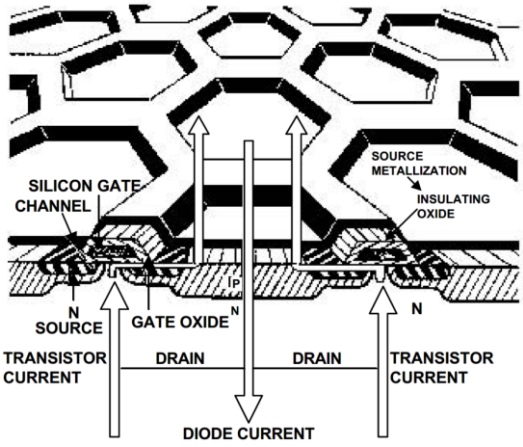

Figure 6 Planar MOSFET structure example

2.3 Rugged MOSFETs

First introduced in the mid-1980s, avalanche rugged MOSFETs are designed to avoid turning on the parasitic BJT until a very high temperature and/or very high current avalanche current occurs. This is achieved by:

- Reducing the P+ region resistance with higher doping diffusion
- Optimizing cell/line layout to minimize the “length” of R_b

The net effect is a reduction of R_b, and thus the voltage drop necessary to forward bias the parasitic BJT will occur at a higher current and temperature. Avalanche rugged MOSFETs are designed to contain no single consistently weak spot, so avalanche occurs uniformly across the device surface until failure occurs randomly in the active area. Utilizing the parallel design of cells, avalanche current is shared among many cells and failure will occur at higher current than for designs with a single weak spot. A power MOSFET which is well designed for ruggedness will only fail when the temperature substantially exceeds rated T_{JMAX}. An analysis of various sets of IR MOSFET™ tested to destruction indicates that failure spots occur randomly in the active area. Some sample areas are shown in **Figure 7**.

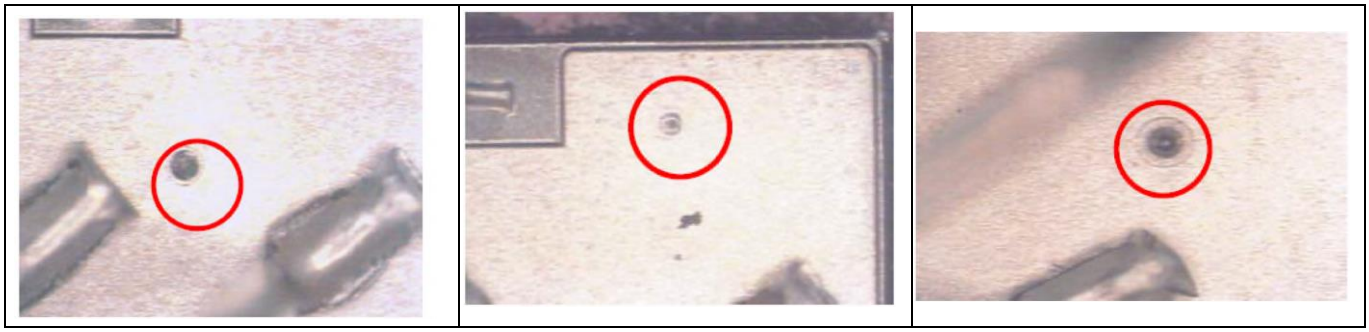

Figure 7 Examples of power MOSFET random device failure spots

The risk of the manufacturing process leading to “weak cell” parts is always present. The SEM cross-section micrograph in **Figure 8** (left) shows one such example. The source metal contacts the n+ layer at the near surface, but not the p+ layer. As a result, the BJT base is floating and easily triggerable. An example of a good contact is shown in **Figure 8** (right). The source metal contacts and shorts the n+ layer to the p+ layer, thus suppressing the parasitic BJT operation. Parts with weak cells such as those shown on the left of **Figure 8** can be removed from the population by 100 percent avalanche (E_{AS}) stress testing during production.

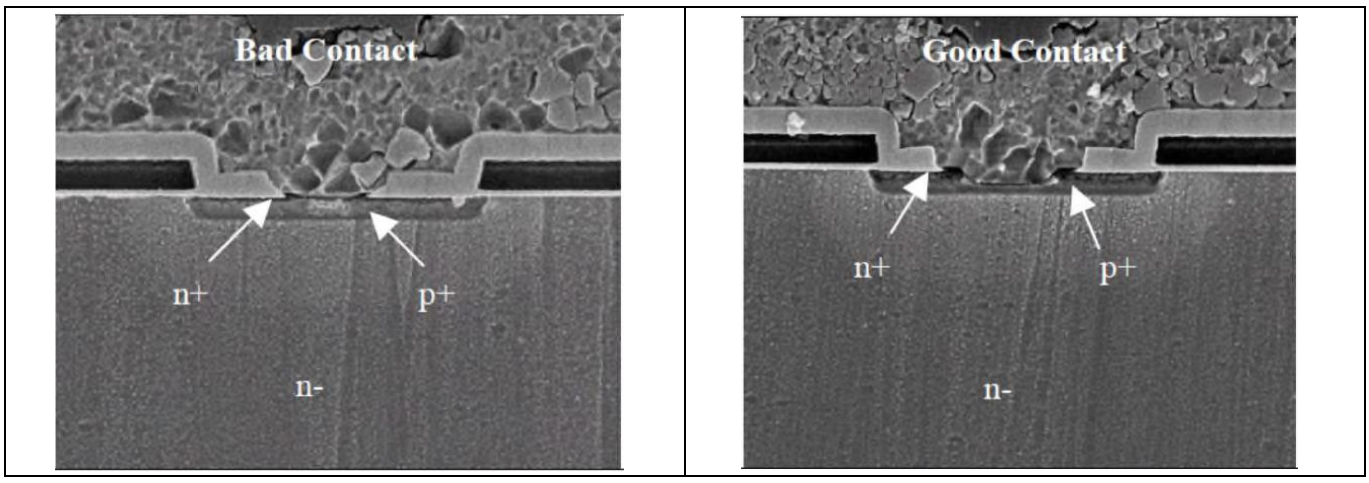

Figure 8 Power MOSFET cross-section images – bad contact (left) and good contact (right)

Through many years of experience, Infineon Technologies has been evolving design and manufacturing disciplines to validate power MOSFET design ruggedness of E_{AS} rated devices. A three-step approach is now used during the design process:

1) Statistically significant samples of prospective designs are tested to failure under test conditions chosen to reach extremes in temperature and current stress. Representative parts from DOE elements are tested to ensure uniform avalanche failure across expected variation of critical process steps.

2) Each design is tested to failure across temperature and inductor (time in avalanche) to ensure that failure extrapolates to zero at a temperature well in excess of T_{JMAX}. (See the example in **Figure 9** of I_{AS} at failure vs. T_{START}, below.)

3) A sample of final design parts are stressed with repetitive avalanche pulses with values to raise junction temperature T_{JMAX}.

This three-step solution helps ensure that designs are rugged and can be avalanche rated. To summarize, the following factors provide rugged avalanche MOSFETs:

- Improved device design
  - To mute the parasitic BJT by reducing R_b
  - To eliminate the effect of weaker cells in particular positions of the layout (cells along device termination, gate bussing, etc.)
- Improved manufacturing process
  - To guarantee more uniform cells
  - To reduce incomplete or malformed cell occurrences
- Improved device characterization
  - To ensure devices fail uniformly across a wide range of I_D and temperature values
  - To ensure devices fail at very high (extrapolated) temperature
  - To ensure devices are capable of surviving multiple avalanche cycles at the thermal limit
- 100 percent avalanche stress testing in production

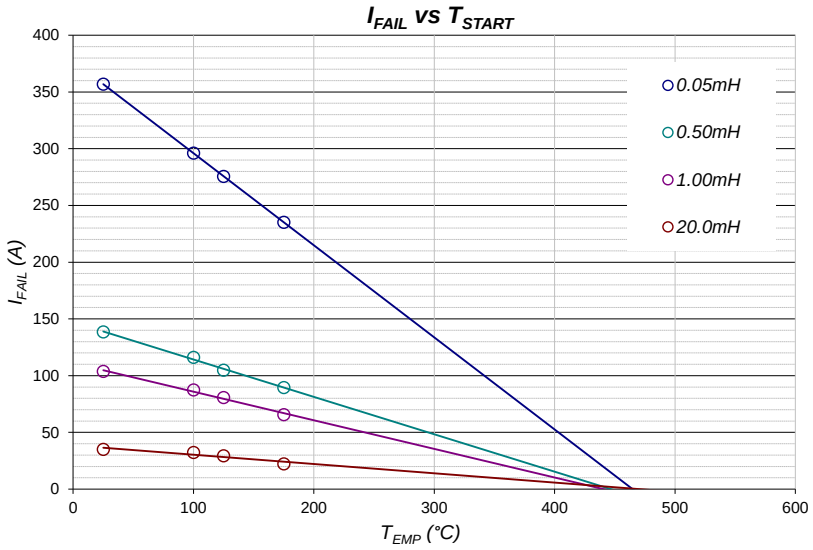

Figure 9 Example plot of I_{AS} at failure vs. T_{START} with various inductances

3 Avalanche testing detail

3.1 Overview

Infineon performs avalanche stress testing on its power semiconductor devices to ensure new designs conform to avalanche ratings, to validate parts for ruggedness and to screen for weak devices.

3.2 Single pulse unclamped inductive switching

During the mid-1980s, International Rectifier initially used the single pulse unclamped inductive switching test circuit for avalanche testing, as shown in **Figure 10** (left). This circuit was referenced in older “legacy” product datasheets.

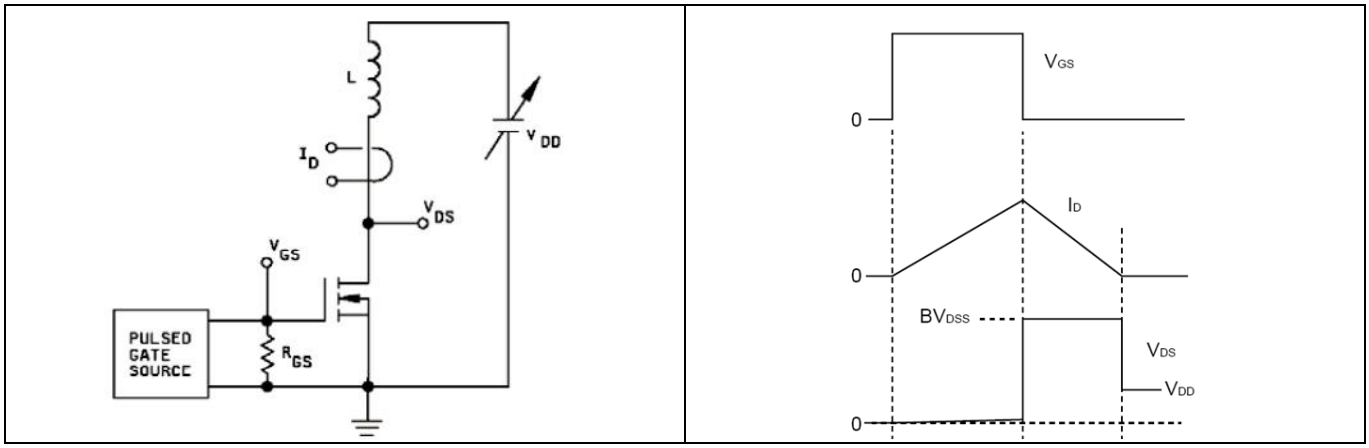

Figure 10 Single pulse unclamped inductive switching test circuit (left) and illustrated output waveforms (right)

From the output waveforms in **Figure 10** (right), we can calculate the single pulse avalanche energy (E_{AS}) as:

$$E_{AS} = \frac{L \cdot I^2{}_{AS}}{2} \cdot \frac{V_{DS}}{V_{DS} - V_{DD}} \quad (1)$$

The measured energy values depend on the avalanche breakdown voltage, which tends to vary during the discharge period due to the temperature increase. Also note that V_{DS}-V_{DD} may become quite small for low-voltage devices, limiting the use of this circuit because it introduces high levels of test error.

3.3 Decoupled V_{DD} voltage source

To surpass the limitations of the single pulse unclamped inductive switching test circuit, the decoupled V_{DD} voltage source has been implemented as illustrated in **Figure 11** since the late 1980s.

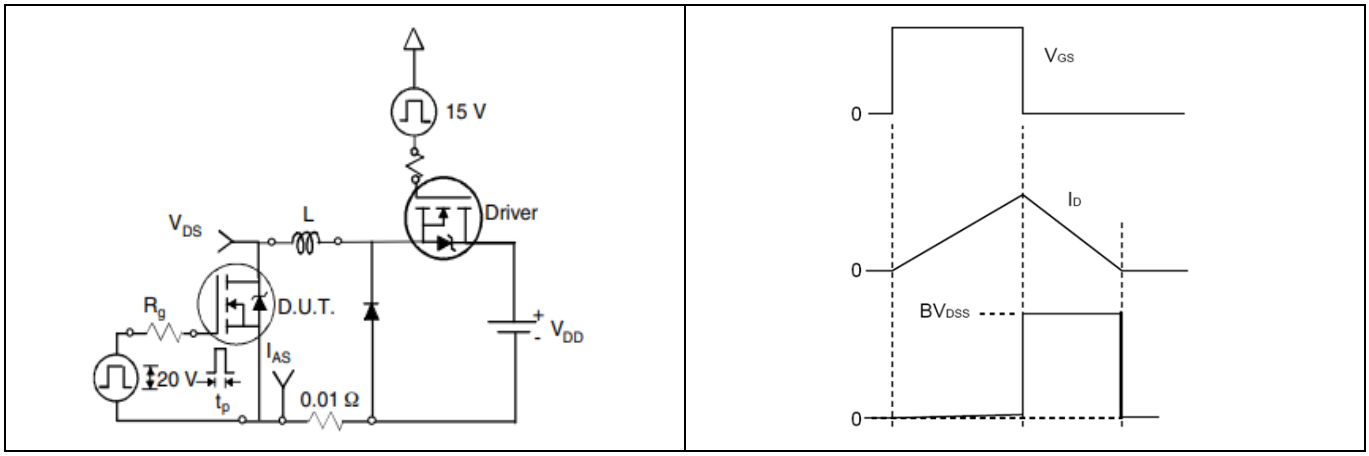

Figure 11 Decoupled V_{DD} voltage source UIS test circuit (left) and illustrated output waveforms (right)

Here a driver FET and recirculation diode are added so that the voltage drop across the inductor during avalanche is equal to the avalanche voltage. With this circuit (ignoring the regular ESR in the inductor) the energy can be simply calculated as:

$$E_{AS} = \frac{1}{2} L \cdot (I_{AS})^2 \quad (2)$$

A better and more accurate reading of the avalanche energy can be obtained by measuring instantaneous voltage and current in the device and integrating it as described in the following equation:

$$E_{AS} = \int_{t_1}^{t_2} v_{(AV)DSS}(t) \cdot i_{AS}(t) \cdot dt \quad (3)$$

For further reference, **Figure 12** depicts ideal and actual avalanche waveforms, respectively.

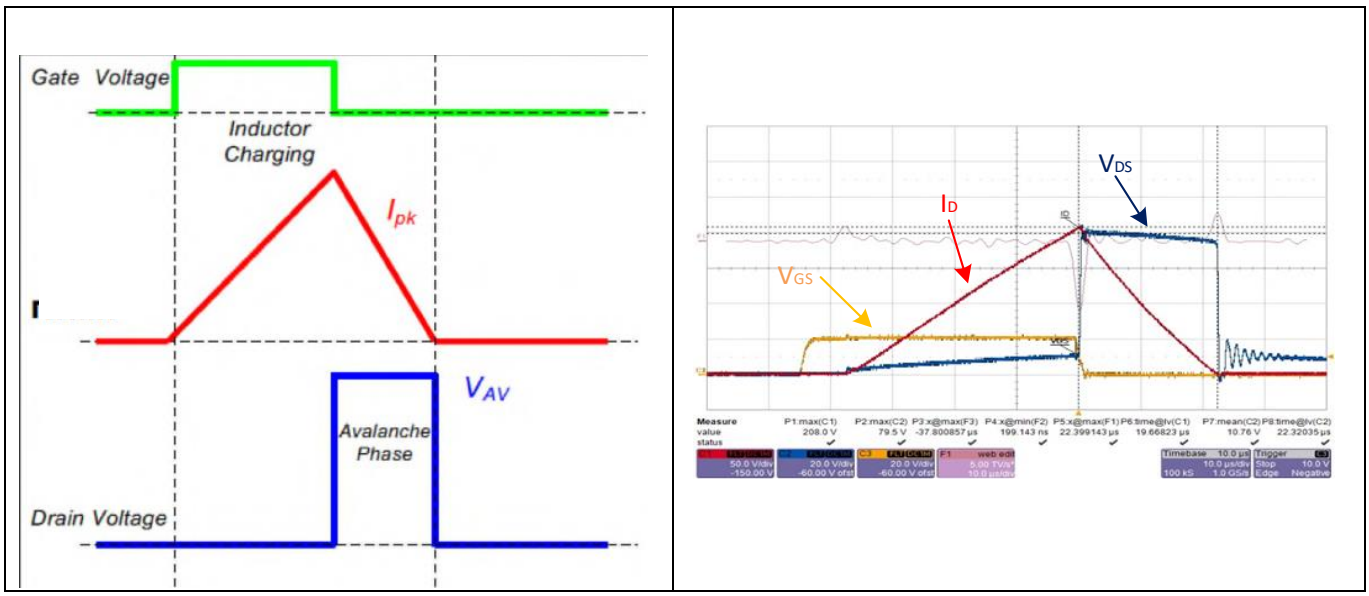

Figure 12 Ideal illustrated avalanche waveform (left) and actual waveforms example (right)

4 Avalanche rating

4.1 Overview

Generally, there are three approaches to avalanche rating devices:

1. Thermal limit approach: the device is rated to the value(s) of energy, E_{AS}, that causes an increase in junction temperature up to T_{JMAX}. E_{AS} avalanche rated MOSFETs provided by Infineon Technologies, including International Rectifier, are rated in this manner.
2. Statistical approach: devices are tested up to the failure point. The rating is given using statistical tools (e.g., average (E_{AS}) - 6σ) applied to the failure distribution. Some IR MOSFET™ are rated in this way and indicated as $E_{AS(tested)}$, generally in addition to the thermally limited rating. However, some MOSFET suppliers provide only this rating on their datasheets.
3. No rating at all.

While the first two approaches provide a value for avalanche energy, the designer must make sure they understand the important differences outlined below.

4.2 E_{AS} thermal limit approach

4.2.1 Single pulse

The single pulse avalanche rating (E_{AS}) assumes that the device is rugged enough to sustain avalanche operation under a wide set of conditions subject only to not exceeding the maximum allowed junction temperature. Typically, the avalanche rating on the datasheet is the value of the energy that increases the junction temperature from 25°C to T_{JMAX}, assuming a constant case temperature of 25°C and assuming a specified value of I_D.

For example, consider Infineon Technologies' IRF7749L1TRPbF as excerpted from the datasheet [4] in **Figure 13**:

IR MOSFET-DirectFET™
IRF7749L1TRPbF

DirectFET™ N-Channel Power MOSFET

V_{DSS}	60V
$R_{DS(on)}$ typ. @ V_{GS} = 10V	1.1mΩ
$R_{DS(on)}$ max @ V_{GS} = 10V	1.5mΩ
I_{D} (Silicon Limited)	345A ⑦
I_{D} (Package Limited)	375A ①

Operating Junction	T_J	-	-55 to + 175	°C
Storage Temperature Range	T_{STG}	-		

Table 4 Avalanche characteristics

Parameter	Symbol	Values	Unit
Single Pulse Avalanche Energy (Thermally Limited ③	E_{AS}	315	mJ
Single Pulse Avalanche Energy (Tested) ③	E_{AS}	714	
Avalanche Current ②	I_{AR}	See Fig.15,16, 19a, 19b	A
Repetitive Avalanche Energy ②	E_{AR}		mJ

Notes:

① Package limit current based on source connection technology
② Repetitive rating; pulse width limited by max. junction temperature.
③ Limited by $T_J$max, starting T_J = 25°C, L = 0.044mH, R_G = 50Ω, I_{AS} = 120A, V_{GS} =10V.

Figure 13 Device summary, avalanche characteristics and footnote from the IRF7749L1TRPbF datasheet

With the following initial conditions as described in the footnote:

- Single pulse avalanche current: I_{AS} = 120 A
- Starting temperature: T_{START} = 25°C
- Inductor value: L = 44 µH

To calculate the temperature increase due to the avalanche power dissipation, we utilize a thermal model with Ohm's Law equivalence. The resulting equation follows:

$$\Delta T_J = Z_{TH} \cdot P_{AV} \quad (4)$$

The average power dissipated during avalanche can be calculated as:

$$P_{AV} = \frac{1}{2} \cdot \frac{V_{AV} \cdot I_{AS} \cdot t_{AV}}{t_{AV}} = 0.5 \cdot 78\,V \cdot 120\,A = 4680\,W \quad (5)$$

Avalanche voltage can be estimated as:

$$V_{AV} \cong 1.3 \cdot BV_{DSS} = 1.3 \cdot 60\,V = 78\,V \quad (6)$$

Now from equation (2) we can calculate:

$$E_{AS} = \frac{1}{2} L \cdot (I_{AS})^2 = 0.5 \cdot 44\,\mu H \cdot (120A)^2 = 316.8\,mJ \quad (7)$$

which agrees with the datasheet value within rounding of the least significant digits.

The duration of the avalanche power pulse can be calculated, assuming the inductor is discharging with a constant voltage applied to it, as:

$$t_{AV} \cong L \cdot \frac{I_{pk}}{V_{AV}} = 44\,\mu H \cdot \frac{120\,A}{78\,V} \cong 67\,\mu s \quad (8)$$

The thermal impedance (Z_{TH}) for this pulse width can be read from the transient thermal impedance plot provided with the datasheet, as shown in **Figure 14**.

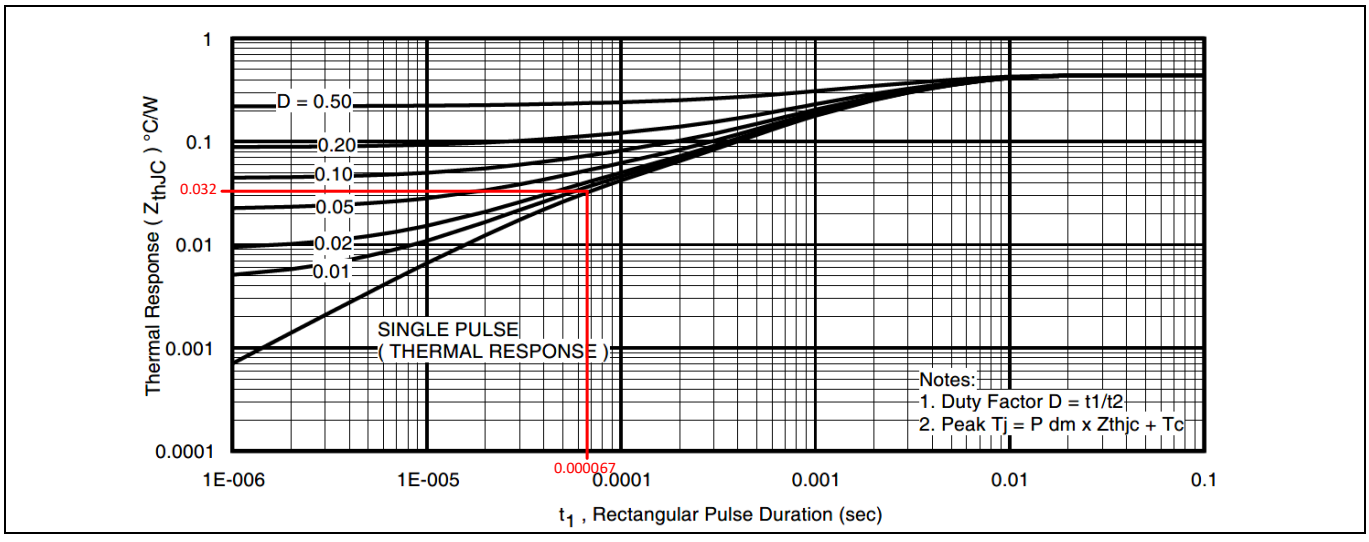

Figure 14 Maximum effective transient thermal impedance, junction-to-case from IRF7749L1TRPbF datasheet

The temperature increase due to avalanche and the final junction temperature can therefore be calculated using **equation (4)**:

$$\Delta T = Z_{TH} \cdot P_{AV} = 0.032 \cdot 4680W = 149.8℃ \quad (9)$$
$$T_J = T_{start} + \Delta T_J = 25℃ + 149.8℃ = 174.8℃ \leq T_{JMAX} = 175℃ \quad (10)$$

showing that the datasheet rating calculated T_{JMAX} within minor reading Z_{TH} from **Figure 14**.

Figure 15 is included in the datasheet for E_{AS} rated parts and shows many values of E_{AS} for varying starting T_J and I_D. Each point along the curves shown represents the energy necessary to raise the temperature to T_{JMAX}.

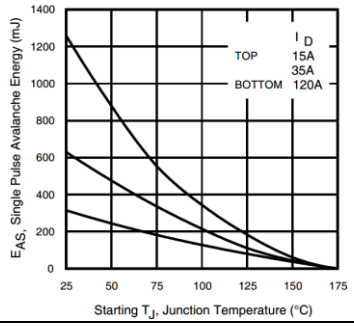

Figure 15 Maximum avalanche energy vs. temperature for various I_D values from the IRF7749L1TRPbF datasheet

Note that this curve belies the myth of trying to compare datasheet table E_{AS} values: by varying current and/or temperature the E_{AS} value can vary significantly. Specifying E_{AS} at lower I_D values results in higher E_{AS} even though the device stress (T_J) is the same.

4.2.2 Repetitive pulse

Historically, International Rectifier rated the repetitive pulse avalanche energy (E_{AR}) at 1/10000 of P_D at 25°C when E_{AR} was introduced on the datasheet. Later, this practice was supplanted by an explicit rating of avalanche operation up to the T_{JMAX} condition. Datasheets for some IR MOSFET™ utilizing this rating methodology also include:

- E_{AS}: the single pulse rating
- Z_{TH} graph: Z_{TH} vs. time for various duty cycles (example in **Figure 14** followed by discussion)
- E_{AS} graph: E_{AS} vs. T_{START} for various I_D values (example in **Figure 15** followed by discussion)
- E_{AR} graph: E_{AR} vs. T_{START} for various duty cycles, single I_D (example and discussion to follow)
- I_{AR} graph: typical avalanche current vs. pulse width for various duty cycles (example and discussion to follow)

The E_{AR} graph shows the avalanche energy necessary to raise the junction temperature from the starting temperature to T_{JMAX} for various duty cycles, at a given current. A sample E_{AR} graph is given in **Figure 16**. The top curve represents single pulse behavior at 5.1 A, while the bottom curve represents repetitive pulse operation at I_D level with 10 percent duty cycle. In repetitive pulse operation, the junction temperature doesn't have sufficient time between pulses to return to the ambient level. The larger the duty cycle, the higher the junction temperature will be when the next pulse arrives. Therefore, with increasing duty cycle, the avalanche energy required to raise the junction temperature to T_{JMAX} will be lower.

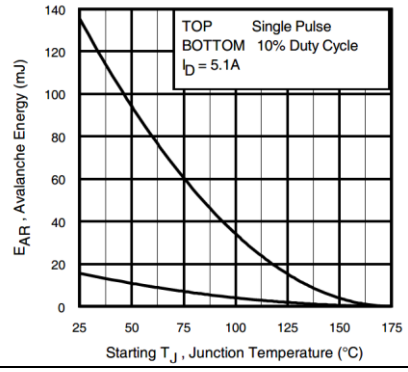

Figure 16 Maximum E_{AR} vs. T_{START} for various duty cycles, single I_D from the IRF7341GTRPbF datasheet

The I_{AR} graph (see **Figure 17**) shows how the avalanche current varies with the avalanche pulse width for various duty cycles, with a "budgeted" increase in junction temperature due to avalanche losses assumed at ΔT_J = 25°C. An effect similar to that in the E_{AR} graph occurs. In repetitive pulse operation, the junction temperature doesn't have sufficient time to decrease to the ambient temperature between pulses. As a result, the starting temperature for subsequent pulses will be higher than the ambient temperature. Therefore, a smaller amount of avalanche energy, corresponding to smaller avalanche current, will raise the junction temperature to T_{JMAX} for subsequent pulses. So for increasing duty cycles, the avalanche current required to raise the junction temperature by 25°C will decrease.

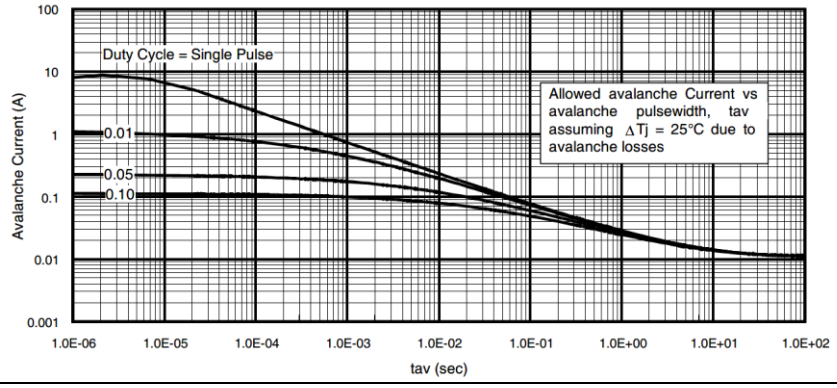

Figure 17 Typical I_{AR} vs. t_{AV} for various duty cycles from the IRF7341GTRPbF datasheet

A detailed specific example now follows to illustrate how to design for repetitive avalanche operation. This example will utilize the automotive fuel injection coil circuit, shown earlier in **Figure 4**, with the 55 V 5.1 A IRF7341GTRPbF MOSFET. Data on IRF7341GTRPbF is excerpted from the datasheet **[5]** in **Figure 18**.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	55	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	5.1	A
I_D @ T_A = 70°C	Continuous Drain Current, V_{GS} @ 10V	4.2	
I_{DM}	Pulsed Drain Current①	42	
T_J , T_{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

	Parameter	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ③	62.5	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.043	0.050	Ω	V_{GS} = 10V, I_D = 5.1A ②
		—	0.056	0.065		V_{GS} = 4.5V, I_D = 4.42A ②

Figure 18 Absolute maximum rating and electrical characteristics from the IRF7341GTRPbF datasheet

The initial application conditions are:

- Ambient temperature T_a = 120°C
- Solenoid inductance L = 5 mH
- Solenoid resistance R_L = 15 Ω
- Pulse frequency f = 125 Hz
- Supply voltage V_{DD} = 14.5 V

By applying Kirchhoff's laws to the fuel injection coil circuit, we find:

$$V_{DD} = L\frac{di(t)}{dt} + R_L i(t) + V_{AV} \quad (11)$$

Using boundary conditions at t = 0 and i(t) = IL = I_{AR} yields the general solution in the time domain:

$$i(t) = I_{AR} e^{\left(-\frac{R_L}{L}t\right)} + L\frac{V_{AV} - V_{DD}}{R_L}\left[e^{\left(-\frac{R_L}{L}t\right)} - 1\right] \quad (12)$$

Solving for the avalanche pulse width (t_{AV}) assuming i(t_{AV}) = 0 gives:

$$t_{AV} = \frac{L}{R_L}\ln\left(1 + \frac{I_{AR}\cdot R_L}{V_{AV} - V_{DD}}\right) = \frac{5\ mH}{15\ \Omega} ln\left(1 + \frac{0.962A\ \cdot 15\ \Omega}{71.5\ V - 14.5\ V}\right) = 75\ \mu s \quad (13)$$

Avalanche voltage can be obtained from measurement, ideally, otherwise estimated from the IRF7484 datasheet using equation (6) as:

$$V_{AV} \cong 1.3 \cdot BV_{DSS} = 1.3 \cdot 55\ V = 71.5\ V \quad (14)$$

And avalanche current can be calculated as:

$$I_L = I_{AR} = \frac{V_{DD}}{R_L + R_{DS(on)}} = \frac{14.5\ V}{15\ \Omega + 1.6 \cdot 50\ m\Omega} = 0.962\ A \quad (15)$$

Repetitive avalanche energy can be calculated as:

$$E_{AR} = \frac{V_{AV} \cdot I_{AR} \cdot t_{AV}}{2} = \frac{71.5\ V \cdot 0.962\ A \cdot 75\ \mu s}{2} = 2.58\ mJ \quad (16)$$

Average power dissipated during avalanche as well as conduction loss can be calculated as:

$$P_{AV} = \frac{E_{AR}}{t_{AV}} = \frac{2.58\ mJ}{75\ \mu s} = 34.4\ W \quad (17)$$

$$P_{ave} = E_{AR} \cdot f = 2.58\ mJ \cdot 125\ Hz = 323\ mW \quad (18)$$

$$P_{cond} = {I_L}^2 \cdot (temperature\ coeff.) \cdot R_{DS(on)} = (0.962\ A)^2 \cdot 1.6 \cdot 50\ m\Omega = 74\ mW \quad (19)$$

Since the avalanche duty cycle can be calculated as:

$$D = t_{AV} \cdot f = 75\ \mu s \cdot 125\ Hz = 0.0094 \quad (20)$$

The average junction temperature at steady-state can be calculated as:

$$T_{SS} = (P_{ave} + P_{cond})R_{\theta JA} + T_a = (323\ mW + 74\ mW\ ) \cdot 62.5°C/W + 120°C = 144.8°C \quad (21)$$

The peak rise in junction temperature due to each avalanche pulse is given by:

$$\Delta T = Z_{TH} \cdot P_{AV} = 0.85 \cdot 34.4\ W = 29.2°C \quad (22)$$

$$T_{J(pk)} = T_{SS} + \Delta T = 144.8℃ + 29.2℃ = 174℃ \leq T_{JMAX} \quad (23)$$

where the thermal impedance (Z_{TH}) is approximated from the transient thermal impedance plot provided with the datasheet, as shown in **Figure 19**.

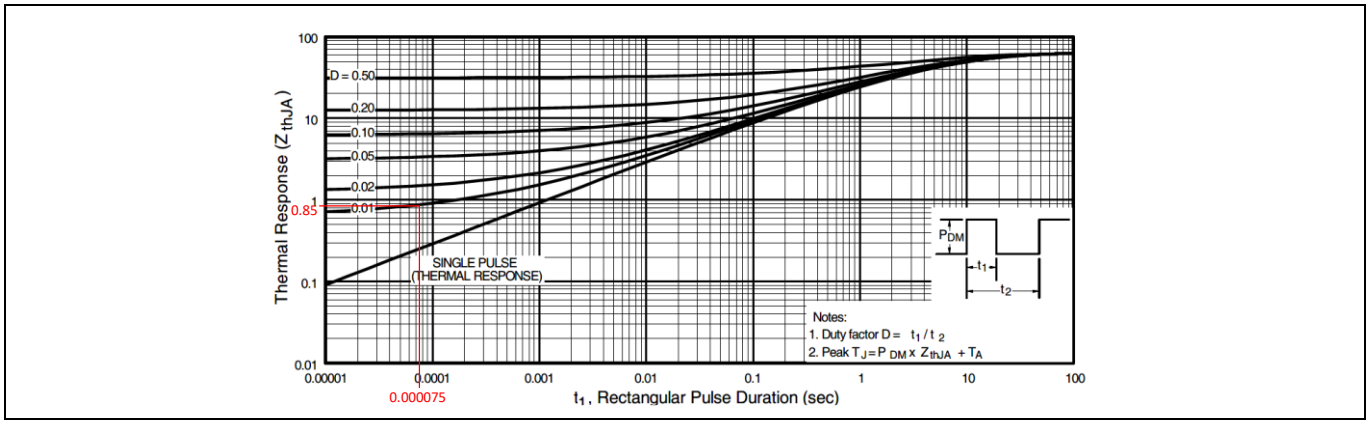

Figure 19 Maximum effective transient thermal impedance, junction-to-ambient from the IRF7341GTRPbF datasheet

4.3 Statistical approach

In this case, a sample of devices are tested for failure without limiting the maximum junction temperature to T_{JMAX}. The test consists of increasing the inductance value under a defined I_{AS} until each device fails. As shown in **Figure 20** (left), the energy, defined as the area under the I_{AS} curve, increases linearly with the load inductance value. Fixing L and increasing I_{AS} until failure occurs can accomplish a similar effect. The failure energy of each device is recorded and plotted so that a failure distribution and E_{AS} value can be found, as shown in **Figure 20** (right). Note that the statistically determined E_{AS} value cannot be used to design for actual avalanche conditions. It represents operation at a single set of conditions that cannot be extrapolated to other circumstances without providing more information. Additionally, the conditions at which statistically rated E_{AS} values are given are mostly outside the normal operation limits at which a part is qualified.

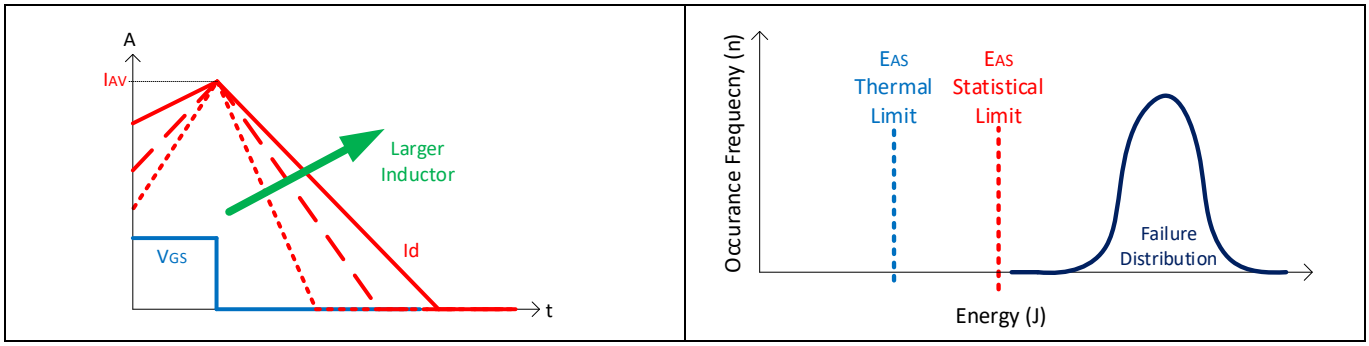

Figure 20 Illustrated $I_{AS(set)}$ vs. t_{AV} waveforms for various inductors (left) and failure energy distribution with limits (right)

Infineon Technologies provides statistically based E_{AS} mostly in conjunction with the thermally limited value and to identify the product screening test numerical values for some IR MOSFET™. Other suppliers sometimes provide only a statistically based value.

5 Buyer beware

Many suppliers rate power MOSFET avalanche capability with only a single number in the datasheet and without providing full circuit or test condition details. The user must be careful in such cases. It is not sufficient to merely compare the numerical values of avalanche energy which appear in the datasheet tables. The following example will help demonstrate why. Since avalanche energy depends on the inductor value and starting current, it is possible to have two pulses with the same energy but different junction temperatures. This phenomenon is illustrated in the following examples in **Table 1**:

Table 1 IRF7749L1TRPbF avalanche calculation for various I_{AS} values with the same E_{AS}

Parameter	Example 1	Example 2
I_{AS}	120 A	35 A
L	44 µH	517 µH
$E_{AS} = \frac{1}{2} L \cdot {I_{AS}}^2$	316 mJ	316 mJ
$t_{AV} = L \cdot \frac{I_{pk}}{V_{AV}}$	≈67 µs	≈232 µs
Z_{th}	0.032°C/W	0.07°C/W
ΔT_J	150°C	96°C
$T_J = T_{start} + \Delta T$	175°C	121°C

Examples 1 and 2 both have the same energy; however, since the inductor varies, so does the junction temperature. While both junction temperatures are within the T_{JMAX}, they are not equal. Please note that Infineon Technologies' power MOSFETs, which are E_{AS} rated, include graphs showing constant junction temperature energy values. See for example **Figure 15** to be sure which value of energy should be compared with another supplier's MOSFET. Another common industry practice is to rate avalanche capability based on curves showing allowable time in avalanche as a trade-off with drain current. At best, such curves are backed up with test failure data, as seen in **Figure 9**. However, sometimes these curves are based on statistically determined limits without apparent regard for junction temperature. The result is that a thermal T_J calculation (see **Table 1**) for the rated allowed condition may show that T_J exceeds T_{JMAX}, without reliability qualification data at this higher-than-T_{JMAX} condition.

6 Conclusion

With many years of evolving experience, Infineon Technologies designs, characterizes and rates power MOSFETs to ensure rugged and reliable operation while in avalanche. Three different classes of avalanche rating are applied:

- The thermal approach allows single pulse and (where indicated) repetitive pulse avalanche operation as long as neither I_{DMAX} nor rated T_{JMAX} are exceeded. Energy loss due to avalanche operation can be analyzed as any other source of power dissipation. Such thermally rated parts are indicated with a rating of E_{AS} and with inclusion of repetitive avalanche SOA graph in the IR MOSFET™ datasheet. See **Figure 16** and **Figure 17** for examples.
- Statistically based avalanche ratings are set based on sample failure statistics. At Infineon Technologies, this rating is labeled $E_{AS(tested)}$ for IR MOSFET™ and corresponds to a production test screening limit. While the statistical approach generally gives higher energy values, it does not provide a practical method for evaluating avalanche capability in conditions that differ from the datasheet. Since circuit designers' conditions usually differ significantly, the statistical approach does not give a clear idea on how to design for occurrence of avalanche.
- Some products were designed by other suppliers without an avalanche rating. Devices without an avalanche rating on the datasheet should not be used in circuits which will see avalanche conditions during any mode of operation.

Power MOSFET users should take care to understand differences in avalanche rating conditions between various suppliers. Devices that are not avalanche robust can cause unexpected and seemingly unexplained circuit failure. Some manufacturers do not rate their MOSFETs for avalanche at all. Others use a statistical rating alone, which does not offer the same assurance for robust operation provided by more complete characterization and rating such as Infineon Technologies uses for E_{AS} rated devices. In this regard, the detail matters; merely contrasting values of avalanche energy that appear in datasheet tables is not an accurate metric for device ruggedness.

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Revision history

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