TO-leaded top-side cooling (TOLT) package power MOSFET

A new package for high-current applications

About this document

Scope and purpose

This document is intended as an introduction to Infineon's innovative TO-leaded top-side cooling (TOLT) package for power MOSFETs. The main advantages of this new package include an increased power density for high-power industrial applications as well as reduced PCB temperatures thanks to decoupling the heat transfer from the current flow. In this document the package concept, thermal performance and board-level reliability of the TOLT are discussed.

Intended audience

This document is intended for engineers working on improving the efficiency of their high-power industrial applications.

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1 TOLT introduction

In recent years the industrial market has become increasingly demanding of industrial MOSFETs. The number of applications, and the transition from mechanical to electronic solutions as well as harsher application conditions all require semiconductor manufacturers to develop new package concepts and implement technology improvements. From through-hole packages, to surface-mount devices (SMDs) like the DPAK or D2PAK, and finally to the latest leadless packages with significantly improved silicon technologies inside, MOSFET solutions are evolving to better address the growing demands of the industrial market.

Infineon is constantly working on bringing superior silicon technologies to the market, and expanding its package portfolio to address a wider variety of industrial applications while meeting even the harshest stress conditions. As a quality leader, Infineon ensures that its products not only fulfill the industrial qualification requirements, but exceed them to enable a longer lifetime and a higher level of robustness.

Alongside traditional MOSFET package concepts like the TO-220, DPAK and D2PAK, Infineon's portfolio also includes a variety of leadless packages, ranging in size and capability from the smallest S3O8, to the mid-range SSO8, and the highest-performing TO-leadless (TOLL) package.

In order to address demanding industrial applications with increasing power requirements, Infineon has introduced a new package concept: the TOLT package, which is based on the TOLL package. Years of experience with the TOLL package and its proven superior reliability have established a solid base for the new top-side cooling variant of the TOLL.

Infineon's TOLT (JEDEC: HDSOP-16) is a new top-side cooling package specially designed to enable the highest power densities for power-demanding industrial applications. This package enhances Infineon's TOLx package family, which includes the TOLL and TO-leaded with gullwing (TOLG) products.

1.1 Target applications

The TOLT helps achieve very high power levels. Thanks to the improved thermal resistance via top-side cooling, it is possible to address power-demanding applications without increasing the component count and system size. For this reason, focus applications for the TOLT package are high-current applications. The package finds relevance in applications such as high-power motor drives with power levels up to 50 kW.

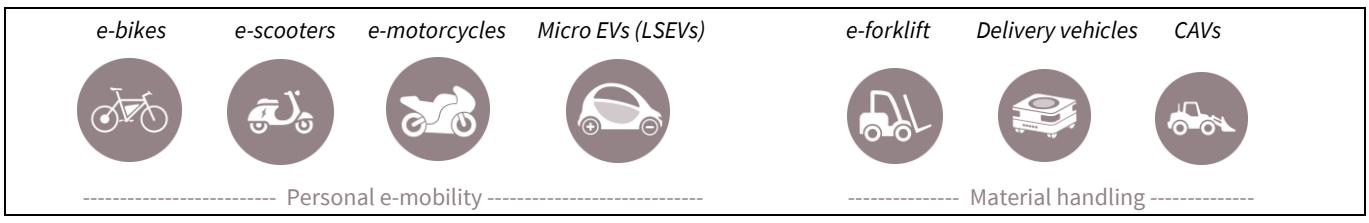

Figure 1 Target applications for the TOLT products

1.2 Package design

The concept of the new TOLT package differs from a standard bottom-cooled power MOSFET. In the TOLT the leadframe inside the package is flipped, and the drain pad (bottom side of the chip = drain connection) is exposed to the top of the package. **Figure 2** shows a side view of the package with the flipped leadframe.

The gate, source and drain pins can be seen in **Figure 3** and **Figure 4**. One row of the eight pins is connected to the exposed pad on top to make the drain connection with the board. On the other side of the package, one pin is used for gate control and the remaining seven pins are connected to the source for the current flow.

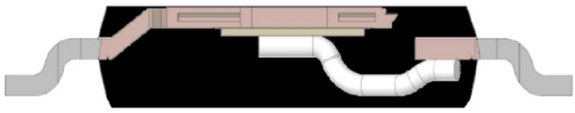

Figure 2 TOLT side view

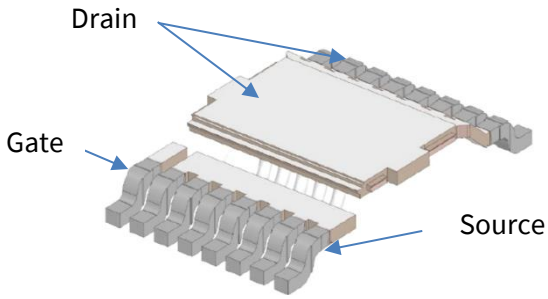

Figure 3 TOLT 3D view (without mold compound)

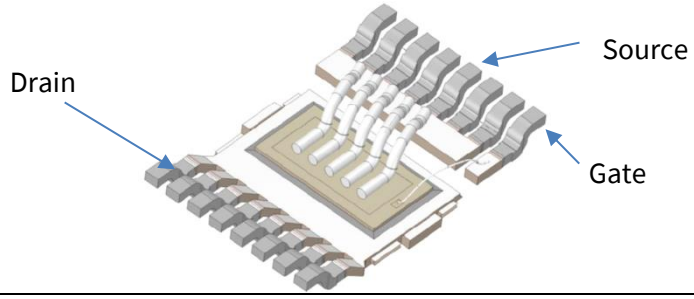

Figure 4 TOLT bottom view (without mold compound)

1.3 Negative standoff

Infineon has taken several measures to keep the package height tolerances as low as possible. One example of those measures is the leads' negative standoff. In this package the leads are lifted slightly above the package body so that when the package is placed on the board the pins do not make contact with the PCB. The solder material used to connect the lead tips to the PCB fills the space between the leads and the board, thereby reducing the potential height increase. Because package height tolerances influence the thermal interface material (TIM) thickness – and, as a result, the thermal performance – negative standoff is an important feature of the TOLT package. Without negative standoff, pin tolerances would be added to package body height tolerances, which would result in a thicker layer of TIM being needed. Due to the two bending processes the tolerances are kept low – between 0.1 and 0.16 mm.

Figure 5 Negative standoff concept. Left: without negative standoff. Right: with negative standoff

1.4 Package outline

Figure 6 shows the dimensions of the TOLT package in detail. The height tolerances are kept tight in both directions, at ±0.05 mm. For the negative standoff, the tolerances are 0.01 to 0.16 mm.

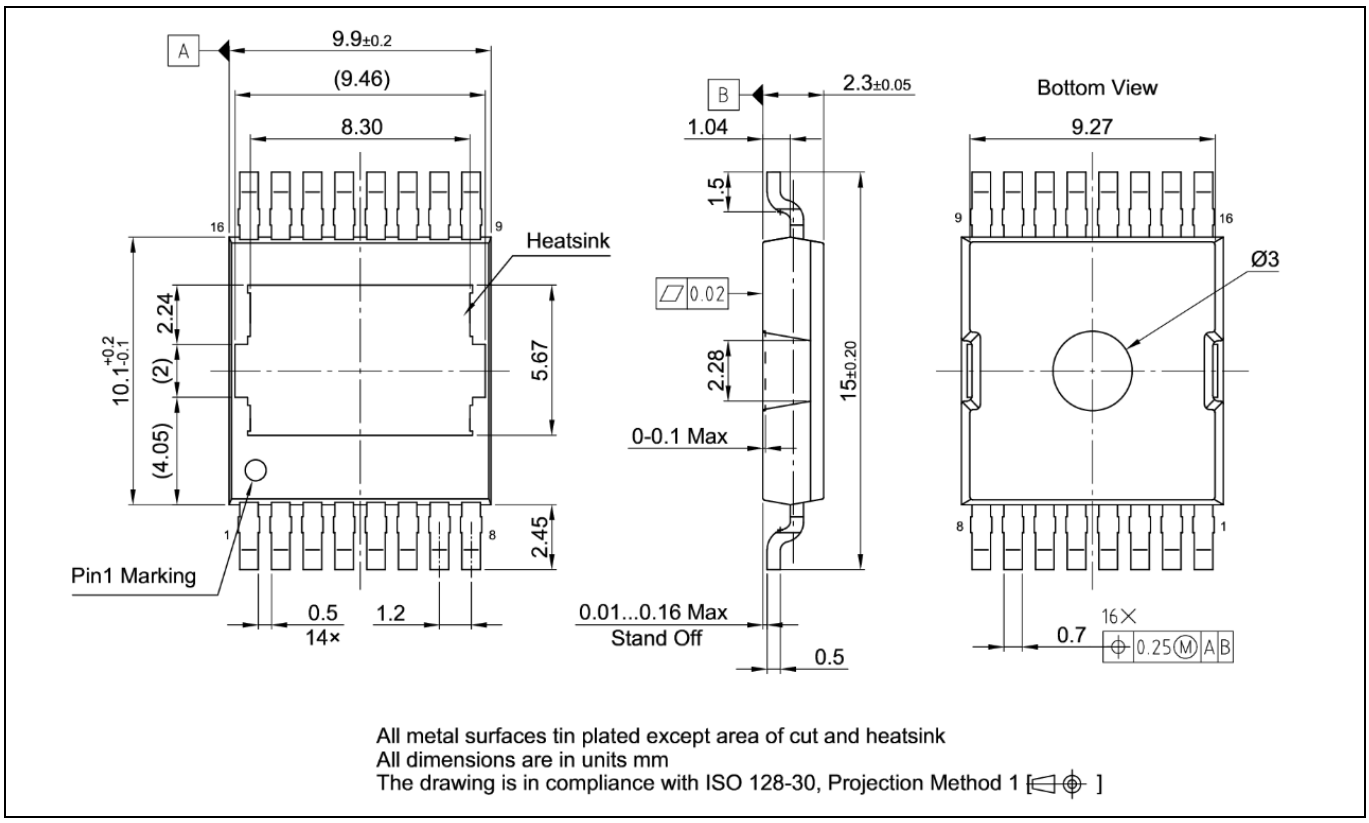

Figure 6 TOLT package outline drawing

2 TOLT advantages and guidelines

With topside cooling, not only is it possible to achieve a higher application power, but there are several other important advantages. Those advantages as well as general guidelines are introduced in this section.

2.1 Cooling concept

In the standard cooling concept (**Figure 9**, left) the heatsink is typically mounted below the PCB. The path for the heat transfer from the chip to the outside is the following:

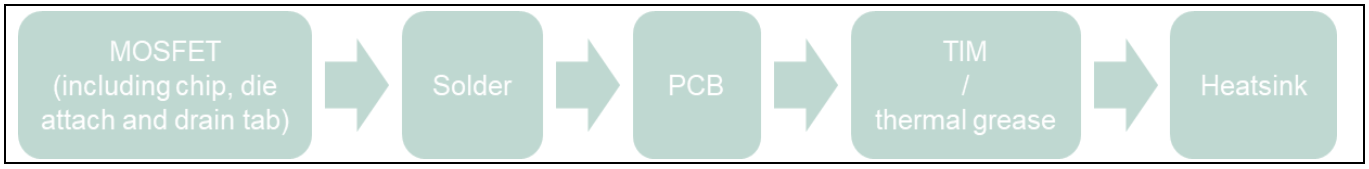

Figure 7 Heat path in a back-side cooling setup

Such a solution has the disadvantage of a reduced thermal performance depending on the PCB and the TIM/thermal paste's parameters. The poor thermal conductivity of these components may cause overheating and a reduction in application power, and might mean higher cooling costs. Additionally, the assembly boards need to withstand higher temperatures, which entails using more expensive PCBs.

Thanks to the top-side cooling concept (**Figure 9**, right) the heat path can be significantly shortened:

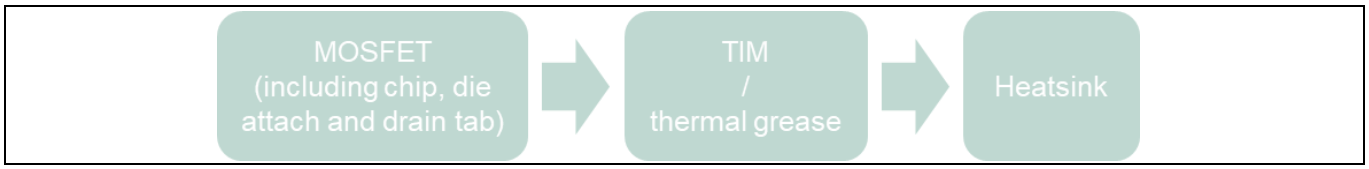

Figure 8 Heat path in a topside cooling setup

Reduction of the heat path by eliminating the PCB and solder interconnect from the heat path has a huge impact on MOSFET performance. Infineon investigated both solutions and the result was that, even assuming a conservative scenario, the total thermal resistance R_{th_JH} from the junction to the heatsink can be improved by at least 20 percent when using FR4-type PCBs.

For a designer of the power stage this means either cost savings for cooling systems for the same application power, or the possibility of reaching higher power output with the same system concept.

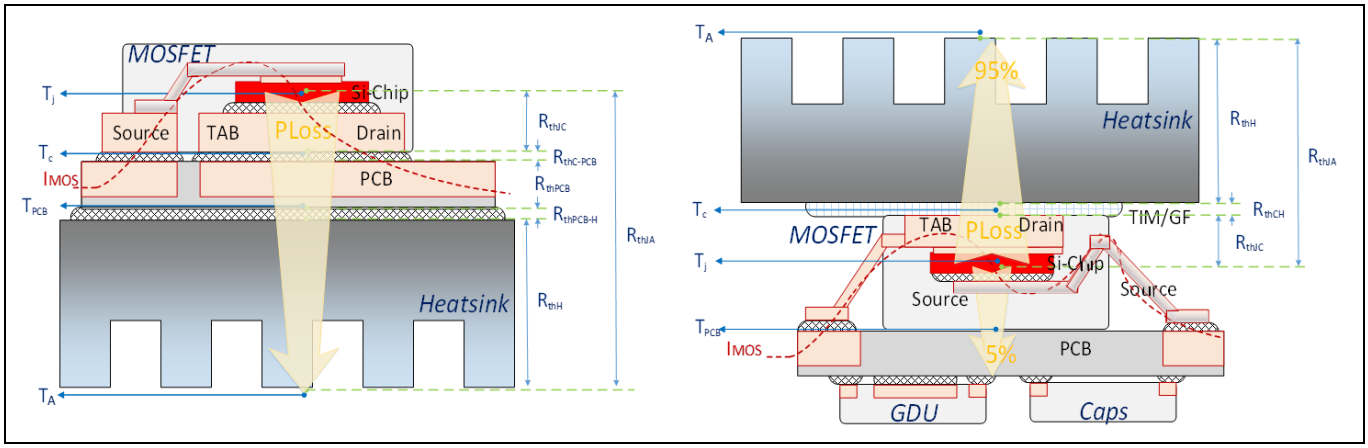

Figure 9 **Left: standard back-side cooling. Right: topside cooling**

2.2 Tin-free exposed pad

To ensure good solderability of SMD MOSFETs, all exposed pins and pads are typically tin-plated. During reflow, the tin plating melts and forms an alloy with the solder material applied on the board.

For systems with the top-side cooling MOSFET, the heatsink is mounted not below the PCB but directly on the MOSFET's exposed (drain) pad on top, as seen in **Figure 9**, right. In most cases the heatsink will, however, not be soldered to the MOSFET but connected to it with an electrically isolating TIM. In this case the tin-plating loses its purpose and may be seen as a disadvantage. Several reflow tests showed that during the reflow process the tin on the exposed pad melts and creates an uneven surface. This may bring a few disadvantages, such as additional package tolerances that may make it more difficult to apply the TIM properly. As a result, a thicker layer of TIM may lead to thermal inequality in cooling of the entire system, or even one MOSFET alone. Since the performance of the TOLT package strongly depends on the thickness of the applied TIM, any additional height may reduce the total thermal performance.

Considering this, it is reasonable not to plate the exposed pad with tin to avoid lump solder after customer reflow and to create a flat surface for the best possible thermal performance of the TOLT package.

To protect the exposed copper from oxidation, the copper is plated with additional passivation layers.

2.3 Additional advantages

Besides achieving higher power densities or cost savings for cooling systems, there are other advantages of TOLT products. Here are some examples:

- Other components can be mounted on the other side of the PCB. Because the heatsink is not mounted under the PCB, and there's no heat going through the bottom side of the MOSFET to the board, gate drivers or capacitors can be placed on the opposite side of the PCB. Such a solution enables a more efficient use of PCB space.
- Creepage distance (distance between source and drain potentials) is increased.
- Use of PCBs with a lower glass transition temperature is possible.
- Less heat is being transferred into the PCB and nearby components.

2.4 Thermal interface material thickness

Optimizing the TIM thickness is crucial to guaranteeing the best thermal performance of the TOLT package and keeping the thermal resistance as low as possible. For the TOLT, Infineon simulated several scenarios with different TIM thicknesses to analyze their impact on the total R_{th} from junction to heatsink. In the simulations the heatsink temperature was fixed to an ambient temperature of 85°C.

Figure 10 shows the dependency of the R_{th} on thermal conductivity of the TIM, for different TIM thicknesses.

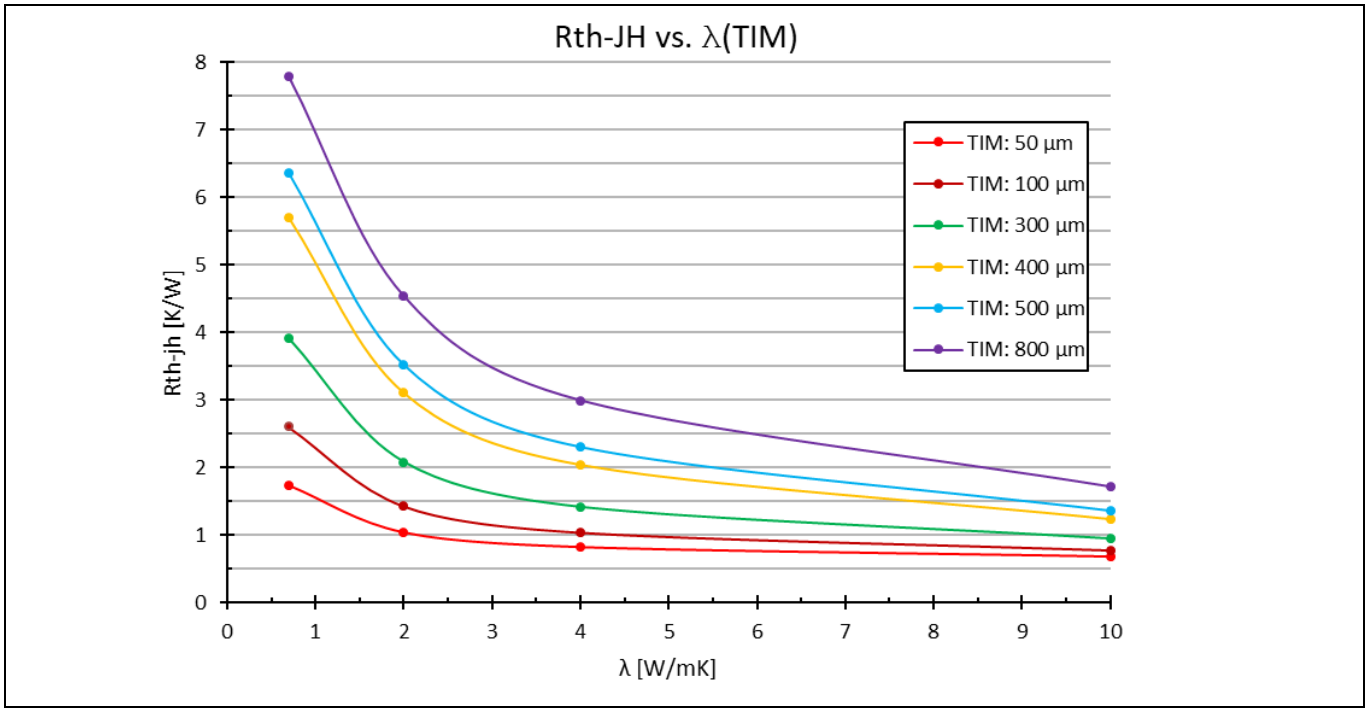

Figure 10 Static results of TIM simulation

As can be seen from the graph, the thinner the TIM, the lower the thermal resistance. However, attention should be paid to the value of thermal conductivity (λ) of the TIM. Better thermal conductivity compensates for the negative influence of the TIM thickness.

The thermal conductivity of TIMs available on the market typically ranges from 3 to 6 W/mK. To achieve the best thermal performance balanced with sufficient electrical isolation, system engineers should optimize both the thickness and the thermal parameters of the TIM. **Table 1** shows a few examples of TIMs currently available on the market.

Table 1 Examples of TIMs available on the market

	Gap pad HC 5.0	Gap pad 3500ULM	Gap filler 4000	Liqui-form 3500	Slim TIM 10000	T-flex UT20000	G-777	TCP 4000 D
Manufacturer	Bergquist®	Bergquist®	Bergquist®	Bergquist®	Laird™	Laird™	Shin-Etsu	Loctite®
Material form	Gap filler	Gap filler	Liquid gap filler	Liquid formable gel	Si-free gap filler	Ceramic-filled silicone sheet	Thermal grease	Phase-change TIM
Thermal conductivity [W/mK]	5.0	3.5	4.0	3.5	5.5	3.0	3.3	3.4

The most common materials used by customers and widely seen on the market are TIMs with thermal conductivity in the range of 3 to 4 W/mK. According to the simulation for this value, the thermal resistance between the MOSFET's junction and the heatsink varies between 0.8 and 3 K/W, depending on the TIM thickness. A realistic TIM thickness of 300 to 500 µm enables reaching thermal resistance values between 1.5 and 2.4 K/W. With the R_{th} equal to 2.4 K/W and the temperature difference between the MOSFET's junction and its case being 90°C (assuming T_{case} = 85°C and T_{jmax} = 175°C), a single TOLT MOSFET can dissipate roughly 40 W of power.

2.5 Electrical parameters

MOSFETs in the TOLT package have the same $R_{DS(on)}$ values as the corresponding TOLL parts. For example, the best-in-class 100 V MOSFET in the TOLT package (**IPTC015N10NM5**) and the corresponding TOLL (**IPT015N10N5**) both have an $R_{DS(on),max}$ of 1.5 mΩ.

Table 2 Parameter comparison: TOLL vs. TOLT

	TOLL	TOLT
$R_{DS(on),max}$ [mΩ]	1.5	1.5
$R_{DS(on)}$ improvement		–
R_{thJH} [K/W]*	5.3	2.74
R_{thJH} improvement		-48 percent
$T_{J,max}$ [°C]	175	175
$T_{J,max}$		–
ΔT [K] (T_{case} = 100°C)	75	75
ΔT [%]		–
$R_{package}$ [mΩ]	0.2	0.25
$R_{package}$ [%]		+25 percent
L_s [nH]	1.5	4**
L_s [%]		+166 percent**
P_{tot} [W]	14.15	27.37
P_{tot} [%]		+93 percent

** 2s2p board with vias. Heatsink temperature fixed to $T_{ambient}$ = 85°C*
*** Depending on layout*

The biggest improvement of the TOLT compared to the TOLL is a visible reduction in R_{th} junction-to-heatsink considering a common 2s2p board with vias and an 85°C ambient temperature. A near-50 percent reduction in R_{th} leads to an improvement in total dissipated power that's above 90 percent.

The added package leads on the TOLT result in a slightly higher package resistance and inductance compared to the TOLL. However, with an optimized design of PCB copper traces the overall circuit resistance and parasitic inductance can be minimized.

3 Soldering and assembly recommendations

For detailed soldering and assembly recommendations, please refer to the "**Board Assembly Recommendations – Gullwing**" document available online.

4 Board-level reliability of the TOLT

Another important topic for all SMD MOSFETs is board-level reliability under different application conditions. Using these MOSFETs in demanding industrial applications subjects the parts to substantial mechanical stress. The most common test used to assess a package's reliability on the PCB is the temperature cycling on board (TCoB) test. For the TOLT package the heatsink is mounted on top of the package, so the maximum mechanical force the part can withstand must also be investigated. Please note that that the results from our standard test setup may not be entirely transferrable to other designs, setups or layouts.

4.1 Temperature cycling on board reliability

During operation, electronic components are exposed to changing temperatures, which leads to material expansion. Each material is characterized by its own thermal expansion coefficient, and if the stress is significant enough, the differences in thermal expansion rates may cause cracks in the solder joints. The test that proves robustness against thermo-mechanical stress is the TCoB test. The IPC-9701 standard defines how and under which conditions the TCoB test should be conducted. **Figure 11** shows the test conditions for different applications, and **Figure 12** shows the test conditions for parts used in automotive applications.

Product Category (Typical Application)	Temperature, °C / °F(1)		Worst-Case Use Environment						
	Storage	Operation	Tmin(2) °C / °F	Tmax(2) °C / °F	ΔT(3) °C / °F	t_D(4) hrs	Cycles/year	Typical years of Service	Approx. Accept. Failure Risk, %
Consumer	-40/85	0/55	0/32	60/140	35/63	12	365	1-3	1
Computers and Peripherals	-40/85	0/55	0/32	60/140	20/36	2	1460	5	0.1
Telecomm	-40/85	-40/85	-40/-40	85/185	35/63	12	365	7-20	0.01
Commercial Aircraft	-40/85	-40/85	-55/-67	95/203	20/36	12	365	20	0.001
Industrial and Automotive - Passenger Compartment	-55/150	-40/85	-55/-67	95/203	20/36 &40/72 &60/108 &80/144	12 12 12 12	185 100 60 20	10-15	0.1
Military (ground and shipboard)	-40/85	-40/85	-55/-67	95/203	40/72 &60/108	12 12	100 265	10-20	0.1
Space leo geo	-40/85	-40/85	-55/-67	95/203	3/5.4 to 100/180	 1 12	 8760 365	5-30	0.001
Military Aircraft a b c Maintenance	-55/125	-40/85	-55/-67	125/257	40/72 60/108 80/144	2 2 2	100 100 65	10-20	0.01
					&20/36	1	120		
Automotive (under hood)	-55/150	-40/125	-55/-67	125/257	60/108 &100/180 &140/252	1 1 2	1000 300 40	10-15	0.1

Figure 11 IPC-9701: performance test methods and qualification requirements for surface-mount solder attachments

Test Condition	Mandated Condition
Cycle (TC) Condition:	
TC1	*0°C ⟷ +100°C (Preferred Reference)*
TC2	-25°C ⟷ +100°C
TC3	-40°C ⟷ +125°C
TC4	-55°C ⟷ +125°C
TC5	-55°C ⟷ 100°
Test Duration	Whichever condition occurs FIRST: 50% *(Preferred 63.2%)* cumulative failure (Preferred Reference Test Duration) or
Number of Thermal Cycle (NTC) Requirement:	
NTC-A	200 cycles
NTC-B	500 cycles
NTC-C	1,000 cycles (Preferred for TC2, TC3,and TC4)
NTC-D	3,000 cycles
NTC-E	*6,000 cycles (Preferred Reference TC1)*
Low Temperature Dwell Temperature Tolerance (preferred)	10 minutes +0/-10°C (+0/-5°C) [+0/-18°F (+0/-9°F)]
High Temperature Dwell Temperature Tolerance (preferred)	10 minutes +10/-0°C (+5/-0°C) [+18/-0°F(+9/-0°F)]
Temperature Ramp Rate	≤20°C [36°F]/minute
Full Production Sample Size	33 component samples (32 test samples plus one for cross-section, add additional 10 samples for rework, if applicable)
Printed Wiring (Circuit) Board (PWB/PCB) Thickness	2.35 mm [0.093 in]
Package/Die Condition	Daisy-Chain Die/Package (see Table 4-2)
Test Monitoring	Continuous Monitoring (see Table 4-4, Preferred Reference-Event Detector)

Figure 12 IPC-9701: temperature cycling requirements, and mandated and preferred test parameters within mandated conditions

What can be read from **Figure 11** and **Figure 12** is that an automotive part should withstand 1,000 cycles from -45°C to +125°C without failure. Despite the industrial qualification, Infineon MOSFETs are still tested according to the harsher automotive standard. According to the standard, the temperature ramp rate shall be less than 20°C per minute. However, during Infineon's TCoB test the ramp rate condition amounts to 60°C per minute. This increases the stress on the devices and meets the requirements of the more stringent thermal shock test. This severe test condition subjects Infineon's packages to significantly more stress than the IPC-9701 standard requires, proving superior robustness and board-level reliability.

During the TCoB test conducted by Infineon, the TOLT parts were monitored and the criterion for an electrical failure was a 20 percent resistance increase. Test results showed that TOLT packages can withstand at least 6,000 cycles without an electrical failure. After 6,000 cycles the test was stopped.

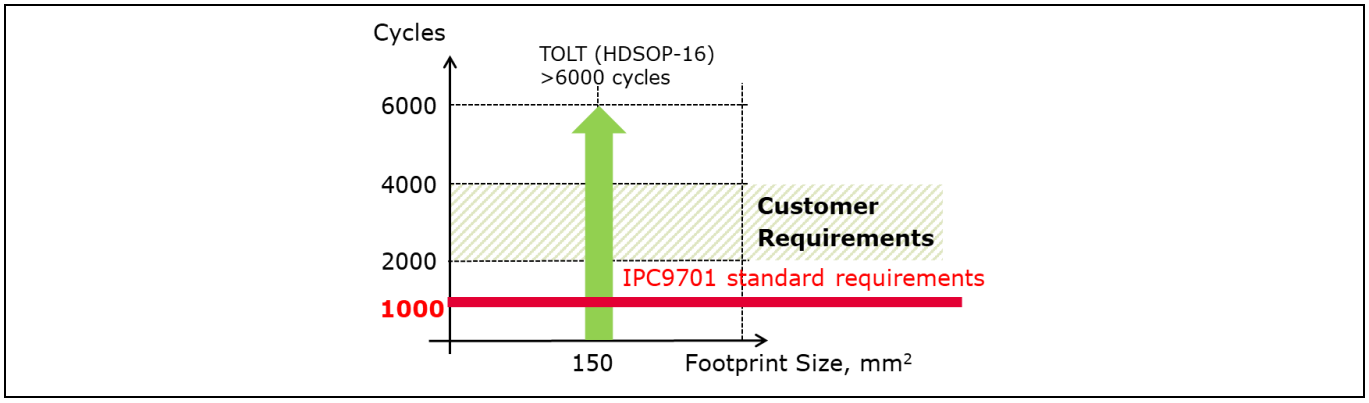

Figure 13 TOLT reaches at least 6,000 cycles in the TCoB test

4.2 Mechanical load/compression reliability

As mentioned previously, the load on top of the package coming from the mounted heatsink causes additional mechanical stress on the package in an application. To prove the reliability of the package with additional mechanical loading, the TCoB test was conducted with pressure being applied to the package's topside.

During this test a force of 20 N was applied to the top of the TOLT package during the TCoB test. Note that this force is by far not the maximum force which can be applied to the TOLT package. The package can withstand a force in excess of 1500 N. **Figure 14** depicts the setup used to generate the required force.

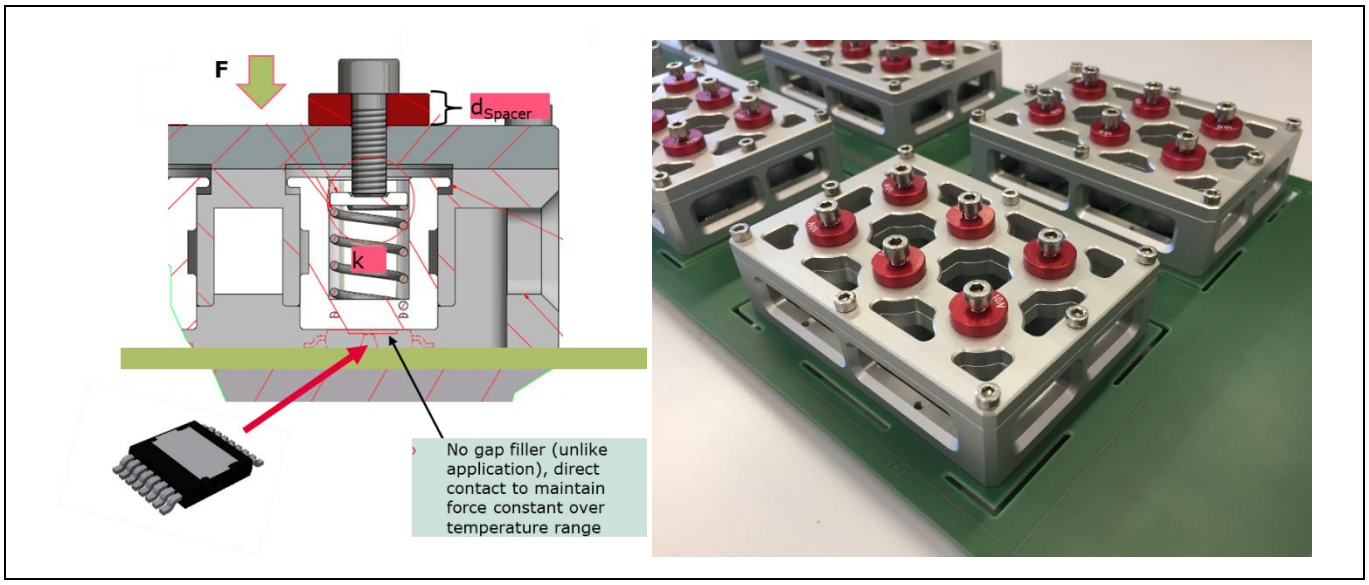

Figure 14 Mechanical load setup. Left: drawing. Right: system view.

During the TCoB test with top loading, the same electrical failure criteria from the standard TCoB test were applied. The test showed that the TOLT can with withstand 3,000 cycles with a force of 20 N being applied on top.

4.3 PCB bending

The TIM between the MOSFET and the heatsink needs to be pressed hard enough to achieve the required thickness and mounting force. Depending on the bolt size and the housing material, the bolting torque may reach 0.5 to 1.0 Nm. Due to the force caused by pressing the heatsink against the TOLT MOSFET, the PCB will bend, which may cause a variation in the gap between the MOSFET and the heatsink (**Figure 15**).

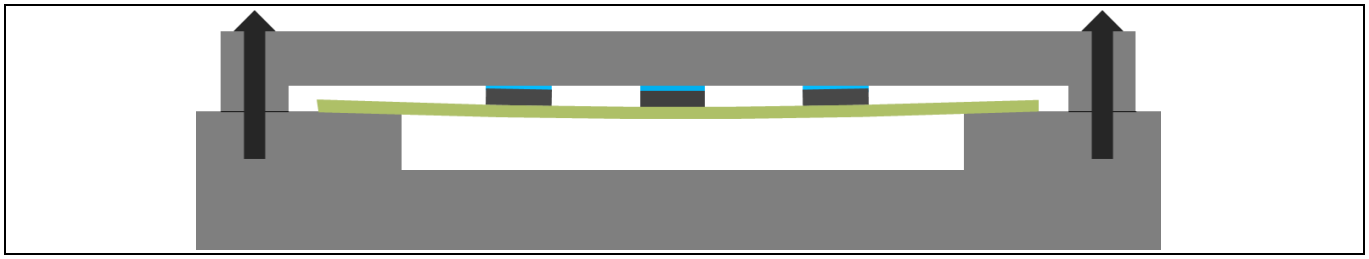

Figure 15 Bending of the PCB under heatsink force

In order to prevent such PCB bending, a proper measure would be to add standoffs under the PCB to act as supporting pillars (**Figure 16**), or to install additional mounting between the heatsink and the PCB (**Figure 17**).

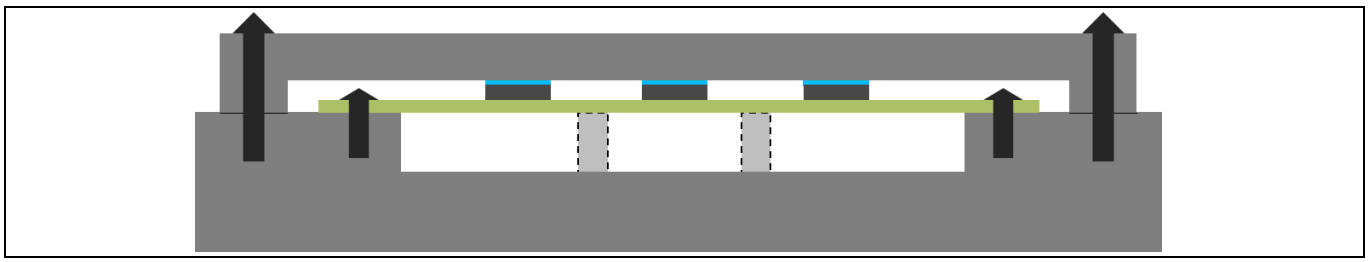

Figure 16 Extra standoffs under the PCB to prevent PCB bending

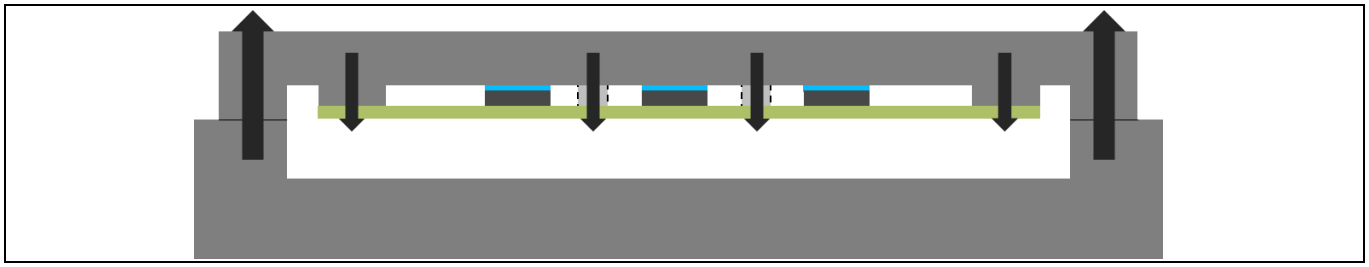

Figure 17 Additional mounting to prevent PCB bending

5 Thermal simulations

In this section the results of thermal simulations with different boards and heatsink mounting configurations are presented and discussed. In the diagrams the thermal impedance values for various configurations can be seen.

Thermal resistance from junction to ambient was simulated with two different configurations of the cooling system:

a) Cooling through the top with a fixed ambient temperature R_{th_JD1} (**Figure 18**), and cooling through the top while leaving the heatsink at natural convection R_{th_JD2} (**Figure 19**).

b) Cooling through both the PCB and the top with a fixed ambient temperature R_{th_JH1D1} (**Figure 20**), and with natural heat convection R_{th_JH2D2} (**Figure 21**).

For each cooling setup, four different PCB configurations were simulated: 2s2p (four-layer PCB with 1 oz. – 2 oz. – 2 oz. – 1 oz. copper layers) with and without vias, as well as 1s0p (one-layer PCB with 1 oz. copper) with and without vias. Thermal conductivity of the selected TIM was 0.7 W/mK, and it was 100 µm thick. The ambient temperature was set to 85°C, where relevant.

As **Figure 18** shows, for the top-side cooling when the heat is transferred directly to the heatsink with active cooling (temperature is fixed), the choice of the PCB does not make a significant difference in terms of Z_{th} performance. This means that cheaper boards with lower glass transition temperatures can be used. Regardless of which board is used, the thermal impedance value amounts to ~2.8 K/W.

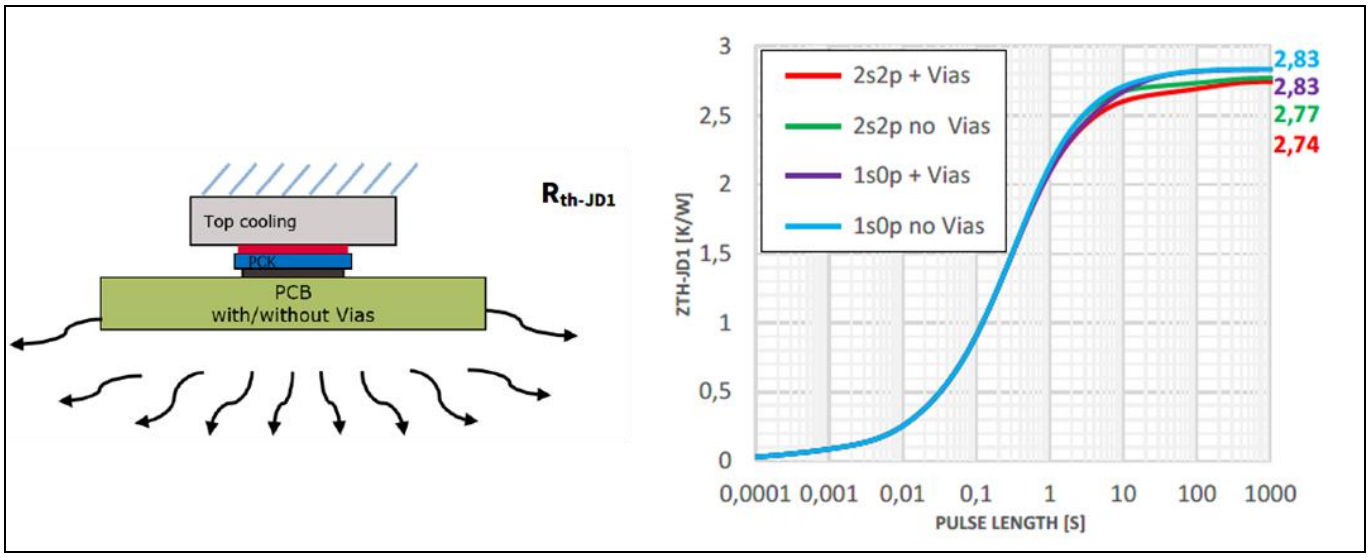

Figure 18 Thermal impedance of TOLT for different boards; top cooling temperature fixed to $T_{ambient}$

In the case of free heat convection (**Figure 19**) the choice of the board may, however, make a difference as some heat will be transferred to the PCB. Thermal impedance for the common 2s2p board would increase to 19.5 K/W.

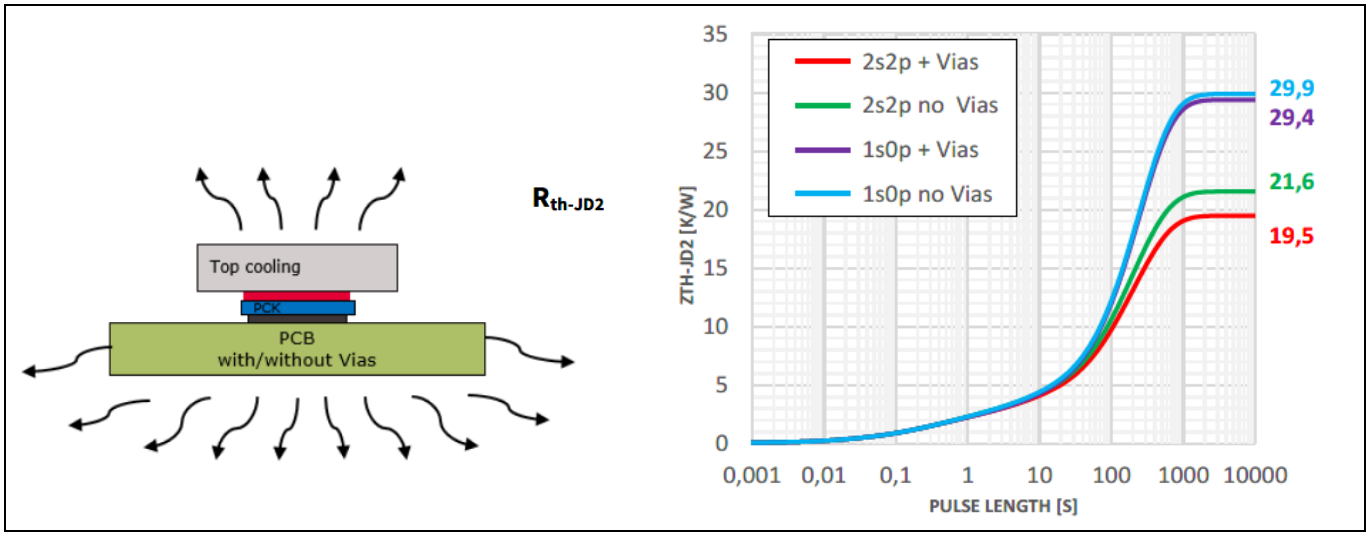

Figure 19 Thermal impedance of TOLT for different boards; free heat convection

Additionally, the simulations show that if a second heatsink is mounted beneath the PCB, the thermal performance will not improve significantly. For example, for a 2s2p board without vias, and with only a heatsink above the package and no heatsink beneath the PCB, the thermal impedance amounts to 2.77 K/W. With an additional heatsink underneath the board, the thermal impedance is slightly reduced to 2.59 K/W, which is negligible. **Figure 20** and **Figure 21** present the results of simulations with a heatsink on both sides.

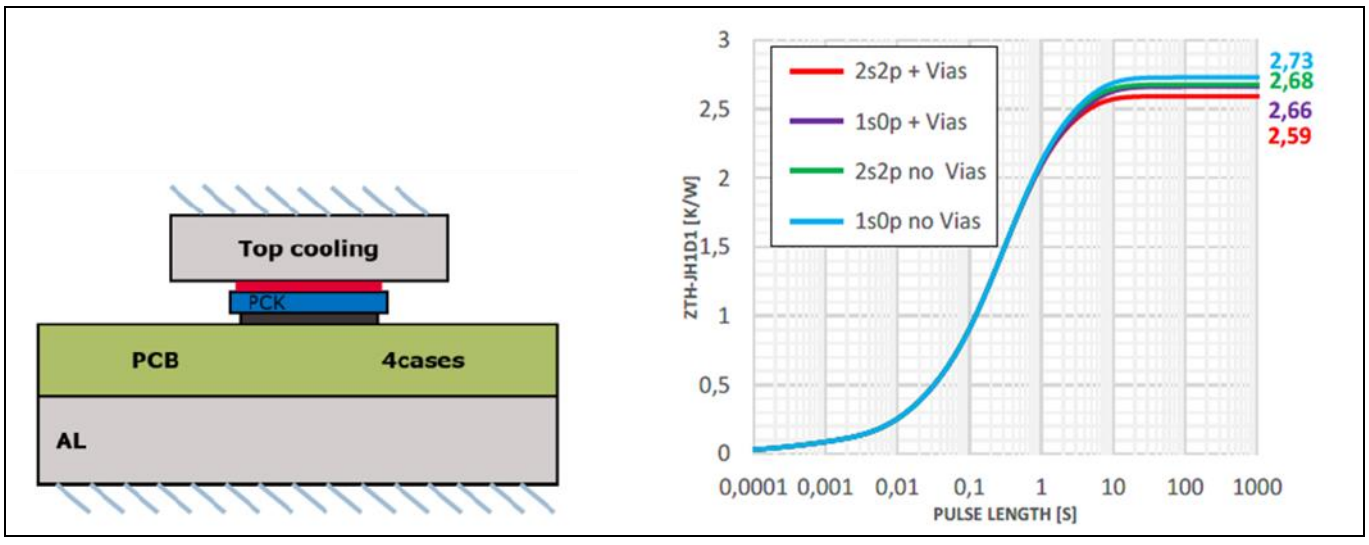

Figure 20 Thermal impedance of TOLT for different boards; top cooling temperature fixed to $T_{ambient}$

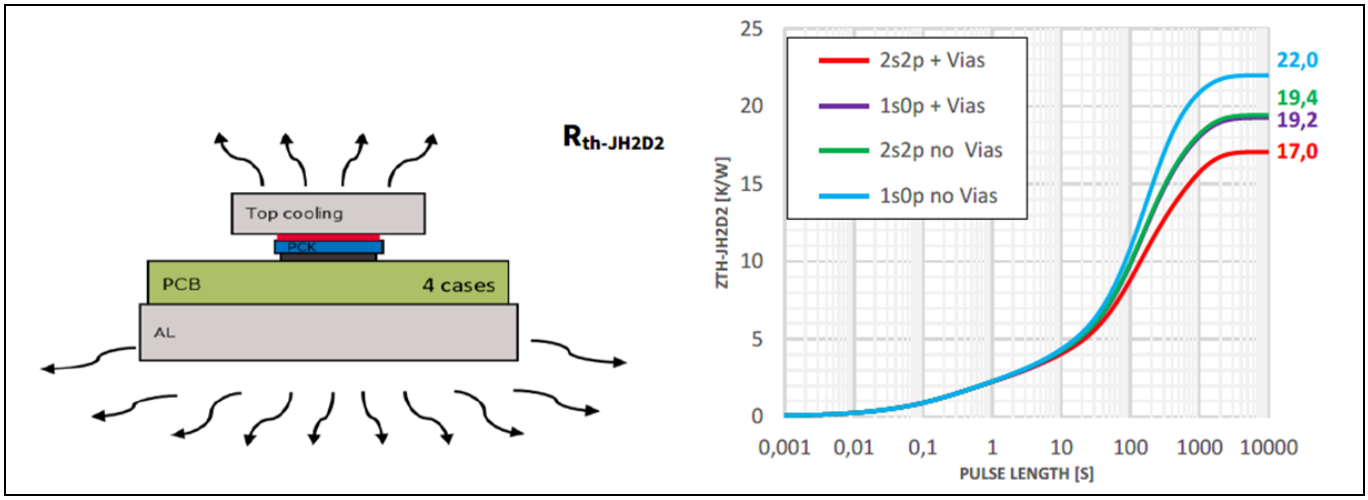

Figure 21 Thermal impedance of TOLT for different boards; free heat convection

6 Summary

With the new top-side cooling TOLT package from Infineon's portfolio of industrial-grade power MOSFETs, high-power industrial applications can be also realized on a FR4 PCB. Thanks to the shortened heat path from the die's junction to the heatsink, the TOLT offers improved thermal resistance and, as a result, improved electrical performance.

To ensure the best thermal performance, different measures were taken during development of the TOLT package. These include minimization of the package height, the introduction of the pins' negative standoff, and having a tin-free exposed pad. A critical aspect influencing the overall thermal performance of TOLT products is the thermal interface material (TIM) between the package's topside and the heatsink. Designers can achieve the desired thermal performance considering the tradeoff between thickness, thermal conductivity and price of TIM.

Thermal simulations confirm a significant improvement of thermal resistance and impedance compared to the standard bottom-side cooling solutions on FR4 PCBs. In addition to the simulations, reliability tests such as temperature cycling on board, and bending and compression tests, were conducted. It has been experimentally proven that the TOLT package can withstand a sufficient number of thermal shock cycles with additional loading on top, exeeding the requirements of common standards.

In addition to the existing TOLL and TOLG packages, the TOLT package enhances Infineon's innovative power MOSFET TOLx portfolio addressing high-power, high-current applications in an efficient and cost-effective way.

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-06-01	Initial release
V 1.1	2022-12-06	Replaced the term “topside-cooled” with “top-side cooling”

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