VADC:Versatile Analog to Digital Converter

XMC™ microcontrollers
September 2016

Agenda

1. Service request generation
2. Safety features

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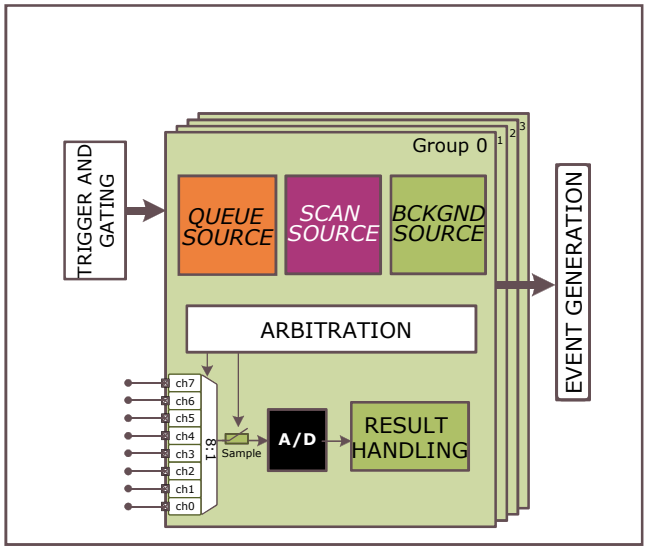
VADC
Versatile Analog to Digital Converter



Highlights

The VADC is comprised of 4* independent analog to digital converters. Each, capable of converting with a resolution of 12-bits at 2 MSamples/sec. This enables highly accurate signal measurement for currents, voltages, temperature signals.

**: depends on the specific device*

Key feature

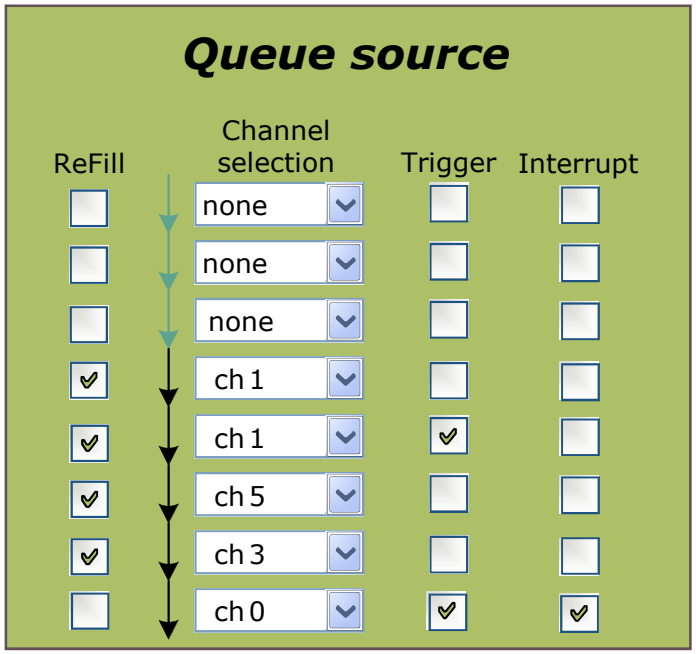
- Flexible sequencing scheme
- Result post-processing
- Triggering and gating conversions

Customer benefits

- 3 flexible request sources (Queue, Scan, Background) for optimized sequence
- Filtering, accumulation without CPU load. 8/10/12-bits results
- External triggering and gating of conversions

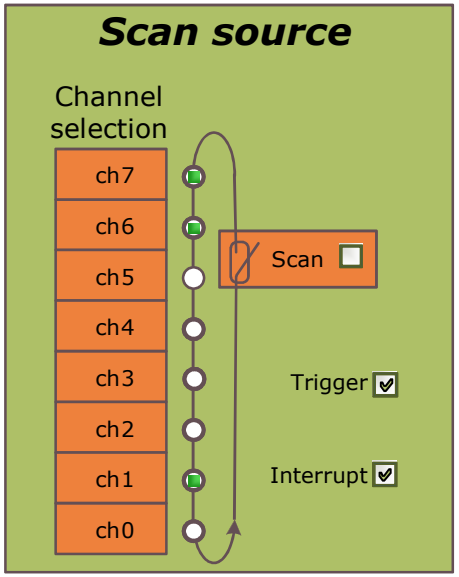
VADC
Flexible sequencing (1/2)

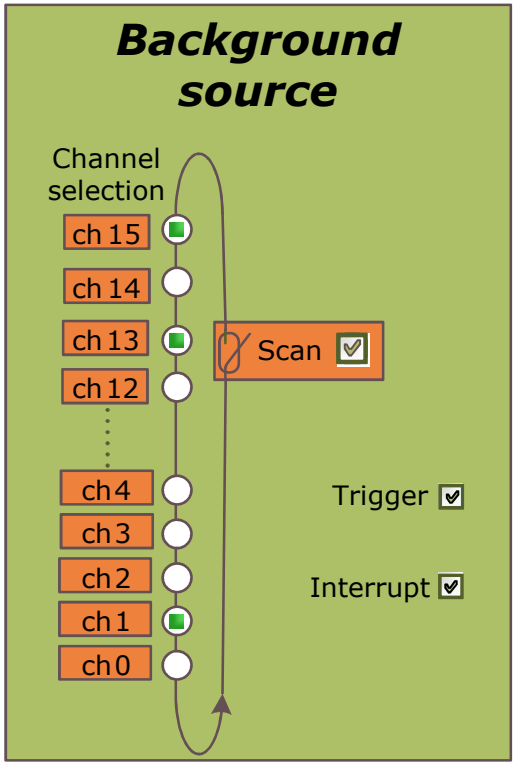
- 3 request sources allows a sophisticated sequencing
  - Queue source → up to 8 channels in 8 stages FIFO with any channel combination possible
  - Refill, source event generation and trigger can be configured individually for any entry in the queue

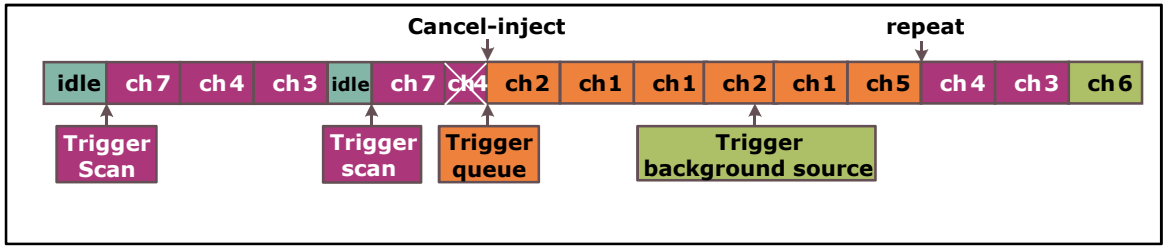


VADC
Flexible sequencing (2/2)

- Scan source → up to 8 channels. Converts from higher number selected until lowest channel number selected
- Background source → a scan source that is able to request conversions in all channels in the microcontroller. It is typically the lowest priority source







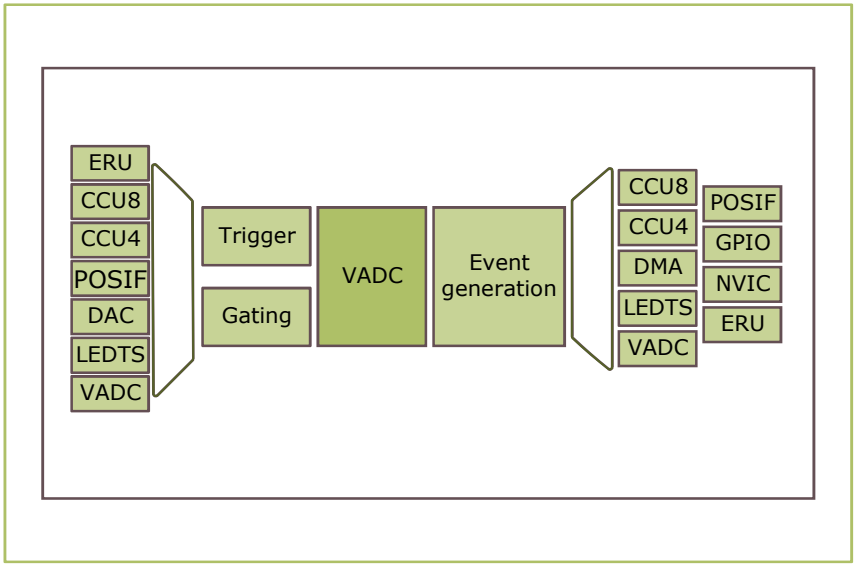
VADC
Result post-processing

- Up to 16 result registers per group (8 channels)
- Additional global result register accessible from any group in the microcontroller
- A post-processing mechanism can execute filtering (FIRs, IIRs), differentiation, or accumulation without CPU interaction
- Wait for read mode blocks new writes in a result register before the content has been read by CPU or DMA for example, to avoid loss of data
- Result events signalize the existence of a new result to other modules or the CPU

VADC
Triggering and gating

- Conversion can be triggered by external events, continuously or by software events
- Full connectivity to other modules for application relevant triggering-gating
- One signal can trigger different groups to allow simultaneous sampling
- A gating mechanism hinders the triggering of a conversion as long as the gating signal is not released

VADC
System integration

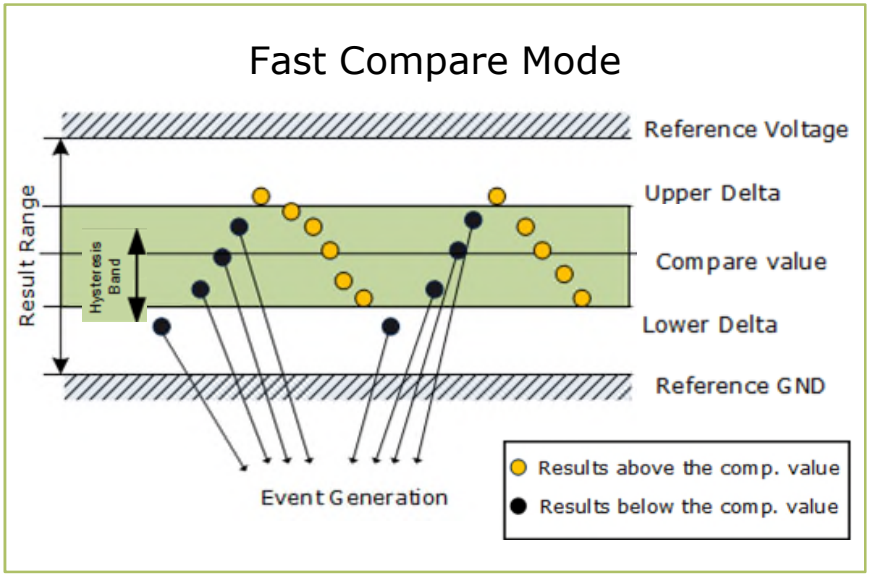


- Target applications
  - Motor control
  - Automation
  - Power conversion
  - General purpose

XMC™4100	XMC™4200	XMC™4400	XMC™4500
2 groups	2 groups	4 groups	4 groups

- The VADC is intelligently connected to other peripherals in the microcontroller, such as CCU8, DMA or NVIC for triggering-gating on the input side and event generation such as interrupt events on the output side
- This provides a perfect starting point for real time applications where the hardware triggering of conversions or signalization of events (i.e. overcurrent) have to happen in a deterministic way with minimum time jitter

Application example
Fast compare



In brief

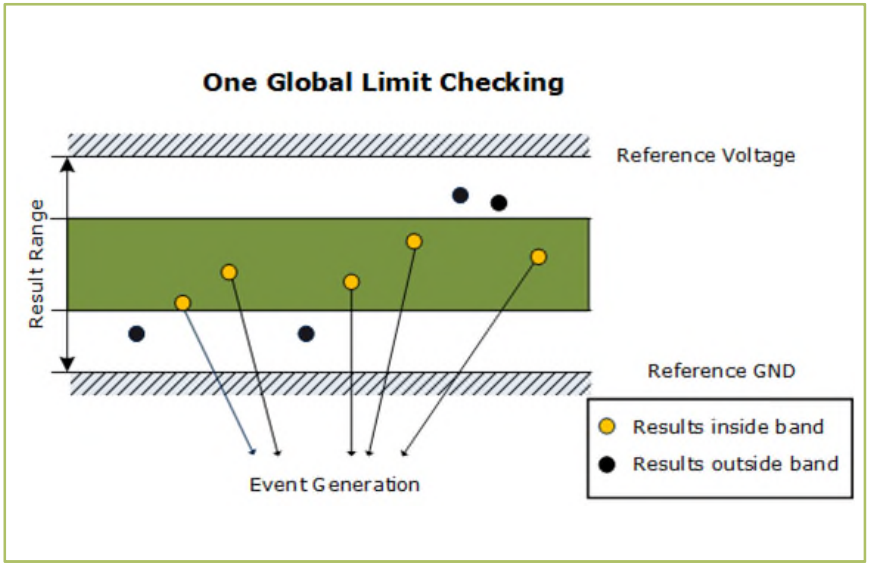
Fast comparison of an analog voltage with a threshold.

Overview

Fast compare mode generates a fast result of a single bit. This bit indicates if the result is above or below a certain pre-programmed reference value. Some hysteresis (delta*) can be built around this threshold in order to avoid oscillations.

**: availability of hysteresis feature in fast compare depends on the specific device.*

Application example
Limit checker



In brief

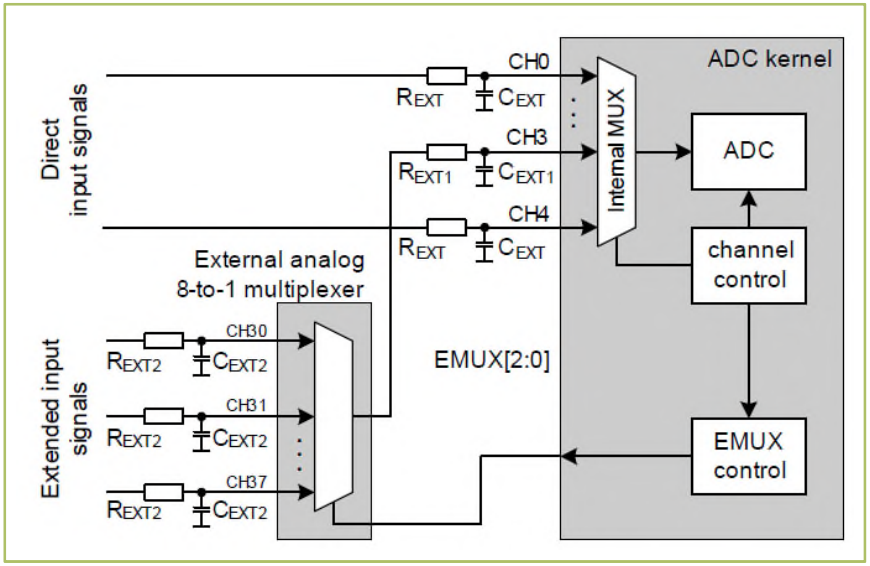
Place some boundaries to create 3 bands in the analog range in order to control the result limits.

Overview

The limit checker permits the control of an analog signal so that when the signal increases or decreases above or below some configurable value, an event can be triggered and an action can be executed.

As an example, a limit checker can detect an overvoltage and generate a stop signal to a timer to avoid damage on the hardware.

Application example
External multiplexers



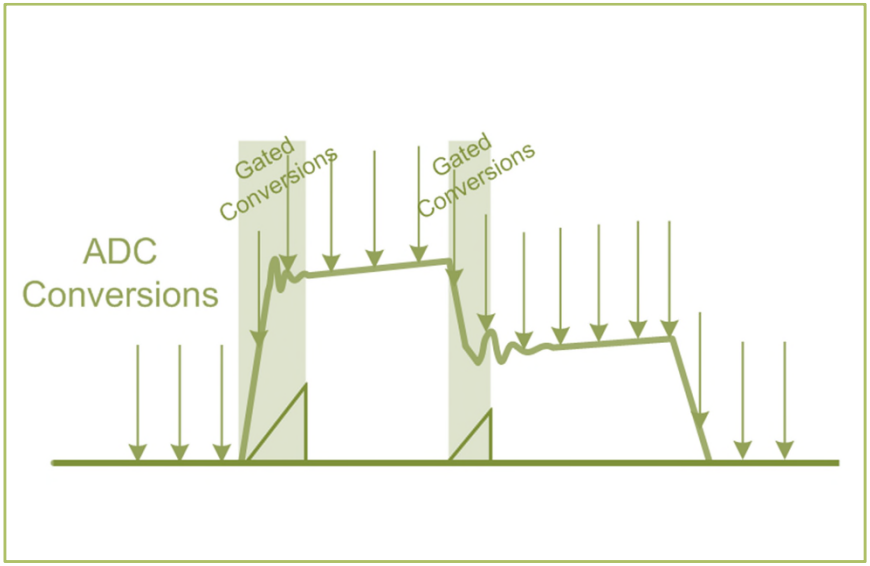
In brief

VADC includes an external multiplexer controller.

Overview

The EMUX controller is able to provide the selecting signals for an external multiplexer. This is synchronized to channel conversion so when the EMUX channel (CH3 in picture) is converted, the EMUX controller detects this and executes a configurable sequencing of the selected signals.

Application example
Blanking time in real time applications



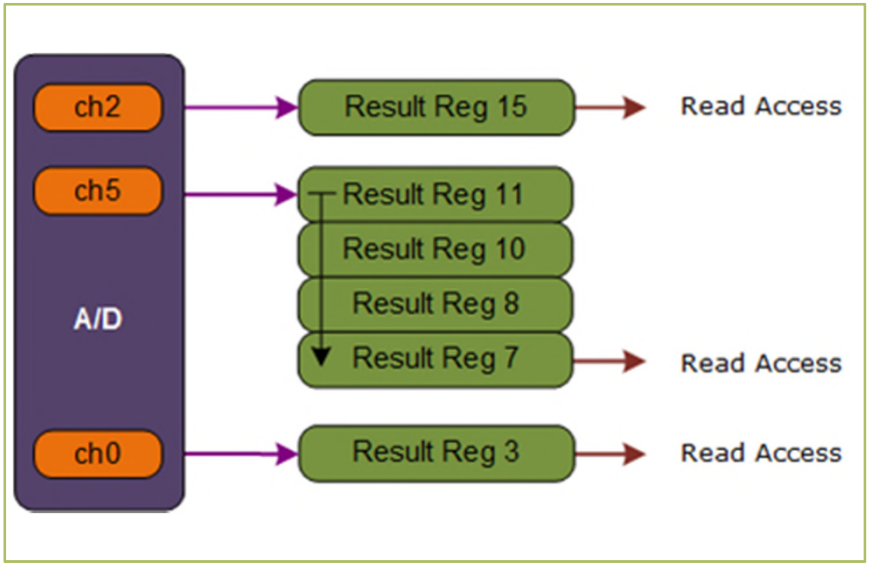
In brief

Gate a continuous running conversion when the information is not relevant for the application.

Overview

Some signals might present oscillations after stepping to a different value. During this oscillation, the value sampled by a continuous converting VADC is not relevant and can be gated through a timer (for example with a status signal –ST) until the signal is settled.

Application example
FIFO on high sampling rate applications



In brief

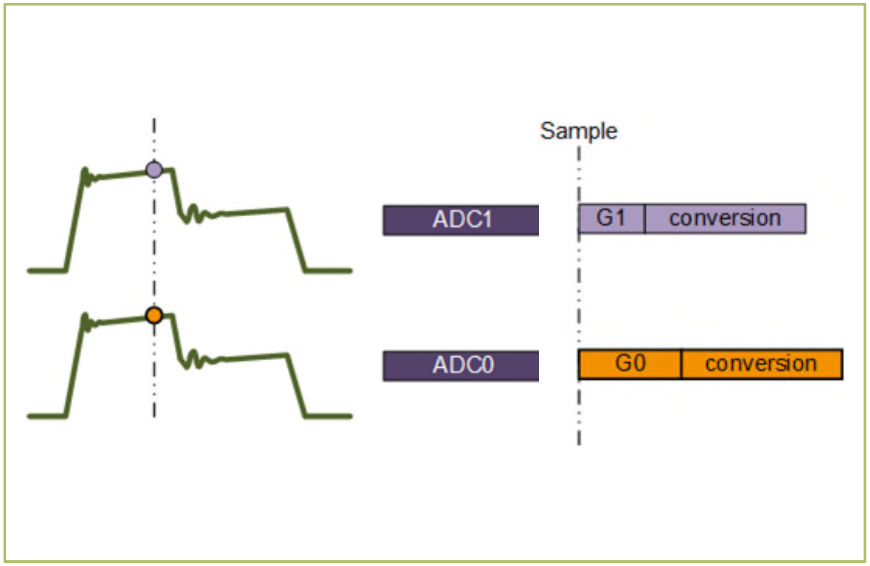
Use a FIFO structure to store results in a safe way.

Overview

Some applications require extreme fast conversions. On the other hand, the CPU load (control loop, for example) might load the CPU in a way that can limit how fast the results of the VADC conversions are read. In this cases, the VADC FIFO result structure will help to conserve results safely, avoiding overwriting, without having to force the CPU to read or slow down the converting rate.

Up to a 16 stages FIFO can be built by means of concatenating result registers. Data reduction mechanisms (filtering, accumulation) as well as event generation is still valid and applicable.

Application example
Synchronous conversions (1/2)



In brief

Sample several signals synchronously.

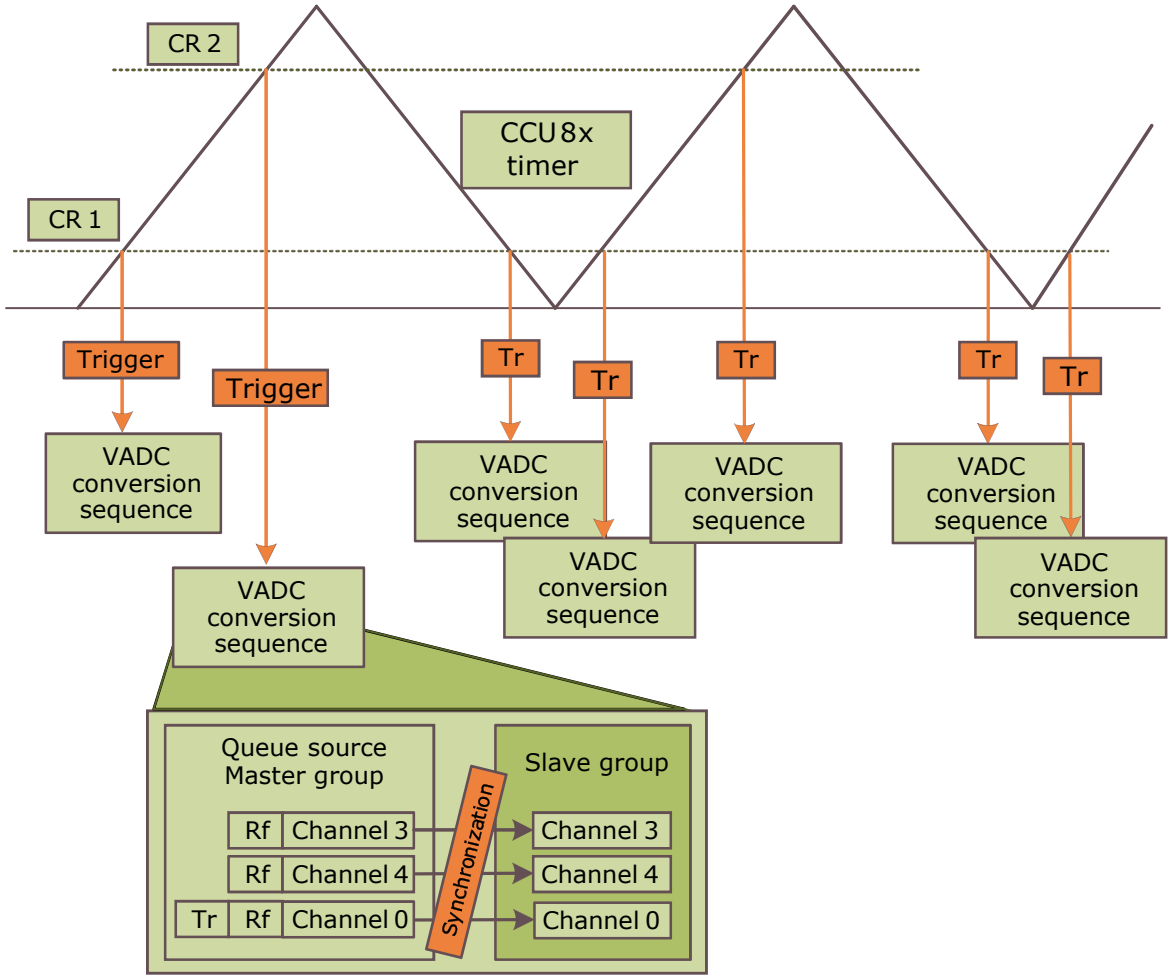
Overview

In many occasions, algorithms request the usage of several analog values that are measured at the same time.

As an example, one could compute the power, for example at a load, by multiplying the current and voltage on it. This calculation would only make sense in case both signals were measured at the exact same point in time.

XMC™4000 allows to measure 2 signals in parallel. The master will request a conversion in its groups. This will automatically lead the request of the same channel number in the slave group. The rest of the VADC features can be used such as result handling, event generation, limit check, etc.

Application example
Synchronous conversions (2/2)

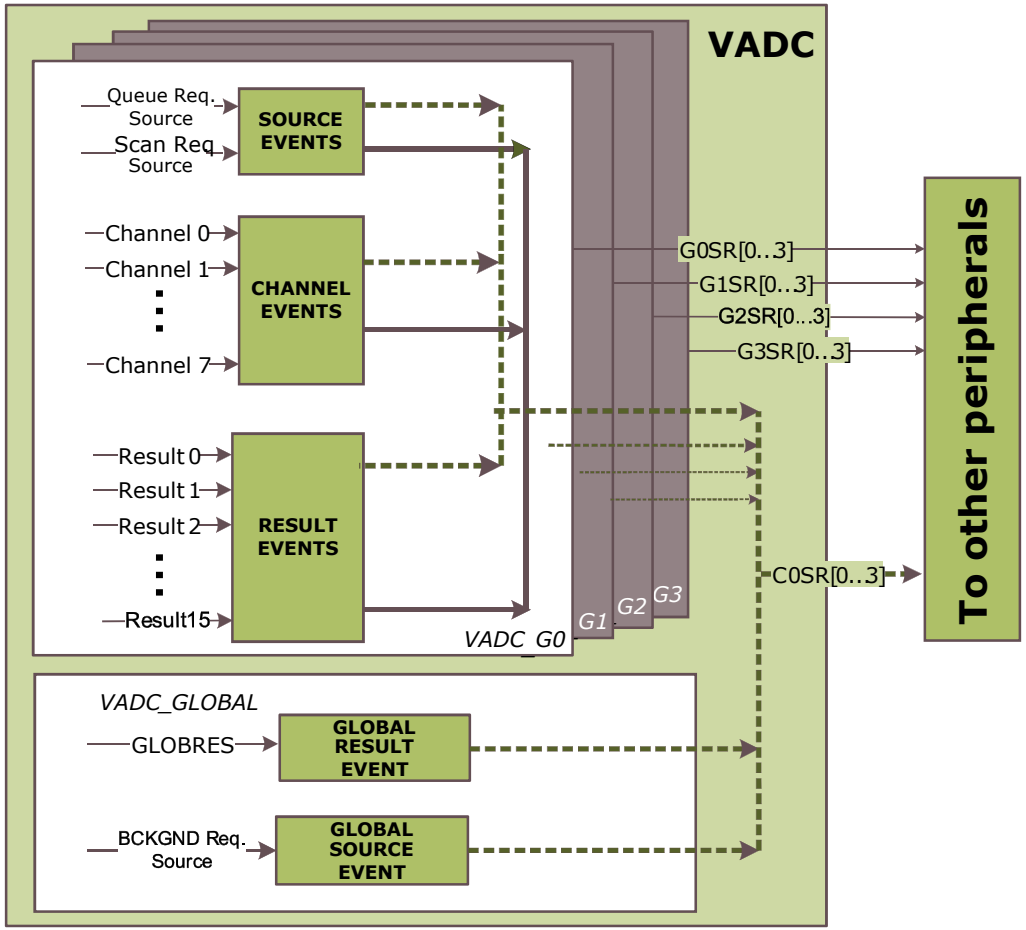


Synchronous conversions: possible sequencing

VADC
Service request generation (1/2)

- 3 different types of service requests can be generated:
  - **Request source event**: channel converted in queue source or sequence finished in a scan source
  - **Channel event**: indicates a channel conversion has finished or in case of limit checker, indicates the corresponding event
  - **Result event**: a new result is available
- The events can be linked to a NVIC node for code execution or to a signal for connectivity to other peripherals

VADC
Service request generation (2/2)



- 2 different kind of request lines are available:
  - **Group specific** are only accessible from the group where the event is generated. Background source events are not included here
  - **Common** request lines. Can be accessed from any group and even from the background source events

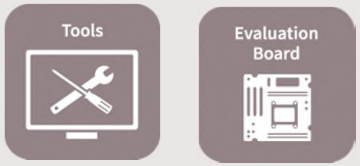
Agenda

1. Service request generation
2. Safety features

VADC
Safety features

- VADC offers a set of safety functionalities including:
  - Broken wire detection for detecting the malfunction of a trace-wire
  - Multiplexer diagnostics can test the existing connection between pins and the internal converter input

Support material

Collaterals and Brochures 	– Product Briefs – Selection Guides – Application Brochures – Presentations – Press Releases, Ads	– www.infineon.com/XMC
Technical Material 	– Application Notes – Technical Articles – Simulation Models – Datasheets, MCDS Files – PCB Design Data	– www.infineon.com/XMC – Kits and Boards – DAVE™ – Software and Tool Ecosystem
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